MOSIS Scalable CMOS Design Rules

(revision 7)

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1 Introduction

1.1 SCMOS Design Rules

This document defines the official layout design rules for MOSIS scalable CMOS (SCMOS) design technology. It supercedes all previous revisions.

In SCMOS technology, circuit geometries are drawn according to Mead and Conway's λ-based methodology [3]. The unit of measurement, λ, can easily be scaled to different fabrication processes as semiconductor technology advances.

A user design submitted to MOSIS in SCMOS technology should be in either Calma GDSII format [1] or Caltech Intermediate Form (CIF version 2.0) [3]. Each design has a technology *designation* that goes with it for the purpose of MOSIS's data prep. At the moment, three designations are used to specify CMOS processes. Each designation may have one or more *options* associated for the purpose of either (1) special features for the target process or (2) the presence of novel device in the design. At the time of writing, MOSIS is offering six CMOS processes from three different foundries with drawn feature sizes ranging from 2.0 μm down to 0.6 μm.

A list of the things that have either been revised or added since our last release can be found in Appendix A. Please refer to the specific sections for detailed descriptions.

2 Standard SCMOS

The standard CMOS technology accessed by MOSIS is a single polysilicon, double metal, bulk CMOS process with enhancement-mode n-MOSFET and p-MOSFET devices [4].