HIGH FREQUENCY PRINTED CIRCUIT BOARD DESIGN

HIGH DENSITY DESIGN

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INTRODUCTION

Packaging Requirements

Bakoglu, Page 82, Table 3.1

Interconnections

- processor speed increasing faster than ability of packaging to handle
- 1990: 50% of system delay from package delays
- 2000: 80% of system delay from package delays

Density

- performance
- improved mounting methods

Thermal Effects

- performance
- reliability

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INTERCONNECTIONS

Effects of Improved Technology

- determine effect of reduced feature sizes on behavior
- first-order (constant-field) scaling
  - basic characteristics preserved
  - good results for medium feature sizes
  - not accurate, but adequate as a guide
- chip size increasing at same time

Device Scaling

- scaling factor α applied to
  - dimensions
  - voltages
  - concentration densities

Kung, page 14, Figure 1.6b

- area for device/wire $A \rightarrow A/\alpha^2$
- for given chip size, number of devices increases by α^2
- switching time decreases by α
- voltage scaling improves performance, hurts noise margins
- oxide thicknesses reduced → yield problems
- current density increases → need wider conductors
- power density stays the same (actually gets worse with real scaling)

Conductor Scaling

- scaling factor α applied to dimensions, including dielectric
- resistance increases by α
- current density increases by α
- RC time constant remains the same

Kung, page 14, Figure 1.6a

Interconnection and I/O Constraints

- interconnect delays dominate switching delays
- stuffing effect: interconnect lengths do not scale with α
- model for maximum interconnect length L_{max} is

$$L_{max} = \frac{1}{2} A^{1/2}$$

- A is chip area
- situation worse if chip size increased

- Rent's rule: number of I/O pins

$$M = N^{2/3}$$

- N is number of devices
- example: 10^6 gates $\rightarrow$ 2000 pins,
  10 mm by 10 mm chip $\rightarrow$ pad every 20 μm
- other problems
  - clock distribution

Desirable Qualities

- local communication
- regularity
- modularity
- globally asynchronous
- locally synchronous

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DENSE PACKAGING

Package Mounting

- traditional approaches
  - through-hole
  - surface mount
- alternate approaches
  - die attachment: wire bonding, TAB, flip-chip
  - direct die mounting: insulated substrate, MCM, hybrids, WSI
- goal: higher performance through better density, reduced delays

Wire Bonding

- back of die glued to lead frame (with good thermal conductor)
- wire bond machine attaches wires between chip pads and lead frame
- wires usually aluminum (no sag), pitch 0.16-0.3 mm

Bakoglu, Page 96, Figure 3.13

- bonding difficult for high I/O density
- interconnect performance evaluation difficult
- inductance large (approximately 5 nH)

Tape Automated Bonding (TAB)

- metal film leads deposited on polymer tape
- chip attached to film and leads
- automation easy, fast

Bakoglu, Page 97, Figure 3.14

- attachment
  - solder bumps placed on die
  - align with copper leads in multilayer tape
  - solder reflow bumps to form bond

Bakoglu, Page 98, Figure 3.15a

- allows close lead spacing (monolithic structure), pitch 0.08 to 0.12 mm
- inductance, capacitance minimal, controlled
- TAB frame expensive - high volume, or standard frame for ASICs
- can mount TAB unit on board or in chip carrier
- thermal mismatch effects troublesome

- alternate attachment - area TAB
  - solder bumps distributed across entire chip surface
  - multilayer tape
  - supports larger number of I/O terminals (exceeding 500 per chip)

Bakoglu, Page 98, Figure 3.15b

Flip-Chip Mounting

- place solder bumps on die
- invert and align to contacts on substrate
- reflow solder to bond
- minimal inductance (< 1 nH), capacitance (< 1 pF)
- use terminals distributed around entire chip area
- thermal problems
  - chip not glued to package, mismatch causes strain
  - thermal path through solder balls
  - use backside?
- inspection difficult

Direct Die Mounting

- eliminate level of hierarchy
- wire bonding, TAB, flip-chips with solder bumps

Insulated Metal Substrate

- aluminum substrate, 10-30 μm of insulating resin
- etch ground vias, deposit and pattern copper
- wire bond chips

Bakoglu, Page 100, Figure 3.16

- low cost
- substrate serves as heat sink, ground plane
- no thermal mismatch
- good for medium densities, wire bonding and single layer limit density
- flip-chip, TAB alternatives

Ceramic Multichip Carriers

- mount dice on ceramic substrate via solder bumps
- multilayer substrate, dense interconnection network
- minimal chip-to-chip spacing
- minimal capacitance, inductance, discontinuities
- can be used in conjunction with advanced cooling systems

Silicon-on-Silicon Hybrid

- silicon substrate as interconnection medium
- thin film interconnections on wafer
- attach separately processed and tested dice
- use wire bonding, TAB, or solder bumps
- different technologies on same substrate
- active devices in substrate

- substrate has one or two aluminum or copper layers (copper preferred)
- polyimide or SiO_2 interlayer dielectric (polyimide preferred)

Bakoglu, Page 107, Figure 3.23

Silicon-in-Silicon Hybrid

- mount dice through substrate
- deposit and pattern first layer metal
- etch holes, mount and secure dice (alignment critical)
- spin on polyimide, deposit and pattern second layer metal

Bakoglu, Page 108, Figure 3.24

MCM Advantages

- lower signal delays, higher density
- matched expansion, assuming low temperature differential
- well suited for cooling structures
- uses IC processing techniques

Bakoglu, Page 109, Table 3.4

Wafer Scale Integration (WSI)

- "chips" on wafer interconnected by global routing
- high performance
  - low signal delays
  - wider paths
  - higher densities
- yield problems
- redundancy
- expensive, not currently commercially viable

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THERMAL EFFECTS

Introduction

- performance
  - semiconductor switching speeds degrade with temperature
  - can result in system failure
- reliability
  - failure mechanisms enhanced
  - electromigration
  - oxide breakdown
  - hot-electron injection effects
  - leakage currents increase
  - corrosion mechanisms accelerate
  - mechanical stresses worsen - expansion

Power Dissipation Requirements

- CMOS gate (inverter) as an example
- components
  - static, due to leakage current
  - dynamic, due to switching, capacitance charge/discharge
- total power sum of dynamic and static

Static Power Dissipation

- devices off $\rightarrow$ no contribution from channel conduction
- diode formation from diffusions $\rightarrow$ leakage
- leakage current

$$i_o = i_s(e^{qV/kT} - 1)$$

- i_s is reverse saturation current
- V is voltage across diode
- k is Boltzman's constant, q is electron charge
- T is junction temperature

- total static power

$$P_s = \sum_{j=1}^{N} i_j V_{dd}$$

- N is number of gates
- i_j is leakage current of gate j
- typical inverter, V_{dd} = 5V, P_s = 1 to 2 nW

Dynamic Power Dissipation

- "short circuit" current (V_{dd} to ground)
- load capacitance charge/discharge
- power, clock period t_c

$$P_d = \frac{1}{t_c}\int_0^{t_c/2} i_n(t)V_o dt + \frac{1}{t_c}\int_{t_c/2}^{t_c} i_p(t)(V_{dd} - V_o)dt$$

- assume step input, capacitive load

$$P_d = \frac{C_L V_{dd}^2}{t_c} = C_L V_{dd}^2 f_c$$

- total dynamic power is sum of gate dynamic power dissipation
- typical inverter, V_{dd} = 5 V, f_c = 10 MHz, C_L = 100 fF, P_d = 25 μW
- dynamic power dominates

Power Dissipation Examples

- output buffers, $P = \frac{1}{4} C V^2 f$
- CMOS, 50 MHz, 3.4 V, 100 output buffers @ 70 pF → 1 W
- ECL gate @ 10 mW → 10k gate chips dissipates 10 W

Prasad, Page 180, Figure 5.5

Heat Transfer

- conduction
- convection
- radiation

Convection

- conduction of heat in moving fluid

Radiation

- bound on radiated power

$$P \leq \sigma_{rad} T_j^4$$

- for T_j = 120° C, P $\leq$ 0.14 W/cm^2
- too small for IC dissipation requirements

Conduction

- heat flux

$$J_Q = -\kappa \nabla T$$

- κ is thermal conductivity, ∇T is thermal gradient
- assume one dimensional, linear gradient

$$\theta = \frac{T_j - T_a}{P}$$

- T_j is junction temperature, T_a is ambient temperature, P is power
- low thermal resistance gives lower junction temperature for given power

Materials

- metals better than nonmetals, gases poor

Bakoglu, Page 114, Figure 3.5

- solids
  - metals: conduction by electrons, light, fast, long mean free path $\rightarrow$ good conductors
  - dielectrics: conduction by phonons, slower, similar mean free path $\rightarrow$ slightly poorer conductors
- liquids, gases
  - weak coupling between molecules $\rightarrow$ poor conductors
  - circulate to improve heat removal

Package Thermal Properties

- need to control junction to ambient thermal resistance
- change lead frames to lower resistance materials
- heat sinks
- heat spreaders

Bakoglu, Page 116, Figure 3.26

Plastic Packages

- DIP (40 pins)
  - 38° C/W for natural convection
  - 25° C/W for forced air convection
  - 2 W or 3 W power dissipation for $\Delta T \leq 25°$
  - higher resistances for fewer pins, 68° C/W for 20 pins
- PLCC
  - 72° C/W for 20 pins
  - 38° C/W for 52 pins
  - 32° C/W for 84 pins

Ceramic Packages

- mounting important
  - heat flow through back side of chip
  - through die bond

Bakoglu, Page 117, Figure 3.27

- LCCC (68 pins)

Bakoglu, Page 118, Figure 3.28

- PGA with heat sink
  - heat flow through back side of chip
  - through die bond, substrate, heat sink

Bakoglu, Page 118, Figure 3.29

- PGA thermal conductivities

Bakoglu, Page 119, Figure 3.30

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CONCLUSION

- require high performance packaging
- packaging for high speeds
- thermal management becomes significant