# HIGH FREQUENCY PRINTED CIRCUIT BOARD DESIGN

## SURFACE MOUNT DEVICES

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# INTRODUCTION AND OVERVIEW

# Why Surface Mount?

- Limits of Conventional Technology
  - based on through-holes
  - weight
  - volume
  - cost
- Surface Mount Features
  - denser
  - lighter
  - more reliable
  - reduced parasitics, lower noise, less interference
  - easier to automate
  - faster
  - cheaper

- Denser

Prasad, Page 12, Figure 1.9

- Density Varies with Package Type

Prasad, Page 89, Figure 3.13

- Lighter

Prasad, Page 11, Figure 1.8

- Reduced Parasitics

Prasad, Page 17, Table 1.1

- Faster

Prasad, Page 17, Figure 1.14

- Comparison

TI, Page 1-4, Table 1-1

# Definitions

- Through-hole Mounting

TI, Page 1-2, Figure 1-1a

- Surface Mount
  - any mounting technique not using through-holes
  - SMT, SMD
  - several types of chip carriers for active devices
  - passive devices also available

TI, Page 1-2, Figure 1-1b

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# SURFACE MOUNTING: THE SHORT STORY

# Surface Mount Component Preparation

- often plated for soldering, or pre-tinned
- neeed to tin to get better joint (if necessary)
- also adds (small) amount of extra board/package clearance

TI, Page 1-6, Figure 1-4a,b

# Printed Circuit Board Preparation

- footprint for component
- pre-tin pads

TI, Page 1-6, Figure 1-4c

# Solder Paste Application

- extra solder to form joint fillets
- paste screen printed on board

TI, Page 1-6, Figure 1-4d

# Component Placement

- component placed on board pads

TI, Page 1-6, Figure 1-4e

# Soldering

- melts solder and forms bond

TI, Page 1-6, Figure 1-4f

# Final Steps

- clean with solvent
- test

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# COMPONENT TYPES

# Dimensions

- standardized
- depend on individual component specifications
- JEDEC (Joint Electronic Devices Engineering Council) and others
- metric or English?!

# Plastic Packages

- circuit mounted on lead frame
- encapsulated with electrically nonconductive plastic
- plastic withstands soldering temperatures

# PLCC, Plastic Leaded Chip Carrier

- "J" leads, bent under package
- leads take up stress (must not touch package body)
- nominal lead pitch is 50 mils (0.050 inches)
- square package specified for 20, 28, 44, 52, 68, 84, 100, 124 terminals

TI, Page 1-7, Figure 1-5

- rectangular package specified for 18, 22, 28, 32 terminals (usually memory)

TI, Page 1-8, Figure 1-6

- thermal resistance similar to DIP

# SOIC, Small Outline IC

- small DIP shape
- 50 mil lead pitch
- gull-wing leads, sensitive to handling
- narrow (150 mil) or wide (300 mil) packages
- available in 8, 14, 16, 20, 24, 28 lead versions

TI, Page 1-10, Table 1-9

- thermal resistance poor (high)

# SOJ, Small Outline J Package

- used for high density DRAM
- "J" leads like PLCC, 20 pins
- hybrid of SOIC and PLCC
- space in center for bypass traces

Prasad, Page 99, Figure 3.22

# PQFP

- high terminal density
- small gull wing leads
- handling difficult

Prasad, Page 100, Table 3.23

# LCCC

- primarily for high reliability applications
- bond using solder fillets in cavities
- thermal mismatch problems

TI, Page 1-11, Figures 1-10,11

# Ceramic Leaded Chip Carriers

- high reliability applications
- use leads to address thermal problems
- preleaded or postleaded

Prasad, Page 86, Figure 3.12

# Discrete Semiconductors

- variety of sizes, types

TI, Page 4-5, Figure 4-5

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# HISTORY AND OTHER TOPICS

# Roots of Surface Mount

- flat packs
- hybrids
- not directly applicable to SMT

## Early Packaging

- point-to-point wiring
- no substrate

## Early Semiconductors

- radial leads
- through-holes
- single sided boards (from resistor, capacitor technology)

# Dual In-line Package (DIP)

- invented by Fairchild
- two rows of leads
- allowed wave soldering

# Flat Packs

- 1950s "surface mount" technology
- high reliability military applications
- mounted close to board surface
- required gold plated leads (two sides of package)
- required discrete soldering
- very costly

# Hybrid Technology

- became popular in 1960s, still used
- SMD soldered inside through-hole or SM package
- usually ceramic substrate, sometimes plastic
- passive components for SMT derived from hybrid technology
- placement, soldering techniques for SMT derived from hybrid technology

Prasad, Page 4, Figure 1.1

## Leadless Ceramic Chip Carriers

- developed in 1970s for military
- smaller packages with high pin count
- hermetically sealed
- expensive substrates
- must match coefficients of thermal expansion (CTE) to prevent solder cracking

## Small Outline Integrated Circuit

- developed in 1960s for watch industry
- surface mountable

# Plastic Quad Flat Packs

- developed in 1970s by Japanese for calculators and consumer electronics
- surface mount
- leads on four sides ("quad")
- gull-wing leads; fragile
- high density

# Surface Mount Passive Components

- wave soldered
- small

Prasad, Page 6, Figure 1.2

# Plastic Leaded Chip Carriers

- leads on four sides, bent down and under ("J")
- more robust to handling damage
- addresses CTE problems
- good for medium to high pin densities

# Worldwide IC Package Consumption

- mix of surface mount types increasingly used
- through-hole mounting down

Hwang, Page 8, Figure 1.5

# Passive Surface Mount Use

- surface mount beginning to dominate

Hwang, Page 8, Table 1.1

# Growth of Surface Mount

Hwang, Page 12, Figure 1.10

# Surface Mount by Market Sector

Hwang, Page 13, Figure 1.11

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# MOUNTING PROCESS

# Component and Board Preparation - Pre-tinning

- need good solderability
- most leaded, passive components pre-tinned
- many leadless components not pre-tinned
- process
  - preheat
  - dip in molten solder at 250° C
  - cool
  - clean with flux cleaner
- utility
  - inspection for wetting prior to assembly
  - increases joint strength
  - elevates carrier slightly
  - removes gold from LCCC pads

# Component and Board Preparation - Board Cleaning

- relatively clean boards
  - light degreasing solution
  - 1,1,1 trichlorethane
- normal oxidation or contaminants
  - non-diluted organic acid flux
  - 15 second dip
- heavy oxidation
  - increase dip time to 30 seconds
- rinse with deionized water, dry with compressed nitrogen

- severe contamination or oxidation
  - use ferric chloride solution
  - dip for 10-15 seconds (until traces "cinnamon pink")
  - etches away copper material
  - board destroyed if dip too long

# Solder Paste

- apply using screening process
- holds components in place until solder reflows
- composed of solder alloy particles suspended in flux binder
- flux binder keeps solder uniformly dispersed throughout paste, typically 60% rosin and 40% others (solvents, thickeners, etc.)
- pre-mixed past with 85-90% metal by weight recommended, but components available separately (careful mixing/handling necessary)
- excess oxide content leads to solder balls
  - only open containers when ready to use
  - often refrigerate or store in nitrogen gas (if refrigerated, warm before opening to avoid condensation)
- separation problems solved by stirring
- minor drying can be overcome by adding solvent

# Solder Paste Application

- screen printing commonly used
- allows paste to pass through at desired points (similar to stencil)
- process
  - make screen
  - align board below screen
  - push squeegee across screen to force paste through

Prasad, page 334, Figure 9.12

# Screen Printing

- screen
  - consists of frame, mesh, emulsion
- frame holds mesh, allows mounting
- mesh
  - usually nylon, polyester, or stainless steel
  - filaments mounted 45° to frame allowing resolution of small objects on Manhattan grid
  - mesh count (openings/inch) about 60 to 150
  - rule of thumb is mean particle size no larger than one third the mesh opening

- emulsion
  - provides pattern for footprints
  - polyvinyl alcohol, polyvinyl acetate, among others
  - expose to UV to cure, except where openings will be (use protective film)
  - rinse off uncured emulsion to form openings
- emulsion thickness and open area in mesh affect paste thickness, need to be properly controlled
- snap off distance controls feature resolution
- screens should be cleaned after each use, for example ultrasonic with Chlorethyl Nu

- squeegee
  - squeegee hardness, angle of attack vary
  - must be cleaned after each use, replace occasionally
- metal stencils sometimes used instead of emulsion, require different pastes

Prasad, page 341, Table 9.5

# Mounting Components

- immediately after past application
- hand placement (low volume)
- automatic pick and place

Traister, page 4, Figure 1-3

- oven bake to evaporate some moisture contents
  - $50 - 80^\circ$ C for 45 minutes
  - minimizes flux and solder bubbling during soldering
- solder surface tension during soldering helps align parts

# Reflow Soldering

- primary surface mount method
- wave soldering occasionally used
- concept
  - pass PCB/component assembly through region of vaporized inert fluorocarbon
  - vaporized fluorocarbon condenses on assembly
  - latent heat from phase change heats board, components, solder paste
  - paste melts, forms bond

- single layer vapor system
  - continuous flow process
  - preheat assembly to 100° C for thermal shock reduction
  - pass through vapor
  - cool

TI, page 2-12, Figure 2-9

- two layer vapor system
  - top layer: secondary vapor layer
    - superheaded Freon TF
    - prevents loss of lower layer
    - preheats, cools assembly
  - lower layer: primary vapor layer
    - vaporized fluorocarbon condenses on assembly
    - melts solder paste to form bond
  - heat transfer to assembly rapid, uniform
    - exposure time short
    - minimizes component degradation, solder bridges

TI, page 2-14, Figure 2-11

- belt reflow system
  - assembly carried across hot plates by belt
  - poor temperature control
  - less flexible
- wave soldering
  - two waves
  - first wets joints - turbulent
  - second removes excess solder - smooth

# Cleaning

- remove flux residues
- minimize time between reflow, cleaning
- similar to through-hole procedures (vapor degreaser)

# Automation

TI, page 2-15, Figure 2-13

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# MIXED COMPONENT MOUNTING

# Sockets

- through-hole technology
  - cheaper fabrication
  - frequently already in place
  - many components not available in SMT
- use of sockets
  - sometimes chips SMT only
  - adapt surface mount device to through-hole board using socket
  - available for PLCC, LCCC packages
  - sometimes cheapest, easiest, but not pleasing
- the other direction (DIP on SMT)

# Types of Surface Mounting

- Type I
  - surface mount only
  - single or double sided

Prasad, page 8, Figure 1.4 I

- process

Prasad, page 10, Figure 1.6

- Type III
  - primarily through-hole mounts
  - passive surface mount devices on bottom

Prasad, page 8, Figure 1.4 III

- process

Prasad, page 9, Figure 1.5

- Type II
  - surface and through-hole components on top side
  - passive surface mount components on bottom side

Prasad, page 8, Figure 1.4 II

- process (complex)

Prasad, page 11, Figure 1.7

# Wave Soldering

- surface mount devices glued to board
- preheat, use fast conveyor speeds to avoid degradation (3-4 seconds or less)
- relatively low temperatures

TI, page 3-1, Figure 3-1

- shadowing

Traister, page 8,9, Figure 1-5,6

- orientation

Traister, page 9, Figure 1-7

- bridging

Traister, page 10, Figure 1-9

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# DESIGN AND LAYOUT GUIDELINES

# Board Structure

- panel size
  - several boards per panel
  - reduces handling
- conductor distribution
  - flatness important for surface mount
  - copper planes equidistant from neutral axis to reduce bimetallic action induced bowing
  - alternate fiber direction between conductor layers to reduce bowing
  - thermal lands often needed below chips to dissipate heat

- panel layout
  - sufficient edge handling area
  - SMT requires optical targets
    - orient artwork
    - orient component lands
    - three fiducial points at corners usually used

# Component Considerations

- substrate population
  - placement machine restrictions - lanes or zones
  - ease of manufacturing
  - space between SMC and cliched leads of THC should be 20-40 mils
- component spacing
  - the more the better for manufacturing, worse for system
  - component pitch governed by component width, spacing
  - width includes rotational accuracy of placement
  - spacing controlled by solder bridging limitations

- substrate orientation
  - align orientation of similar components for ease of manufacturing
    - no rotation needed
    - ease of manufacturing
  - critical for wave soldering
    - passive components parallel to each other
    - SOICs parallel to each other
    - longer axes of SOICs and passive components perpendicular to each other
    - long axes of passive components perpendicular to direction of travel of board
- less critical for other soldering methods

# Board Features

- smaller features than through-hole boards
- more vias than through-hole boards
- conductor routing
  - conductors connecting to land areas act as solder thieves (draw solder from lands)
    - narrow conductor entering land area
    - route conductors into land areas "necked down"
    - use solder mask over lines

Traister, Page 220, Figure 6-9

- vias within lands
  - size governed by board thickness versus hole diameter
  - normally plated through-holes, 25-40 mils in diameter
  - locate away from lands to avoid solder migration
  - use "necked down" layout or solder mask to avoid solder migration
  - tented or filled vias reduces migration
  - vias within lands desirable for wave soldering
- vias under components
  - can place vias under SMC
  - may aid cleaning
  - use tented or filled vias for wave soldering to prevent flux trapping
- vias as test points
  - vias used to connect probe points to other board layers
  - may be tented

- conductors and vias, typical clearances

Ginsberg, Page 121, Figure 4.1

Ginsberg, Page 121, Figure 4.2

Ginsberg, Page 122, Figure 4.3

# Land Pattern Considerations

- influences joint strength, reliability
- layout scale - use sufficient resolution (CAD)
- sharing lands
  - don’t do it
  - solder thief
  - component float

- land geometry
  - too long → components float to one side
  - too wide → components rotate

Traister, Page 219, Figure 6-8

- land pattern separation
  - contain solder paste
  - two narrow traces better than single wide trace
  - land to land 50 mils minimum
  - equivalent to 75 mils between leads of PLCCs

Ginsberg, Page 123, Figure 4.4

- conductors under components
  - no problem with narrow conductors
  - wide conductors can be solder thieves, cause component lift
- adhesive control
  - too much leads to land coverage
  - dummy land used to improve height control
- solder mask clearances
  - 10-15 mils between edge and conductor

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# INSPECTION, TESTING, AND REPAIR

# Inspection

- small → magnification
- density, packaging → most of joint obscured
- solder paste application
  - too much → bridging
  - too little → poor joints
  - visual inspection slow
  - pattern recognition
    - camera generates image
    - image compared to "good" pattern

- solder joints
  - solder balls, dewetting, missing solder relatively easy to detect
  - bridging difficult to detect, often under component
  - too much solder impedes inspection
  - voids affect conductivity, mechanical strength
    - detect by observing pinholes
    - reject if found

- visual inspection
  - microscope, perhaps with camera and display
  - limitations
    * operator fatigue
    * operator judgement
    * view

- X-ray inspection
  - detect hidden flaws
  - expensive equipment
  - low throughput
- laser inspection
  - laser heats joints
  - infrared detector senses radiation from joint
  - results compared to "good" pattern
  - detects cracks, pinholes, voids
  - fast, totally automated

# Testing

- pre-assembly conductor tests
  - tester with spring-loaded pins
  - make contact to pads
  - continuity, isolation, resistance
  - must be aligned for each design
- solderability tests

- post-assembly tests
  - identical to through-hole testing
  - automatic test equipment (ATE) essential
  - bed-of-nails tester adjusted for smaller grid

# Repair

- remove faulty component
- mount new component
- heated collet
  - load PLCC into collet
  - apply solder paste to PLCC footprint
  - align PLCC over footprint, make contact with PCB
  - center pin holds PLCC down
  - collet heated to reflow solder
  - collet lifted, pin holds PLCC down
  - removal similar
  - closely spaced devices difficult to handle

- heated probes
  - similar to collet
  - scissor handles
  - contacts leads on all sides
  - probes heated like soldering iron
  - closely spaced devices difficult to handle

- hot air repair terminal
  - hot air directed onto SMC connections
  - devices removed when solder reflows
  - care must be taken to avoid damage to footprint pads
  - good for closely spaced devices
- other approaches possible
  - superheated, clean gases used instead of air for reflow
  - infrared heater

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# RELIABILITY AND YIELD

# Reliability

- SMT usually more reliable than through-hole mounting
- PCB failures less likely
  - fewer plated through-holes
  - fewer layers needed
  - automation straightforward
  - PLCC temperature cycle and flexure test results good on various board types
  - LCCC temperature cycle test results good for small devices, poor on large (44 pads or more) devices except on stiff boards
- component reliability similar or superior to through-hole versions

# Yield

- problems similar to those in through-hole mounting
- reject mechanisms
  - contaminated PCBs
    - oxidation, grease
    - affects solder bonding to pad
  - solder paste
    - purity, oxides, particle size and shape
  - solder paste screening
    - proper mesh adjustment
  - component placement
    - alignment, rotation
    - automatic pick-and-place
  - soldering
    - solder balls, pinholes, voids, bridges

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# CONCLUSION

- denser
- lighter
- more reliable
- reduced parasitics, lower noise, less interference
- easier to automate
- faster
- cheaper