Design and FPGA Implementation of an Adaptive Demodulator

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Introduction

Field Programmable Gate Arrays (FPGAs) -

- *Re-configurability* - ideally suited for adaptive applications. Circuits can be loaded and deleted as required.
- *Parallelism* - required for high throughput computation involved with real time processing of signals.

Adaptive Signal Processing Systems -

- will need to operate in rapidly changing environments.
- require re-programmable hardware to implement adaptive algorithms.

The Idea Exploit *re-configurability* and *parallelism* offered by FPGAs to build adaptive signal processing systems.

Presentation Overview

- Motivation
- Automatic Modulation Recognition (AMR)
  - Need for AMR
  - Existing strategies
  - Novel algorithm of AMR
- Design Flow for FPGA Synthesis
- Design and FPGA Implementation of PSK and FSK demodulators
- Reconfigurable Platform
  - WILDFORCE
  - Adaptive Demodulation
- Testing and Results
- Conclusions and Future work

Motivation

- To suitably adapt to changing requirements, control strategies targeted at selecting and tuning of signal processing algorithms need to be developed.
- Changing requirements are identified as, to be able to support processing of communication signal of different typologies that emit from different sources.
- Universal receivers do exist that can switch between resident demodulators based on the input from the modulation recognizer.
- The proposed approach is to dynamically reconfigure the same FPGA to perform the necessary demodulation while monitoring for any changes in the input.

Automatic Modulation Recognition

Why do we need AMR ?

- Civilian Applications
  - Signal conformation, interference identification, spectrum management, monitoring non-licensed transmitters.
- Defense Applications
  - Electronic warfare, surveillance, threat detection, threat analysis, warning, target acquisition and jamming.
  - Example: COMINT (Communications Intelligence)
    - A military surveillance system

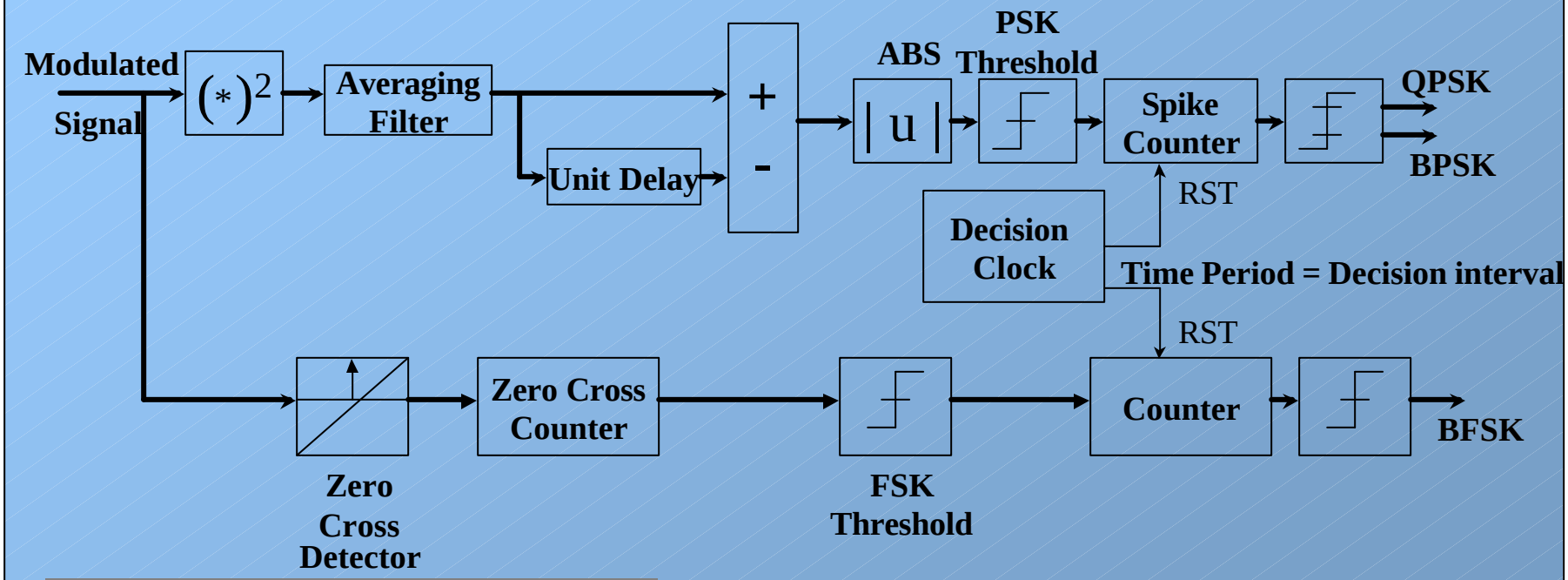
Automatic Modulation Recognition

Existing Strategies -

- Decision theoretic approaches
  - Probability and hypotheses testing are employed
  - Statistical moments, Likelihood functions, auto-regressive spectrum modeling are popular methods.
- Statistical Pattern Recognition
  - Pre-processing of signals
  - Key feature extraction (Instantaneous amplitude, frequency and phase, Spectral processing)
  - Pattern Recognition
    - Training phase
    - Testing phase
  - Artificial Neural Networks

Automatic Modulation Recognition

Novel Algorithm of AMR



Modulations Supported:

PSK - {BPSK, QPSK}

FSK - BFSK

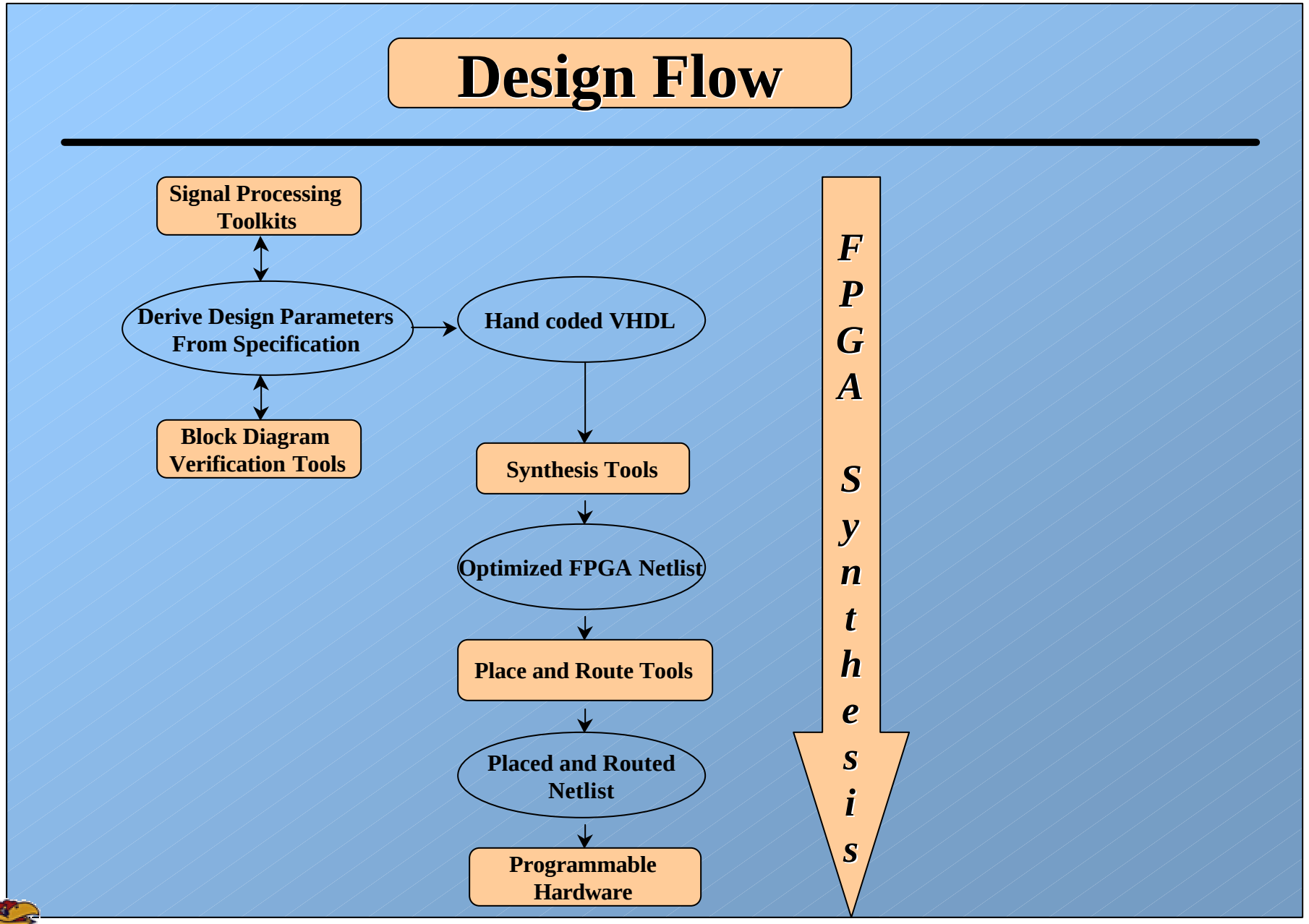
Automatic Modulation Recognition

FPGA Implementation details of AMR

- Specifications
  - Data rate: 100 kbps
  - Carrier: 500 kHz - BPSK, QPSK
    400 kHz - Mark } BFSK
    600 kHz - Space }
- PSK Threshold: 2 mV, for input of 500 mV P-P
- FSK Threshold: 9
- Decision Period: 2048 clock cycles, 8 MHz clock

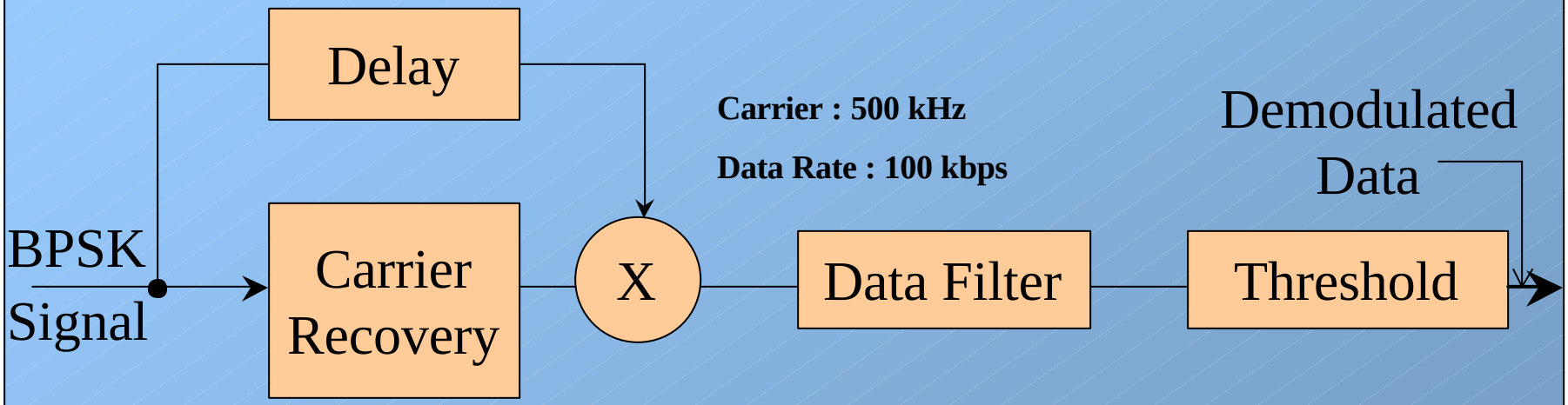
FPGA Implementation Details:

- Parttype : 4085 xla HQ240 -09
- CLB Usage : 588 of 3136 (18%)
- Max. Clock : 26.4 MHz
- Sampling : 8 MHz


Design Flow
Signal Processing Toolkits
Derive Design Parameters From Specification
Block Diagram Verification Tools
Hand coded VHDL
Synthesis Tools
Optimized FPGA Netlist
Place and Route Tools
Placed and Routed Netlist
Programmable Hardware
FPGA Synthesis

BPSK Demodulator

Block Diagram



BPSK Signal

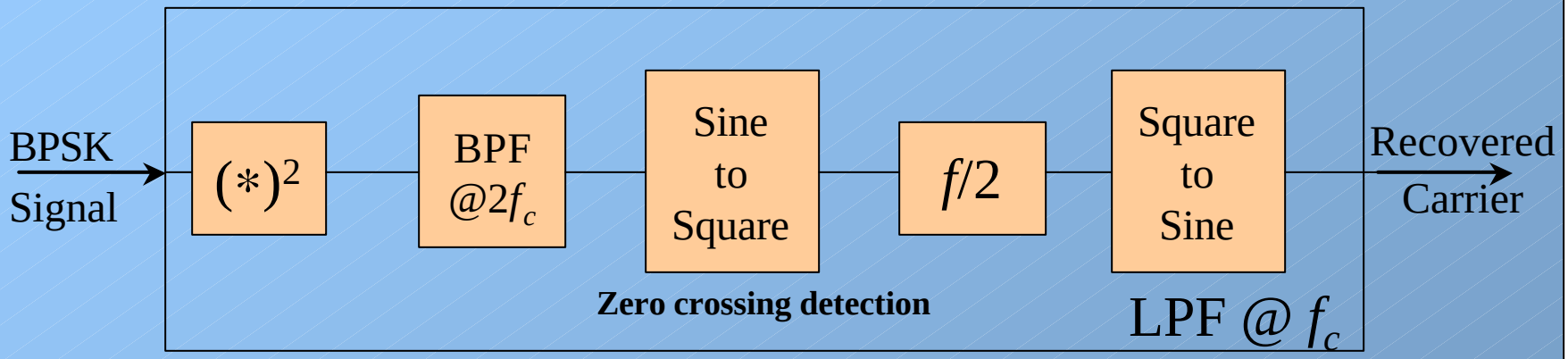
$$s(t)=k*d(t)\cos\left(w_c t+q\right)$$

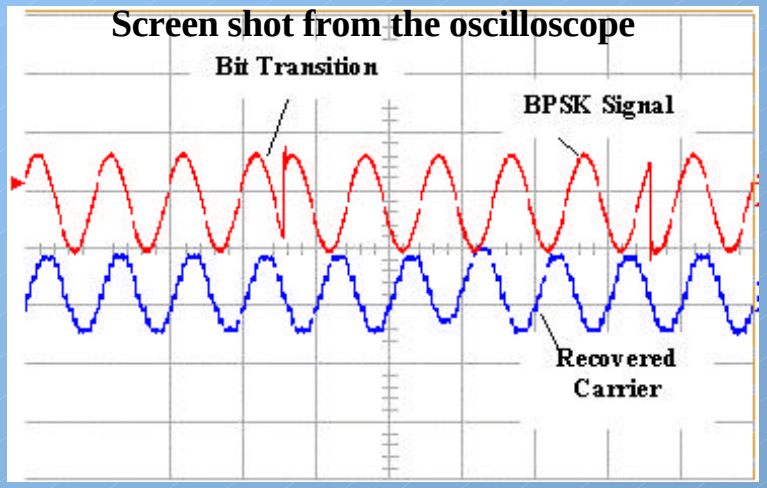
where $d(t)$ ε {-1,1}

k - amplitude and w_c - carrier frequency

BPSK Demodulator

Carrier Recovery





FPGA Implementation Details:

- Parttype : 4025E HQ240 -4 (Xilinx).
- CLB Usage : 530 of 1024 (51%)
- Max. Clock : 10.14 MHz
- Sampling : 8 MHz

BPSK Demodulator

FPGA Implementation details

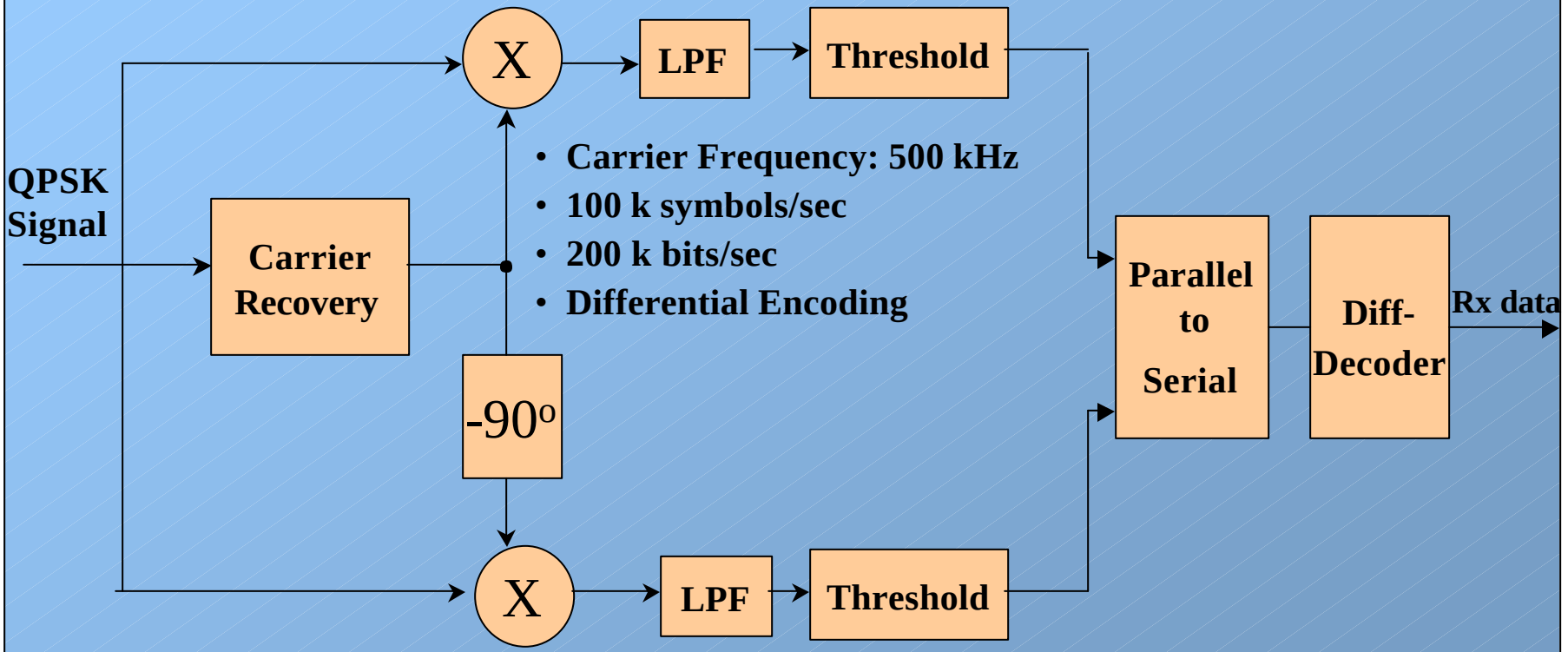
- 72.5 MHz IF signal at the input is sub-sampled using an 8 MHz clock and the image at the 500 kHz is used for rest of the processing. The information content is retained.
- All filters implemented as Finite Impulse Response.
- Multipliers in the filters reduced to Look Up Tables (LUTs).

FPGA Implementation Details:

- Parttype : 4025E HQ240 -4 (Xilinx).
- CLB Usage : 898 of 1024 (87%)
- Max. Clock : 10.07 MHz
- Sampling : 8 MHz

QPSK Demodulator

Block Diagram



QPSK Demodulator

FPGA Implementation Details

- Most of the blocks designed for BPSK re-used.
- Hilbert Transformer used for the 90^{o} phase shift, is implemented as a FIR structure with anti-symmetric coefficients.
- Design is partitioned across three FPGA chips for better timing and performance.

QPSK Demodulator

FPGA Implementation Details

IOFPGA:

Modules: Lower Channel, Parallel-to-Serial, Differential Decoder.

Parttype: 4013 PG223 -5 (Xilinx).

CLB Usage: 538 of 576 (92%).

Max. Clock: 10.06 MHz

FPGA1:

Modules: Carrier Recovery, Hilbert Transformer

Parttype: 4025E HQ240 -4 (Xilinx).

CLB Usage: 835 of 1024 (81%).

Max. Clock: 9.41 MHz

FPGA2:

Modules: Upper Channel.

Parttype: 4025E HQ240 -4 (Xilinx).

CLB Usage: 530 of 1024 (52%).

Max. Clock: 9.34 MHz

Summary:

CLB Usage: 2003 CLBs

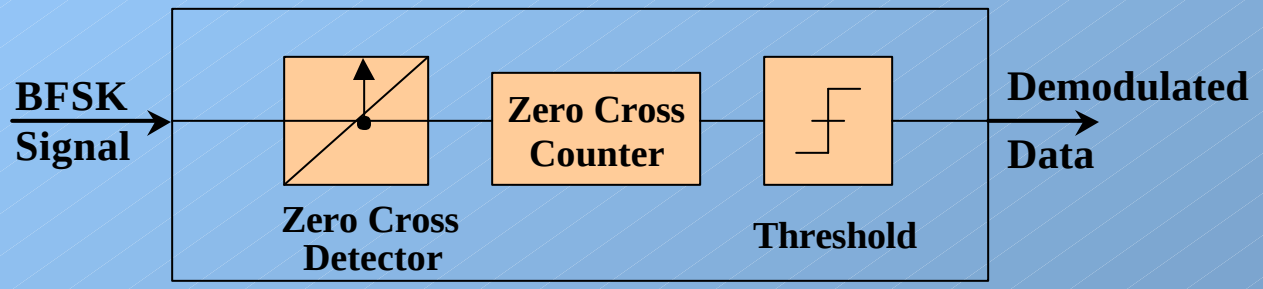
Max. Clock: 9.34 MHz

Sampling: 8 MHz

APTIX MP3A Prototyping board.

BFSK Demodulator

Block Diagram



Specifications:

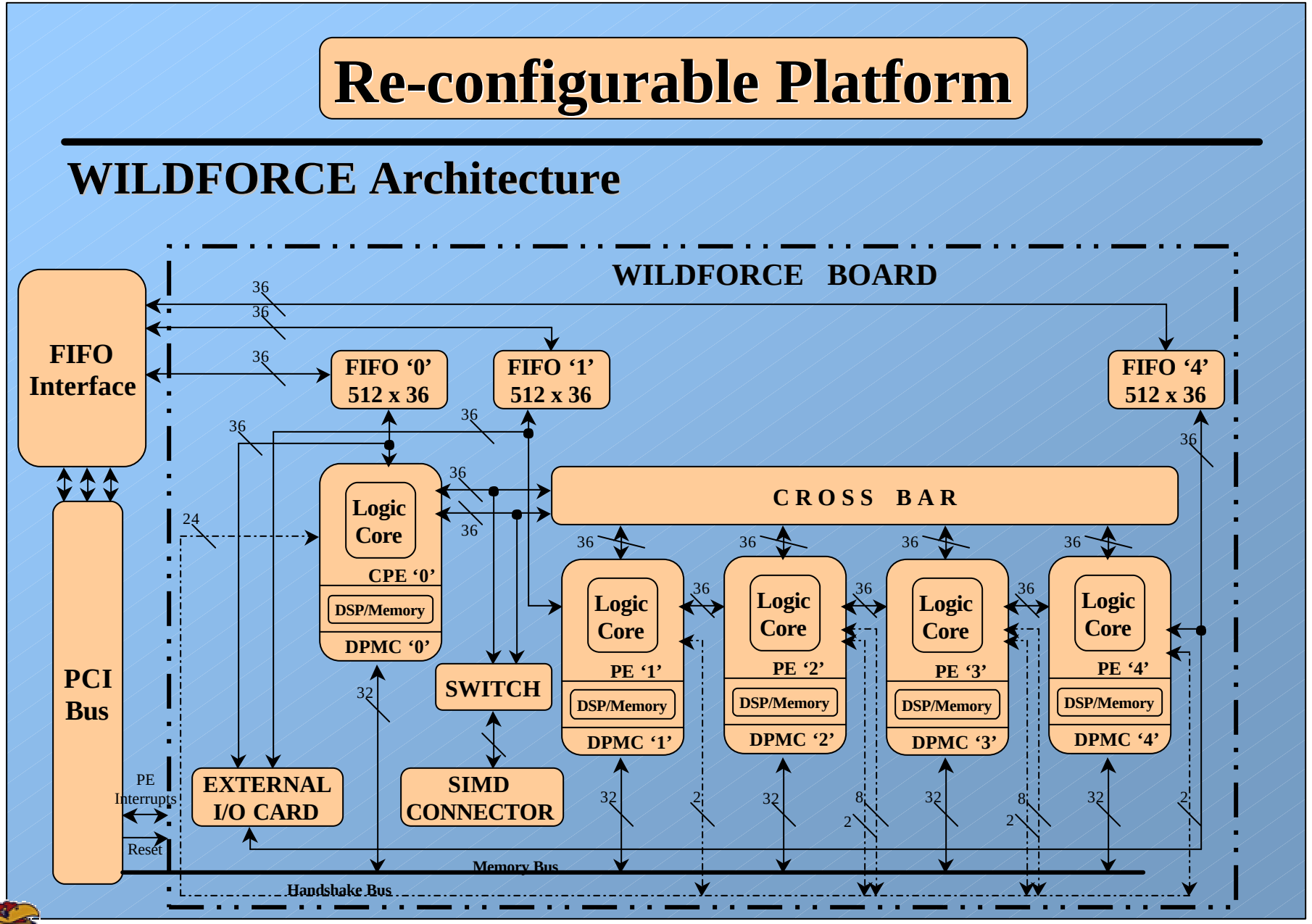
- Data rate: 100 kbps
- Carrier: 400 kHz - Mark
  600 kHz - Space

FPGA Implementation Details:

- Parttype : 4013 PG223 -5 (Xilinx).
- CLB Usage : 4 of 576 (1%)
- Max. Clock : 63.4 MHz
- Sampling : 8 MHz

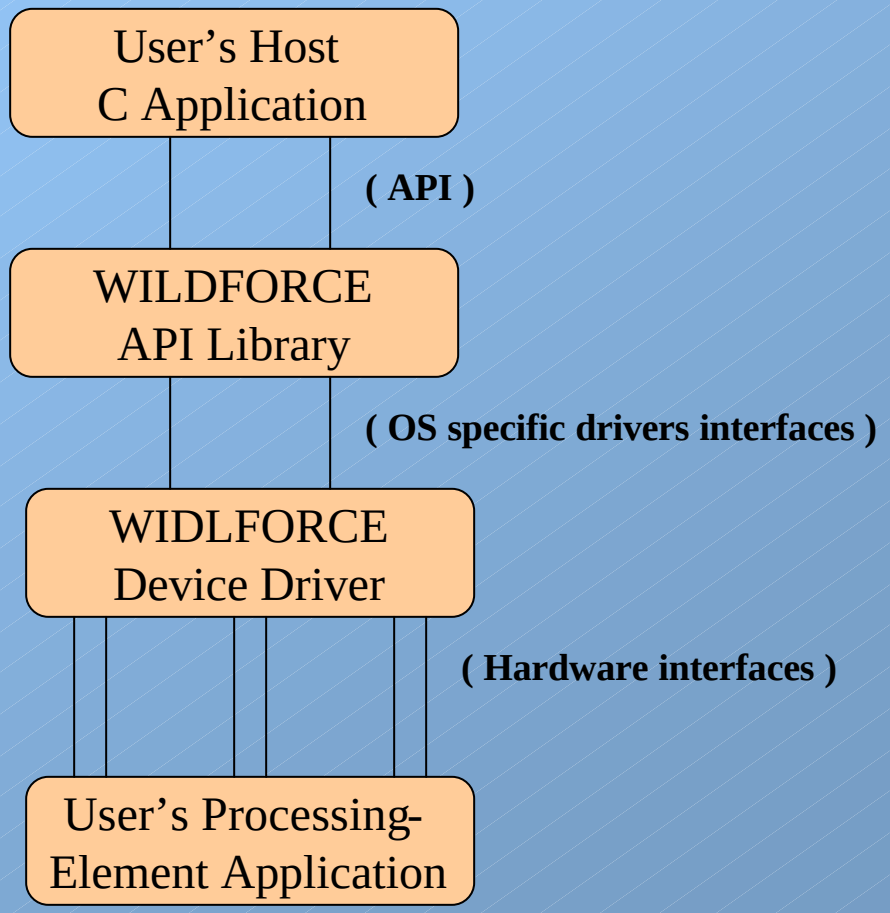
Re-configurable Platform

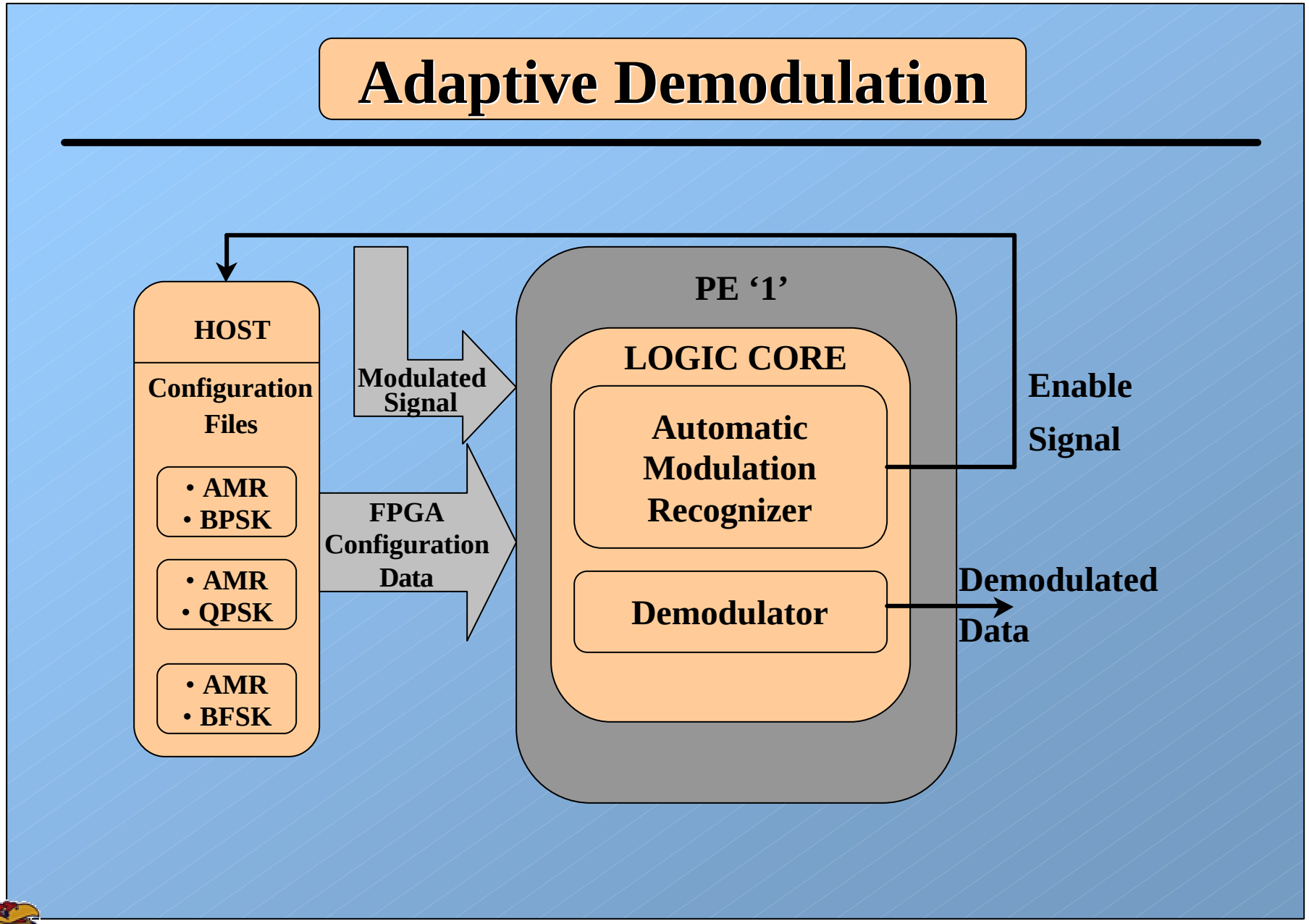
WILDFORCE Architecture



Re-configurable Platform

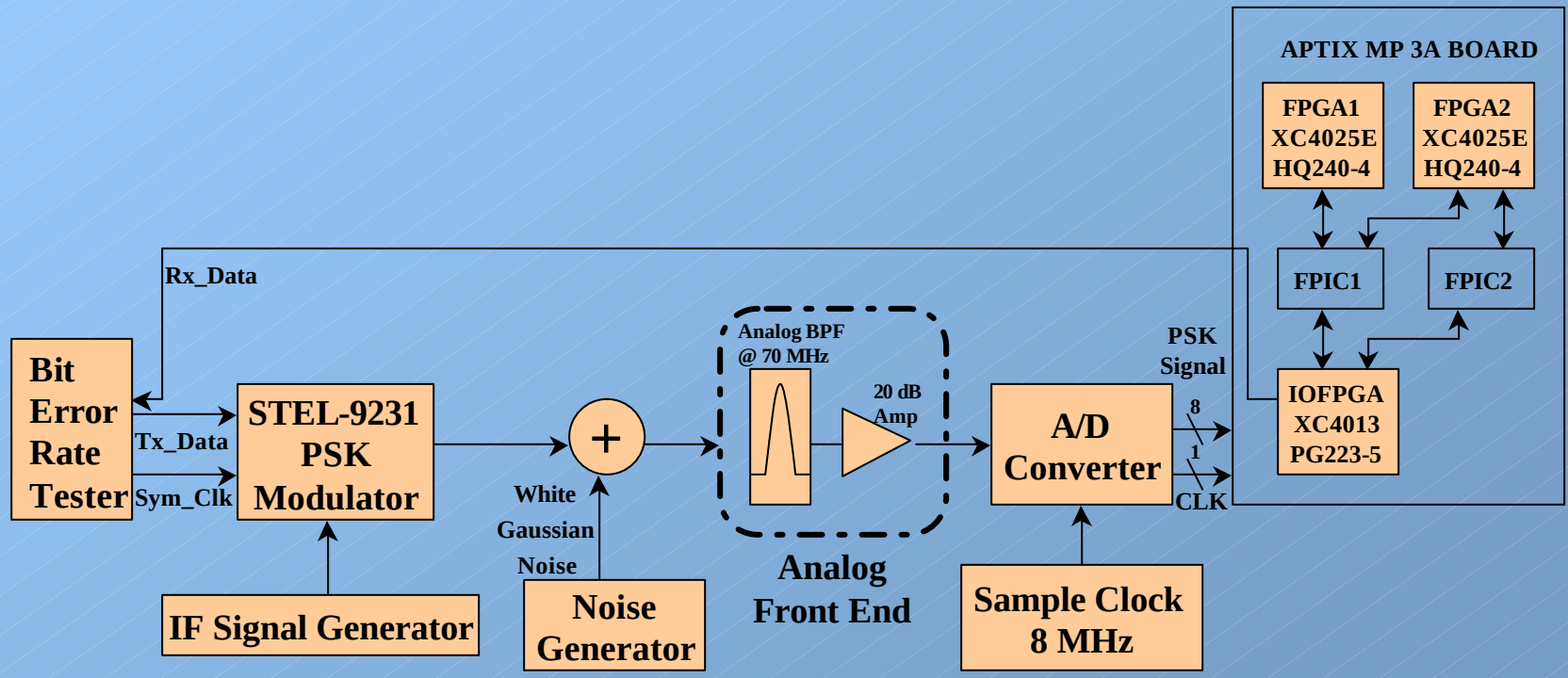
WILDFORCE Software Hierarchy




Adaptive Demodulation
HOST
Configuration Files
• AMR • BPSK
• AMR • QPSK
• AMR • BFSK
Modulated Signal
FPGA Configuration Data
PE '1'
LOGIC CORE
Automatic Modulation Recognizer
Demodulator
Enable Signal
Demodulated Data

Testing

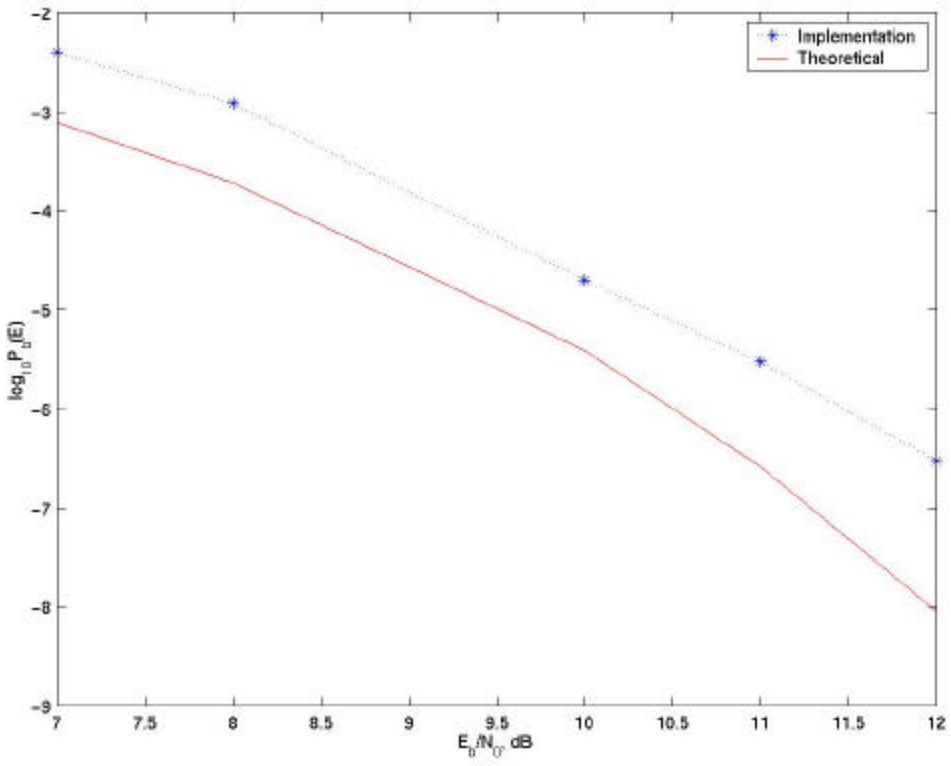
Test Setup for Performance Evaluation of PSK Demodulators



Results

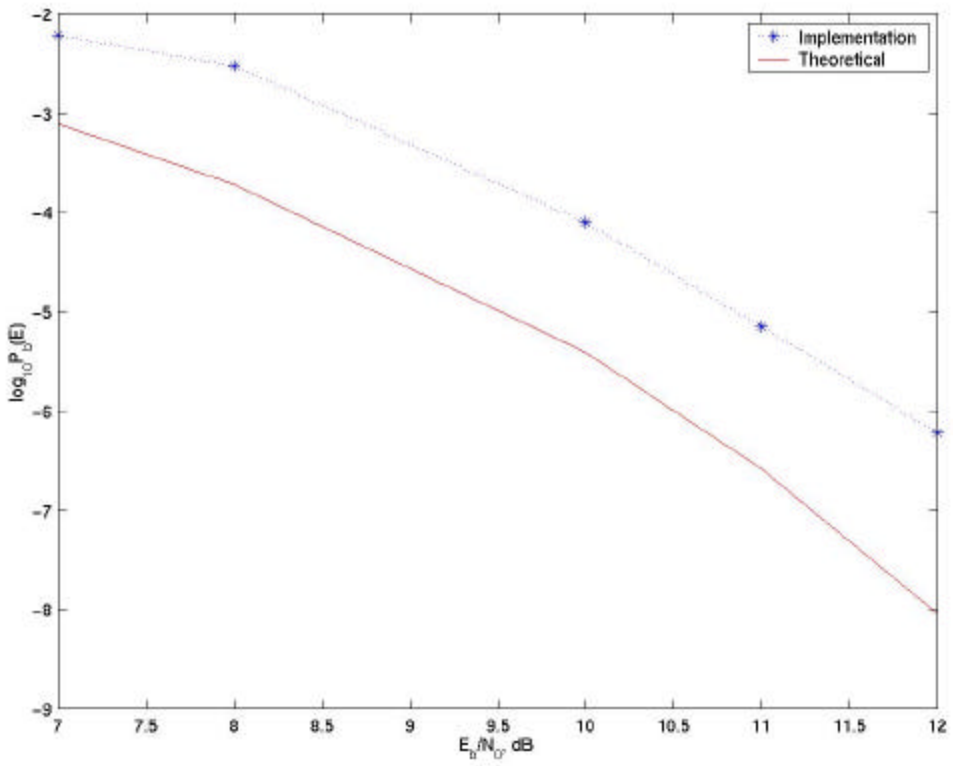
How good are the PSK demodulators ?

E_b/N_0 Vs BER curves for BPSK : Implementation Vs Theoretical



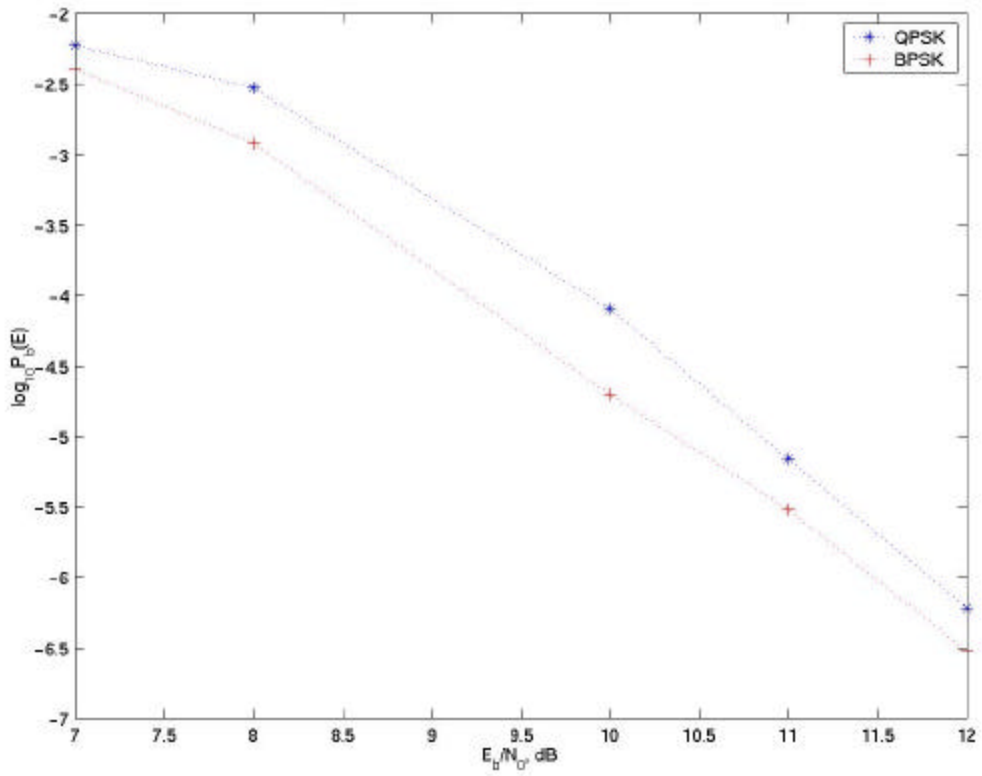
Results

E_b/N_0 Vs BER curves for QPSK : Implementation Vs Theoretical



Results

E_b/N_0 Vs BER curves for PSK : BPSK Vs QPSK



Results

How good is the carrier recovery scheme used ?

- The carrier recovery scheme employed for the BPSK demodulation could tolerate a carrier in the band 450-550 kHz, which is about 100 kHz. This can be attributed to the bandwidth of the bandpass filter in the carrier recovery circuit.
- The QPSK receiver had a tolerance of 50 kHz drift in the carrier frequency centered at 500 kHz.

Results

Noise Tolerance of the AMR algorithm

- The proposed algorithm of AMR was tested to measure its performance in presence of Additive White Gaussian Noise.
- AMR algorithm could tolerate noise levels as low as Signal-to-Noise ratio of 20 dB when all the modulations BPSK, QPSK, and BFSK are present.
- The algorithm could detect the modulation correctly for BFSK with noise levels as low as 5 dB of SNR.
- Noise tolerance for modulations BPSK and QPSK remain at 20 dB. (Depends on how good the filtering is !)

Conclusions

- Proposed and implemented a novel algorithm of automatic modulation recognition for detecting BPSK, QPSK and BFSK.
- Designed and implemented the individual demodulators - BPSK, QPSK and BFSK on FPGAs.
- The AMR algorithm along with the demodulators are integrated into an adaptive demodulator.
- The capabilities offered by the re-configurable platform have been demonstrated which can be a promising choice for a more robust signal processing or communication system.

Future Work

• Extension of the modulation recognition algorithm to accommodate other modulation types.

• Analysis of the effects of signal-to-noise ratio on the thresholds in the AMR algorithm to make them more noise tolerant than 20 dB.

• Exploit the re-configurability of FPGAs to partially reconfigure them, thereby making the demodulators adapt to changing environments. Supporting a wide range of data rates would be a good example in this direction. To support the drift of the carrier frequencies in the spectrum could be another…Many more !!!