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Technical Report

Agile Radio Digital Board Design

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1 Introduction

This document describes the Design of the Agile Radio 3.0 Digital Board. The Digital Board is the base-band signal processing and radio control printed circuit board. It interfaces to a Power board and a RF processing board.

This document is a successor to the Design Document for the Agile Radio 2.0 Digital Board. This Design Document's major difference is that the Cerfcube has been replaced with a PC in a COMeXpress form factor. Other changes that are a consequence of the COMeXpress board are a USB controller for configuring the FPGA and Compact Flash for persistent memory. Additional connectors on the front panel are for VGA video and USB. The two Analog Devices ADCs on the Digital 2.1 board are replaced by a dual ADC from Linear Technologies.

Section 2.0 describes the design of the Digital Board. The restrictions on the design based on design decisions on other parts of the radio are in section 3.0.

Many of the design considerations described in this document are required by the COMexpress Module Base Specification[1].

1.1 Notation

The names of documents are in *italics*.

Digital Signal names are denoted as BLOCK_SIGNAL_TYPE[_ASSERSION][_POSITION] where:

- 'BLOCK' is either the source of the signal or destination of the signal. Examples: CPH, FPGA, ADC, DAC, SRAM1.
- 'SIGNAL' is the base name of the signal. These are often abriviations to reduce the overall length of the name. Examples: ADDR, DATA, RST.
- 'TYPE' is the electrical type of the signal. Examples: LVC=Low voltage TTL, LVC = Low voltage CMOS, T=TTL, C=CMOS.
- 'ASSERSION' L= low voltage assertion, H=high voltage assertion. If this is left off then there is no assertion level for the signal.
- 'POSITION' is a number denoting the position of the signal in a signal bus of the same 'SIGNAL'. 0=LSb.

2 Design

The following is the design for the Digital Board 3.0 of the KU Agile Radio. This includes specification of the devices used for implementation of the subsystems, definitions of the pins interconnecting these devices, and the I2C register programming necessary for specified operation of each device.

This document is divided into sections organized by the subsystems shown in the figure below in the Overview section. The specific device used for implementation of the subsystem is discussed in the corresponding section.

2.1 Overview

The Digital Board is composed of 5 subsystems

1. CPH (Central Processing Host, COMeXpress)
2. DSU (Digital Signal Unit)
3. Memory
4. ADC (Analog to Digital Converter)
5. DAC (Digital to Analog Converter

The CPH provides the interface to the external world through a 100BaseT Ethernet connection. Through this interface data to be transmitted and data received is exchanged with a host or network. Radio parameters can be set and algorithms changed through SSH (Secure Shell) or a web server residing on the CPH. The primary component of the CPH is a Kontron ETXeXpress-PM module. Associated components on the board are the Compact Flash drive, front panel connectors (VGA, Ethernet and dual USB), and the Real Time Clock backup battery.

The DSU performs the bulk of the digital signal processing in the radio. Data to be transmitted is provided to the DSU by the CPH and data received is given to the CPH by the DSU. Base-band complex (I and Q) digital signals are sent to the dual DAC to be transmitted. Received base-band complex digital signals are given to the DSU by the dual ADC. Instructions, tables and parameters for the digital signal processing used by the DSU are held in the Memory subsystem. The primary component of the DSU is a Xilinx Virtex II Pro P30.

The Memory is composed of 4 independent 256K by 36 bit Static Ram chips. Each memory chip is connected to its own bank of the FPGA. Since each chip has independent data and address buses they can be use simultaneously.

The DAC is used to convert the digital signal to be transmitted into an analog base-band signal. The digital signal out of the DSU is a complex signal with 16 bits of I and 16 bits of Q data. The main component of the DAC is an Analog Devices AD9777. This DAC can accept digital data at 160 MSPS. The output of the DAC is a differential current driven complex base-band analog signal that is sent to the RF board through MMCX connectors.

The ADC is used to convert the received analog base-band differential complex signal into a digital signal. The dual ADC converts the analog I and Q channels to digital I channel and Q channels. The ADC component is a Linear Technology LTC2284. This ADC has 14 bit resolution so the 2 LSBs of the 16bit inputs of the FPGA are zero padded to create 16 bit data for each channel. This ADC can sample at 105MSPS.

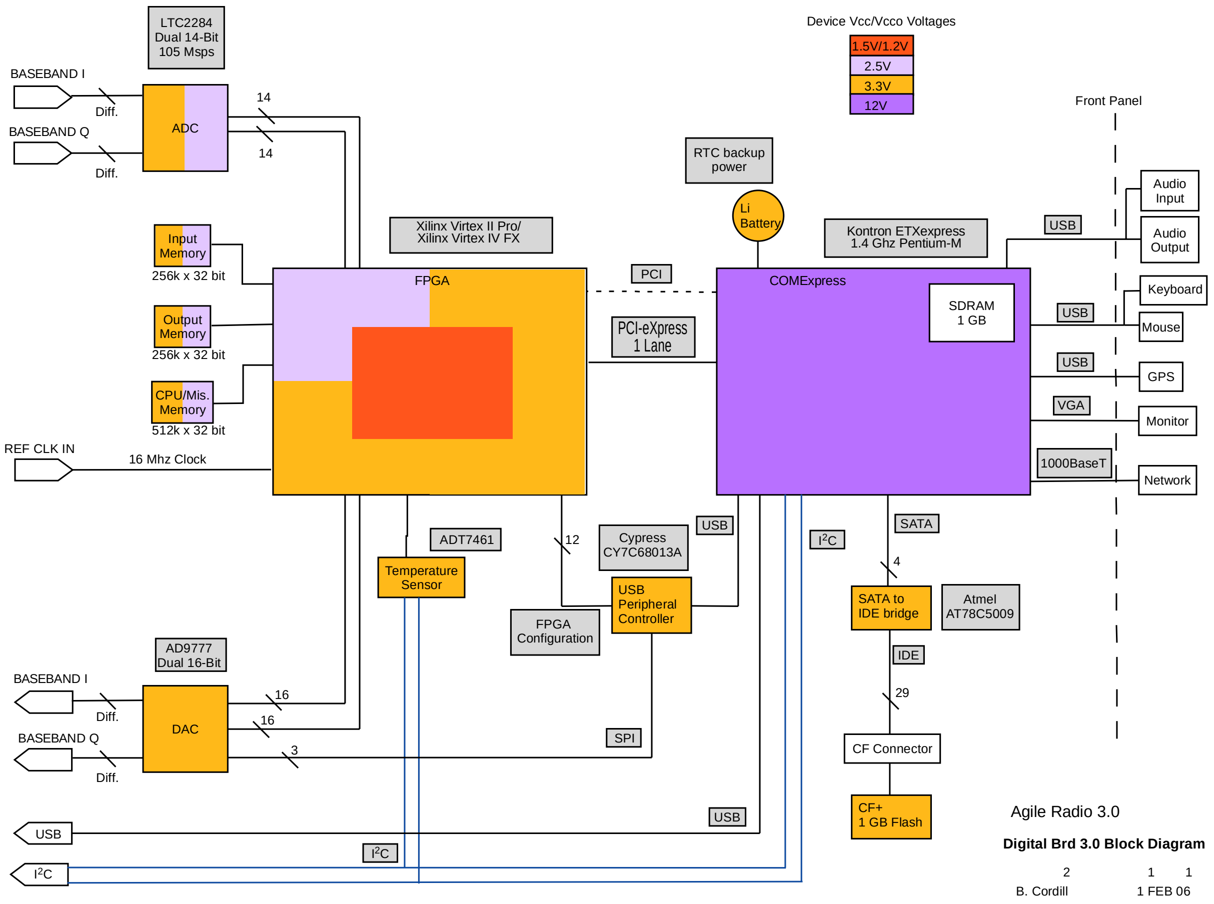


Figure 1 Digital Board Block Diagram.

2.2 Central Processing Host (CPH)

2.2.1 Introduction

The Central and Processing Host (CPH) is the control processor for the Agile Radio. It has interfaces to the outside world over Ethernet and USB, to the DSU over a PCI parallel data bus, a serial PCIexpress bus and a USB High Speed bus. The CPH has an I2C bus to control the other two in the Agile Radio.

The CPU board of the CPH is a Kontron ETXexpress. The CPU is a Pentium M 1.4GHz. The ETXepress had a SODIMM slot for DDR2 memory. For interfacing the ETXexpress has two 200 pin connectors with the following buses:

- PCIexpress
- PCI
- USB
- I2C
- SATA, PATA
- LPC

Two of the USB ports are available on the front panel of the Radio for keyboard, mouse, GPS, etc. One USB port is used internally for configuring the FPGA via a USB peripheral controller chip.

The Ethernet port allows the CPU to connect to a network. This allows external applications to connect to the CPU over a network. Since the CPU runs a Linux OS these connections can be through SSH, HTTP, etc. Example: A browser on a desk top could connect to a HTTP server on the CPU allowing a user to configure the radio through a graphical interface at the browser. The radio could also be controlled over the Ethernet using a Software Communications Architecture (SCA) interface. Digital data that is RF transmitted or received can pass over the Ethernet interface.

The I2C interface connects to all I2C devices in the radio. There are connectors on the digital board to connect I2C to the RF board and the battery board.

2.2.2 Software

CPU software resides in the ETXexpress Compact Flash memory. The recommended size of compact flash drive to build the software for a KUAR is 8GB. The size required to run a KUAR is 4GB.

2.2.2.1 Operating System

The operating system is a Fedora Linux. The version of Fedora Linux used during initial development is Fedora 5. The Linux kernel used is 2.6.17. The Fedora version of kernel 2.6.18 has a timer problem and is not recommended.

2.2.2.1.1 OS Configuration

2.2.2.1.1.1 Udev

The ‘udev’ system has to be configured to handle the loading of firmware into the USB controller and setting the group and permissions of the USB device.

The firmware for the USB controller (named kuarFX2lp) is placed in /etc/udev/usb/firmware.

‘udev’ rules for the USB controller device are placed in /etc/usb/rules.d/52-usbKUAR.rules. This rules file must us ‘fxload’ to load the firmware into the USB controller when the USB device is loaded. It must set the device group to be ‘kuar’ and set permissions of the device to 0664 to allow anyone user in the ‘kuar’ group to use the USB controller.

The 52-usbKUAR.rules file is one of the locations where the experimental Product ID 0x5001 is used.

2.2.2.1.1.2 Kernel Modules

The Kontron JIDA32 kernel module and library API must be loaded. This kernel module and API is required for use of the I2C bus of the Kontron. The library ‘libkaurI2C’ uses this API and module.

Only the ‘e100’ network module is required for networking.

2.2.2.2 libkuarFX2lp Library

The ‘kuarFX2lp’ library provides an application interface for communication with the USB controller. This library uses the ‘libusb’ open source library locate, open an interface, send KUAR specific commands and receive status and send and receive End Point data.

This program is one of the locations where the experimental USB Product ID = 0x1005 is used to identify the renumerated KUAR firmware in the USB controller.

2.2.2.3 libkuarI2C Library

The kernel I2C mechanism only allows access to the SMBus of the Kontron. The I2C bus of the Kontron can only be accessed through the BIOS using the JIDA32 kernel module and library API. The ‘libkuarI2C’ library is an interface that implements the ‘lm_sensors’ functions ‘i2c_smbus…’.

In the future a kernel module should be created that fits within the kernel I2C module structure then then utilizes the JIDA32 kernel module. The ‘libkuarI2C’could then be removed.

2.2.2.4 libdacSPI Library

A library named ‘dacSPI’ is created for the CPH to allow an application on the CPH to send data to the SPI registers of the DAC. The library makes calls to the kuarFX2lp library to send SPI data to the USB controller. The USB controller in turn sends the SPI data out on dedicated SPI lines to the DAC using a bit-banging method.

2.2.2.5 fpgaCnfg Application

The fpgaCnfg application is responsible for loading a Virtex II Pro bit file into the FPGA via the ‘libkuarFX2lp’ library and the Cypress CY7C68014A USB Peripheral Controller.

The USB side of the controller is connected to 1 of the 8 USB buses of the COMexpress. The GPIF lines of the controller connect to the FPGA.

The Slave SelectMAP programming mechanism is used to configure the FPGA. The 3 pin programming selection jumper(s) must be in the correct position (M0 jumpered, M1 open) for this programming mechanism.

2.2.2.6 fpgaRW

The fpgaRW application is responsible for low level and debugging data interface with the FPGA. It can write data to and read data from registers in an FPGA configuration.

2.2.3 Hardware

The CPH is implemented with the Kontron ETXexpress board.

2.2.3.1 Power

The Kontron ETXeXpress requires a 10.8 to 13.2V voltage supply at a maximum current of 2.5A. The power is delivered to the ETXeXpress board through pins on the two 200pin connectors. The 12V power is obtained from 3 pins on the 24pin Power Board connector.

2.2.3.1.1 Power Conditioning

The 12V power has several large (1mF) electrolytic capacitors.

2.2.3.2 Ethernet Connector

The Ethernet connector is an RJ-45 with LEDs for activity and 100MBs link status. The connector is on the front panel edge of the Digital board near at the same end as the video connector.

Magnetics for the Ethernet are on the digital board.

2.2.3.3 USB Connector

Two USB interfaces are routed from the COMeXpress to the dual USB Type A connector on the front panel.

The Vbus is required to have 120uF of capacitance by the USB 2.0 specification.

Each of the Data lines has an inline inductor to reduce EMI. The inductor must be placed as close to the connector as possible. The TDK Common mode choke ACM2012-900-2P is chosen as described in http://www.tdk.co.jp/epuf/acm2012_e.pdf .

2.2.3.4 I2C and SMBus

2.2.3.4.1 I2C

The general purpose I2C bus of the COMeXpress is used to control I2C devices on the carrier board (Digital board). Note that the I2C bus can control SMBus devices if the bus clock is <= 100kHz**. Since the FPGA temperature sensor is an SMBus device the COMeXpress I2C bus is to be run at 100kHz.**

The following I2C addresses are already used or reserved on the COMeXpress board.

Table 1 ETXeXpress Module I2C Addresses

Address	**Device (Use)**
(0xa0)	EEPROM for CMOS data
(0xb0)	Reserved for ETXeXpress
(0x58)	Reserved for ETXeXpress

The COMeXpress extension connector has an I2C bus on it.

This low speed bus is used to read FPGA junction temperatures using a ADT7461 temperature sensor.

There are 2 devices on the Digital Board that use the I2C bus:

- Temperature Sensor – Measures FPGA junction temperature
- EEPROM – Used to store carrier board information for the COMeXpress.

The following I2C addresses are used by devices on the Digital Board.

Address	**Device (Use)**
B1001100 (0x4C)	ADT7461 (temperature sensor)
B1010111 (0x57)	CPH EEPROM Microchip 24AA64 (64Kbit)

Table 2 Digital Board Used I2C Addresses

The COMeXpress Carrier Board Configuration occupies the top 2048 bits of the memory.

2.2.3.4.2 SMBus

The SMBus is used for system management by the COMeXpress. No carrier board devices shall be placed on the SMBus.

2.2.3.5 EEPROM Memory Map

The EEPROM is used to store semi-permanent information about the COMeXpress carrier board and the Agile Radio Digital board such as hardware board version number.

The COMexpress specification states that the EEPROM shall have an address of 0x57.

NOTE: The Kontron ETXexpress-PM ignores the eeprom! It stores all of its BIOS settings in an internal EEPROM at address 0x50.

2.2.3.5.1 COMexpress Carrier Board Configuration Data

The COMexpress specification states that the carrier board configuration information occupies the top 2048 bits of the EEPROM device. The Microchip 245AA64 EEPROM has 64Kbits.

The top two bytes contain an unsigned integer checksum of bytes 0x1F00 through 0x1FD.

Desc	Value	Byte Address	Byte Length
Checksum of address 1F00-1FFD	0x????	0x00FE	2

Table 3 EEROM Checksum

There is a reserved area from address 0x1FF0 – 0x1FFD. Fill with 0x00.

Desc	Value	Byte Address	Byte Length
Reserved	0x0	0x00F0	14

As a sanity check there is an ID string placed into the EEPROM.

Desc	Value	Byte Address	Byte Length
COMexpress ID string in ASCII	‘COMExpressConfig’	0x00E0	16

Table 4 EEPROM COMexpress ID String

There is a reserved area at 0x1FDF. Fill with 0x00.

Desc	Value	Byte Address	Byte Length
Reserved	0x0	0x00DF	1

No SATA/SAS devices are on the Digital Board.

Desc	Value	Byte Address	Byte Length

No devices implemented	0x00	0x00DE	1

Table 5 EEPROM SATA/SAS Descriptor Byte

There are no Express Cards on the Digital Board.

Desc	Value	Byte Address	Byte Length
No Card1 device implemented	0x00	0x00DD	1
No Card2 device implemented	0x00	0x00DC	1

Table 6 EEPROM Express Card 1 Descriptor Byte

There are 3 used USB channels on the Digital board..

Desc	Value	Byte Address	Byte Length
3 Used USB ports	0x03	0x00DB	1

Table 7 EEPROM USB Descriptor Byte

Only the VGA display is used on the Digital board..

Desc	Value	Byte Address	Byte Length
VGA display only	0x10	0x00DA	1

Table 8 EEPROM Display Descriptor Byte

Only the GBE0 is used on the Digital board..

Desc	Value	Byte Address	Byte Length
GBE0 only	0x01	0x00D9	1

Table 9 EEPROM Ethernet Descriptor Byte

Only Wake1 and Wake0 are use on the Digital board. Unused I/O areAC/97, Watchdog timmer, external BIOS, Thermal Protection, Battery Low and Suspend.

Desc	Value	Byte Address	Byte Length
Wake1 and Wake0 are available	0x03	0x00D8	1

Table 10 EEPROM Miscellaneous I/O Descriptor Byte

There is a reserved area from address 0x1FD7 – 0x1F80. Fill with 0x00.

Desc	Value	Byte Address	Byte Length

Reserved	0x0	0x0080	88

Only 1 PCI lane is used. This lane connects to the FPGA. It uses COMexpress lane 0.

Desc	Value	Byte Address	Byte Length
PCIE 31 not used	0x00000000	0x007C	4
PCIE 30 not used	0x00000000	0x0078	4
…	0x00000000		
PCIE 1 not used	0x00000000	0x0004	4
PCIE 0, 1 lane @ lane 0	0x00000100	0x0000	4

Table 11EEPROM PCI Express Lane Descriptor Data

2.2.3.5.2 Agile Radio EEPROM Information

The Agile Radio portion of the memory map of the EEPROM is as follows:

TBD

2.2.3.6 PCI Bus

The PCI Bus is 32bits wide at a speed of 33MHz. The FPGA is never a Bus Master. It is only a Target Device.

The COM express Specification states that the PCI clock, when connected to a carrier board PCI device (not a PCI slot device) must have a clock delay of 1.6ns. With a FR4 dielectric of 8mils the propagation delay is 0.141 ns per inch which is 11.3 inches for 1.6ns. The tolerance is 0.1nS so the length could be 10.8 inches.

Not all of the PCI signals are used. The following signals are not connected to the FPGA:

- JTAG
- INTB, INTC, INTD
- SB0, SDONE
- LOCK

The FPGA PCI device must use AD[20] as its IDSEL signal.

2.2.3.7 PCIexpress Bus

A single lane of PCIexpress bus is connected to a Rocket IO transceiver of the FPGA.

2.3 USB Peripheral Controller (EZ-USB)

The USB Peripheral Controller is the Cypress Semiconductor CY7C68014A. It's USB lines connect to the USB0 bus of the ComExpress. It's parallel lines connect to the configuration lines of the FPGA. The USB Peripheral Controller is used to configure the FPGA.

With 3 of the USB controller's lines connected to GPIO lines of the FPGA the controller can also be use as a conduit for data transfer between the FPGA and COMeXpress in the same way that classical PCI and PCIexpress is used.

2.3.1 USB Controller Reset

An RC network is placed on the RESET line to ensure that it is de-asserted at least 5ms after power is applied. The recommended R=27K. The recommended C=1uF.

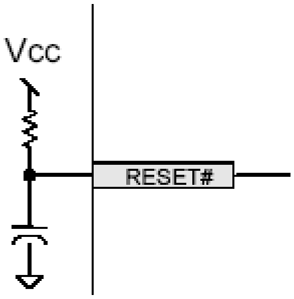
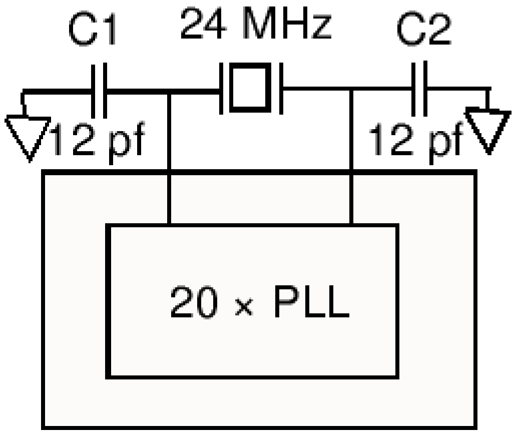


Figure 4 Reset network from CY7C68014A data sheet.

2.3.2 Oscillator

The EZ-USB oscillator is connected as shown in the picture below:



12-pF capacitor values assumes a trace capacitance of 3 pF per side on a four-layer FR4 PCA

Figure 4 Clock network from CY7C68014A datasheet.

2.3.3 USB GPIO

2.3.3.1 Address Logic (FPGA memory map)

The USB controller interface with the FPGA is as a memory mapped device. The USB controller has 3 available address lines that can be used to select registers in the FPGA.

2.3.3.2 USB to SPI

The USB Peripheral controller is used to generate the SPI signals needed to program the DAC. USB commands are received by the controller containing SPI data to send out over the SPI dedicated pins of the controller.

Three of the GPIO lines of the controller are used for the SPI_EN, SPI_MOSI and SPI_CLK signals. The controller CPU is responsible for bit-banging these lines.

2.3.4 GPIF/FPGA Configuration

The FPGA is configured using the GPIF of the USB controller. The Long Transfer Mode is used when writing configuration bits to the FPGA.

2.3.4.1 USB Controller Initial Register Setup

B7:5	B4:3	B2	B1	B0

Don’t Care	CLKSPD	CLKINV	CLKOE	8051RES
0	0x2	0	0	0
Does not apply	48MHz	Clock Out Not Inverted	Clock Out Disabled	Does not apply

Table 12 CPUCS register

The IFCLK is run at 48MHz by setting register IFCONFIG as shown. Clock polarity is inverted so that the FPGA reads data in the middle of a state. The GPIF mode is also set in this register.

B7	B6	B5	B4	B3	B2	B1:0
IFCLKSRC	3048MHz	IFCLKOE	IFCLKPOL	ASYNC	GSTATE	IFCFG
1	1	1	1	X	0	0x2
Internal Clock	48MHz clock	Driven	IFCLK inverted	Does not apply	No Gstate	GPIF mode

Table 13 IFCONFIG Register

The Data output is held for 1 IF clock cycle (state).

B7:2	B1:0
0	HOLDTIME
0	0x2
Does Not Apply	Hold 1 IFCLK cycle

Table 14 GPIFHOLDAMOUNT Register

During the Idle state the data output is put into tristate.

B7	B6:1	B0
Done	0	IDLEDRV
X	0	0
Cant Set	0	Tri-state data bus

Table 15 GPIFIDLECS Register

By setting TRICTL = 1 the outputs CTL2:0 are either CMOS output or Tri-state depending on the settings of GPIFIDLECTL bit CTLOE2:0.

B7	B6	B5	B4	B3	B2	B1	B0
TRICTL	0	NA	NA	NA	CTL2	CTL1	CTL0
1	0	X	X	X	X	X	X
CMOS/Tri	0	X	X	X	X	X	X

Table 16 GPIFCTLCFG Register

B7	B6	B5	B4	B3	B2	B1	B0
CTLOE3	CTLOE2	CTLOE1	CTLOE0	CTL3	CTL2	CTL1	CTL0
0	1	0	1	0	1	1	1
N/A	CMOS	Tri-state	CMOS	N/A	PROGB off	RW read	CE off

Table 17 GPIFIDLECTL Register

This document assumes that the USB bus is operating at High Speed (480 Mbps).

The Endpoints are setup for double buffering. EP2 and EP6 are set to be valid while EP4 and EP8 are set to invalid.

- EP2CFG, VALID=1, TYPE=BULK(0x2), Direction=Out, Buffering = triple, size=512
- EP4CFG, INVALID=0
- EP6CFG, INVALID=0
- EP8CFG, INVALID=0

Set RDY lines to be asynchronous and let the transaction counter be the RDY5 signal:

- `GPIFREADYCFG.SAS = 1`
- `GPIFREADYCFG.TCXRDY5 = 1`

Enable Internal INT4 instead of interrupt pin:

- `INTSETUP.INT4SRC = 1`

Enable autovectoring on INT4:

- `INTSETUP.AV4EN = 1`

Enable the GPIFWF interrupt so that a GPIF state can send an interrupt to the CPU:

- `GPIFIE.GPIFWF = 1`

NOTE: For the GPIFWF we may want to utilize the INTSETUP to streamline interrupt handling.

2.3.4.2 Starting FPGA Configuration

The PROGB signal must be asserted for a minimum of 300nS ($T_{Program}$ symbol from *Xilinx Virtex-II Pro DC and Switching Characteristics* data sheet section “Configuration Timing”).

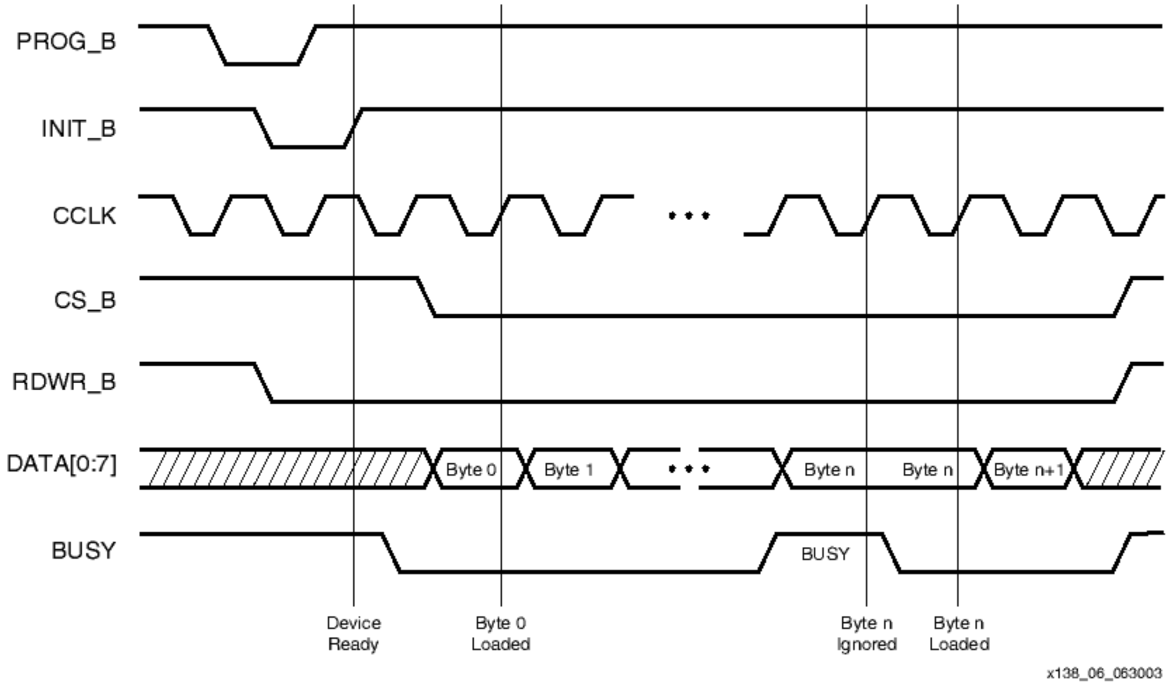


Figure 1 “Express Style” Continuous Data Loading in SelectMAP from Virtext II Pro User Guide.

Slave SelectMAP configuration mode of the FPGA uses 8 parallel data bits therefore:

- `WORDWIDE = 0`

To start the configuration the CPU first check to make sure that the INIT_B line is not asserted. It then asserts the PROGB line. It waits 300uS (using a timer and interrupt) and then checks to see if INITB was asserted. It then deasserts PROGB.

Next the de-assertion of INIT_B must be seen. The amount of time from the de-assertion of PROGB until the de-assertion of INITB is a maximum of 4uSec per frame. The number of frames per device type is as follows:

Device	Number of Frames
P20	1756
P30	1756
P40	2192

Table 18 Number of Configuration Frames per Device Type

The amount of time to wait for the INITB line to be de-asserted by the P20 FPGA is 4uSec * 1756 = 7024 uSec. There are 7024uSec / 20.8nSec = 337,692 clock cycles (@48MHz IFCLK) to wait for the INITB signal to be de-asserted.

If at any time the expected state of the INIT_B line is not seen then the CPH is notified of the error and the configuration state is reset.

2.3.4.3 Send FPGA Configuration Frames to FPGA

Since the FPGA data sheet states that the maximum clock frequency without needing the BUSY line is 50MHz and the EZ-USB IFCLK is at 48MHz, the BUSY line from the FPGA is ignored.

If it becomes necessary to deal with the BUSY signal then the FlowState registers are to be utilized to halt and resume the dataflow.

Enable the DONE interrupt:

???

When the Transaction Count reaches 1 and the IDLE state is entered the DONE interrupt is thrown to let the CPU know that the data transfer is completed.

Enable the Endpoint 2 Empty Flag:

- `EP2GPIFFLGSEL.FS=1`

The state machine uses the Endpoint empty flag to determine that it must deassert the CS_B line and wait for data to enter the Endpoint FIFO before it can write more data to the FPGA.

The Endpoint should only enter the DONE state when the Transaction Count has been met:

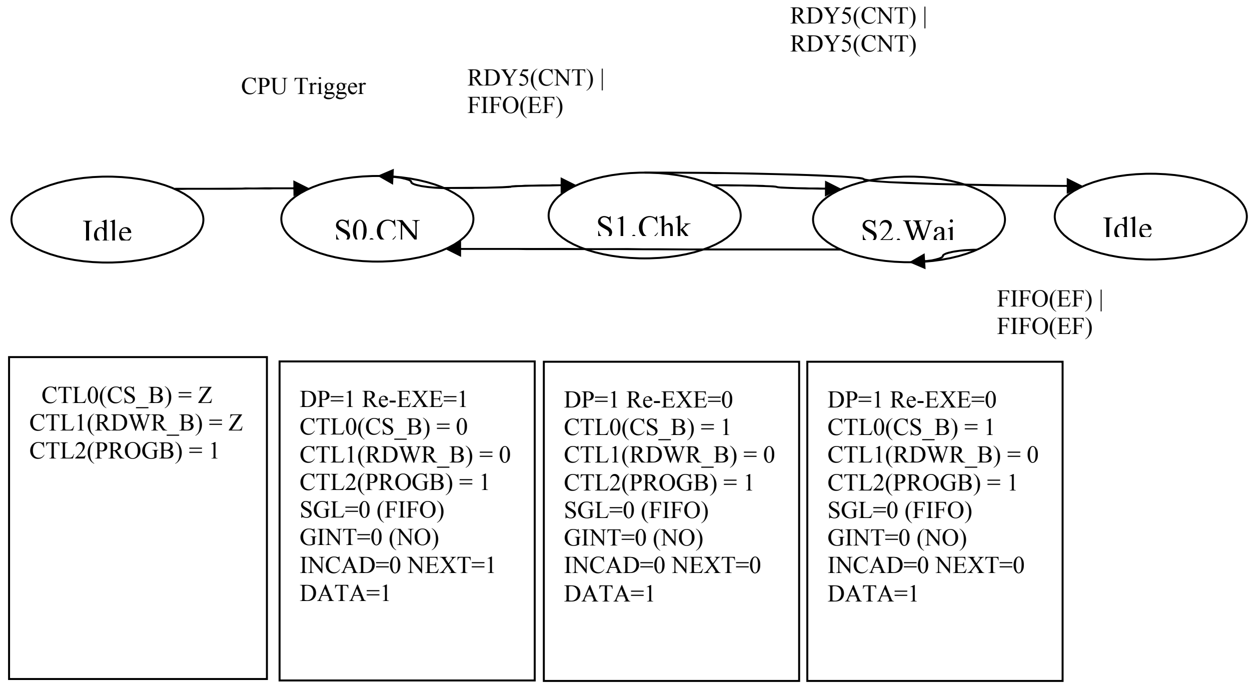
EP2GPIFPFSTOP.FIFO2FLAG = 0

Setup the FIFO Read waveform to be index 0.

- `GPIFWFSELECT.FIFORD = 0`

Start the GPIF states:

- `EP2GPIFTRIG = 0xFF`



CTL0(CS_B) = Z
CTL1(RDWR_B) = Z
CTL2(PROGB) = 1
	DP=1 Re-EXE=1
	CTL0(CS_B) = 0
	CTL1(RDWR_B) = 0
	CTL2(PROGB) = 1
	SGL=0 (FIFO)
	GINT=0 (NO)
	INCAD=0 NEXT=1
	DATA=1
		DP=1 Re-EXE=0
		CTL0(CS_B) = 1
		CTL1(RDWR_B) = 0
		CTL2(PROGB) = 1
		SGL=0 (FIFO)
		GINT=0 (NO)
		INCAD=0 NEXT=0
		DATA=1
			DP=1 Re-EXE=0
			CTL0(CS_B) = 1
			CTL1(RDWR_B) = 0
			CTL2(PROGB) = 1
			SGL=0 (FIFO)
			GINT=0 (NO)
			INCAD=0 NEXT=0
			DATA=1

Figure 1 SelectMap Slave data write state diagram.

2.3.4.4 FPGA Configuration Success Check

After the configuration data has been written the INITB and DONE lines must be checked for problems. If there was a CRC error then INITB will be asserted by the FPGA.

The CPU should perform a 1 time poll on the INITB line. If the value is 0 then a CRC error occurred and the host must be notified of the error. If the value is 1 then continue.

Next the CPU should perform a 1 time poll on the DONE line. If the value is 0 then the FPGA did not finish its startup sequence. This error must be reported to the Host. If the value is 1 then the FPGA was successfully configured. It may be desirable to add in a 6 cycle wait period (@ 48 MHz) before sampling the DONE pin since the FPGA takes about 6 internal clock cycles before it releases the DONE pin.

2.4 FPGA

2.4.1 Intro

The FPGA unit takes digital message signal data from the serial or Ethernet port and outputs it as baseband modulated data to the DAC.

2.4.2 Firmware

The design of the firmware is TBD.

Input/Output Library Components.

Banks 1 (DAC), 2 (SRAM0), 3 (SRAM1), 6 (SRAM2) and 7 (SRAM3) use DCI on their output lines. This means that the VRP and VRN pins of these banks are dedicated to resistors that match the impedance of the traces on their respective banks. The use of DCI standards on these banks causes the FPGA to put series termination resistance on each output pin that is a OBUFT_LVDCI_## library component. There is no input termination for the DCI scheme so inputs should be IBUFT_LVCMOS33_24 for the DAC. Clock outputs are cleaner if destination parallel termination is used. The hardware has been designed so that DAC, ADC, and memory clocks are all parallel terminated so these lines must use OBUFT_LVCMOS33_24 library components for the DAC and OBUFT_LVCMOS24_24 for the SRAMs.

The SRAM data lines are IO lines so these must use IOBUFT_LVDCI25 library components.

Banks 0 (ADC) and 4 and 5 (CPH, TP) do not use DCI so these lines use IBUFT_LVCMOS33_24 for input lines, OBUFT_LVCMOS33_24 for output lines and IOBUFT_LVCMOS33_24 for bi-directional data lines.

For all non DCI lines use slow slew rate initially until testing has been completed to determine which lines can use fast slew rate.

2.4.2.1 PCI interface

The PCI interface lines are on Banks 4 and 5.

The IDSEL signal is AD[20] for the FPGA.

2.4.2.1.1 Configuration Addresses

The Vendor ID to use is difficult since ITTC/KU does not have a PCI Vendor ID. The "Kontron Canada" has been chosen (0x1058) since the ETX is a Kontron device.

The Product ID has been chosen to be 0xAAAA. This is arbitrary since the PCI VendorId/ProductID lists found in a Web search did not turn up any product IDs with the Kontron Canada Vendor Id.

Byte/DblWrd Addr	3	2	1	0
	Dev Id		Vendor ID	
0x00	0xAAAA {R}		0x1058 {R}	
	Status		Command	
0x01	0000 0000 0000 0000b		0000 0000 0010 0010b {R}	
	Class Code	Sub Class	Prog. I/F	Revision ID
0x02	0xFF {R}	0x00 {R}	0x00 {R}	0x00 {R}
	BIST	Header Type	Latency Time	Cach Ln Size
0x03	0x00 {R}	0b{R} 0000000b	0x00 {R}	0x00 {R}
	Base Address Register 0			
0x04	0xFFFFFFE{R/W} 0x0{R}			
	Base Address Register 1			
0x05	0xFFFF000{R/W} 0x0 {R}			
	Base Address Register 2			
0x06	0xFFFF000{R/W} 0x0 {R}			
	Base Address Register 3			
0x07	0x0000000{R} 0x0 {R}			
	Not implemented Base Address Registers			
0x08..0x09	0x00000000 {R} or leave unimplemented			
	CardBus CIS Pointer			
0x0A	0x00000000 {R}			
	Subsystem ID		Subsystem Vendor ID	
0x0B	0x0000{R}		0x0000{R}	
	Expansion ROM Base Address			
0x0C	0x00000000{R}			
	Reserved			
0x0D	0x00000000 or leave unimplmented			
	Reserved			
0x0E	0x00000000 or leave unimplemented			
	Max_Lat	Min_Gnt	Int_Pin	Int Line
0x0F	0x00 {R}	0x00 {R}	0x01 {R}	0xFF {R/W}

Table 19 PCI Configuration Registers

Bit	Reset Value {read/write}	Comment
0	0 {R}	Does NOT use IO Access
1	1 {R}	Uses Memory Access
2	0 {R}	Not a Master Device
3	0 {R}	Special Cycle Recognition not implemented
4	0 {R}	Memory Write and Invalidate not implemented
5	1 {R}	VGA Palette Snoop need=1 for non VGA device
6	0 {R}	Does NOT handle PERR
7	0 {R}	Wait Cycle, Does not support stepping
8	0 {R}	Does not support SERR
9	0 {R}	Fast Back-to-Back Enable only used by bus master
15:10	0 {R}	Reserved

Table 20 PCI Configuration Command Register

Bit	Reset Value {read/write}	Comment
4:0	0 {R}	Reserved
5	0 {R}	Not 66MHz capable
6	0 {R}	No User Definable Features
7	0 {R}	Fast Back-to-Back only implemented by BusMasters
8	0 {R}	Data Parity Reportedonly implemented by BusMasters
10:9	00b {R}	Fast DELSEL# timing
11	0 {R}	Target Abort not implemented
12	0 {R}	Received Target Abort only implemented by BusMasters
13	0 {R}	Received Master Abort only implemented by BusMasters
14	0 {R}	Signaled SERR# not implemented
15	0 {R}	Detected PERR# not implemented

Table 21 PCI Configuration Status Register

Revision ID Register is 0x00.

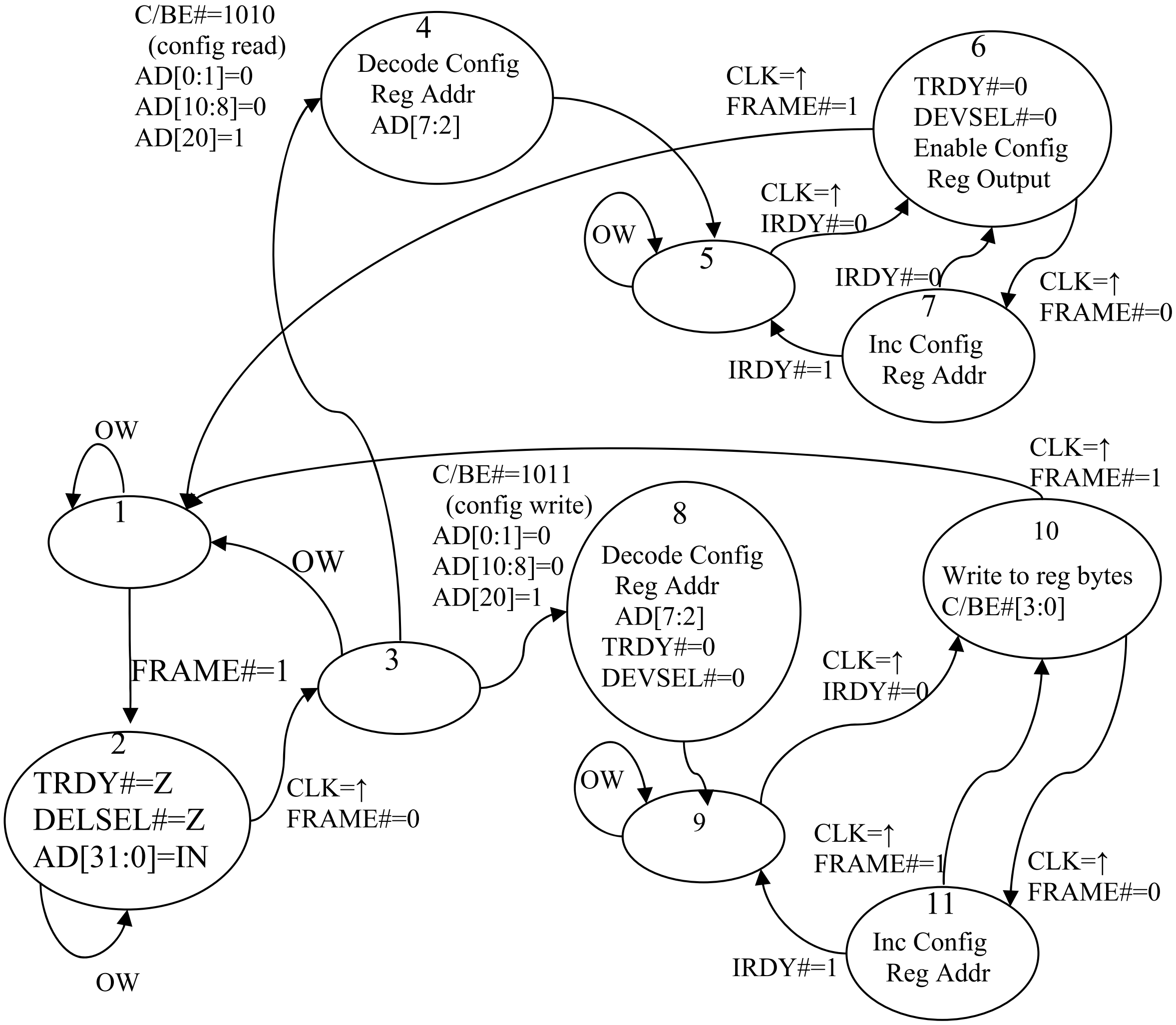
Class Code = 0xFF since this PCI device does not match any standard class codes.

Base Address Register 0 is intended for command and status registers and is 32 double words in size.

Base Address Register 1 is intended for a transmit data FIFO. It is 16k double words in size.

Base Address Register 2 is intended for a receive data FIFO. It is 16k double words in size.

Base Address Register 3 indicates to the host that it is not implemented by being read only with a value of 0x00000000. The PCI assumes that all of the other Base Address Registers are not implemented.



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State1 – This is the initial state and the state to wait in until another PCI device's data phase is complete. A data phase is complete when FRAME#=1. While FRAME#=0 the state machine stays in this state. When FRAME#=1 the state machine moves to State 2.

State2 – This state detects the start of an address phase. An address is on the AD lines on the first CLK↑ after FRAME#=1. While the start of an address phase had not been detected the state machines stays in State1. When the start of an address phase has been detected the state machine moves to State 3.

State3 – In this state the state machine looks at C/BE#[3:0] (which contains the 4 bit command) do determine which set of states to jump to. For a configuration read or write it also looks at the AD lines. For a configuration read or write the AD[0:1] bits must=00b to indicate a type 0 address, AD[10:8] must =000b to indicate device function 0 (the only function the FPGA will have) and AD[20] must =1b to indicate the IDSEL for the FPGA. If the AD lines are correct and C/BE#=1010b then a configuration read is indicated and the state machine jumps to State 4. If the C/BE#=1011b then a configuration write is occurring and the state machine jumps to State 8. For all other conditions either the C/BE# is not supported or the address is for another PCI device so the state machines jumps to State 1 to wait for the end of the data phase of the current transaction. The state machine should never pause in state 3. It should look at the condition of the signals and immediately jump to another state.

State 4 – The state machine must decode the address held in AD[7:2] to determine the address of the configuration double word (32 bits) that is to be read. AD[7:2] must be latched into an address latch bits [5:0]. The state machine does not stay in State 4. It must immediately jump to State 5.

State 5 – State 5 waits for the CLI↑ and IRDY#=0 exit condition. This condition indicates that the PCI bridge is ready to accept data on the AD bus. If IRDY#=1 then the PCI is busy doing something and the state machine must wait in State 5 until the exit condition. When the exit condition occurs the state machines jumps to State 6.

State 6 – This state puts data on the AD bus (all 4 bytes) and tells the PCI bridge that the data is ready by asserting TDRY#=0 and DEVSEL#=0. The state machine waits in this state until the next CLK↑. If FRAME#=1 then the data transfer is complete and the state machine changes to State 1. If FRAME#=0 then there is another data transfer coming for the next configuration register so the state machine jumps to State 7.

State 7 – The purpose of this state is to increment the configuration register address latch value. The state machine does not ever wait in this state. If IRDY#=0 then the PCI bridge is ready for the data so jump to State 6. If IRDY#=1 then the PCI bridge is not ready for the new configuration register data yet so jump to State 5.

State 8 – This state is the start of data phase of a configuration write. The AD[7:2] configuration register address is decoded and write to a address latch bits [5:0]. TDRY=0 is asserted and DEVSEL#=0 is asserted. The state machine immediately jumps to State 9. The state machine never waits in this state.

State 9 – State 9 waits for the CLI↑ and IRDY#=0 exit condition. This condition indicates that the PCI bridge is ready to send data on the AD bus. If IRDY#=1 then the PCI is busy doing something and the state machine must wait in State 9 until the exit condition. When the exit condition occurs the state machine jumps to State 10.

State 10 – This state reads that data on the AD bus and writes it to a configuration register. Only this bytes indicated by C/BE#[3:0] are written. If C/BE#[3]=0 then the line is asserted and the top byte (byte 3) of the AD data is written to upper byte (byte 3) of the currently addressed configuration register. C/BE#[0] is the low byte indicator. The bytes to write may be enabled in any combination. Bytes that do not have their C/BE# bit asserted must not be changed. Example: C/BE# = 1010b, in this case bytes 3 and 1 of the currently addressed configuration register are to be written from the AD bus corresponding bytes but bytes 2 and 0 of the configuration register are to remain unchanged.

The State machine waits in this state until the next CLK↑ event. If FRAME#=0 then the state machine moves to State 11. If FRAME#=1 then the state machine moves to State 1.

State 11 – State 11 is entered when the PCI bridge has indicated that there are more bytes to write to the configuration registers. The address in the configuration address latch is incremented and the state machine moves to State 9.

2.4.3 Hardware

The FPGAs is implemented with the Xilinx XC2VP30FG676 Vertix II-pro. Please refer to the DSU firmware design document for the pin-out information for this subsystem.

2.4.3.1 FPGA Configuration Selection (M pins)

The type of configuration used by the FPGA is determined by the M2, M1 and M0 dedicated configuration pins. We are only using JTAG, Slave SelectMAP and SlaveSerial configuration modes. JTAG and SlaveSerial are performed with off board programmers. SlaveMAP is used by the CPH. One jumper can be used to set the configuration mode.

Table 22 Configuration Mode Pins

Mode	M2	M1	M0
JTAG	1	0	1
Slave-Serial	1	1	1
Slave SelectMAP	1	1	0

One jumper used on a 3 pin header can select the configuration mode. Each H pin has a weak pull-up resistor in the FPGA. Pin H2 is left unconnected so that it has a continuous 1 value.

A 3 pin header should be connected as follows:

Table 23 Configuration Mode Jumper Connection to FPGA

Pin	Signal
1	M0
2	GND
3	M1

4	GND

With a jumper on pins 1 and 2 the FPGA is configured for JTAG mode since M1 is 0 and M0 is 1 (due to the weak pull-up resistor built in to the H pins).

With the jumper on pins 2 and 3 the FPGA is configured for Slave SelectMAP mode since M0 is 0 and M1 is 1.

With NO jumpers at all the Slave-Serial mode is set.

Note: Even though the PINs use LVCMOS25 they are 3.3V tolerant.

Table 24 Configuration Mode Jumper Usage

Configuration Mode	Jumper Pins
JTAG	1 & 2
Slave SelectMAP	2 & 3
Slave-Serial	No Jumper

2.4.3.2 HSWAP_EN Pin

The HSWAP_EN pin is left unconnected so that the configuration I/O pins internal pull-up resistors are disabled. Since the dedicated configuration pins (2.5V levels) are driven or read by the Cerfcubes 3.3V signals we want to use external pullup resistors to control current. Leaving HSWAP_EN unconnected allows this.

2.4.3.3 VBATT Pin

Encryption is not used to configure the device so the VBATT pin is left unconnected.

2.4.3.4 PWRDWN_B

This pin is left unconnected. There is an internal pull-up resistor the takes care of the logic value on this pin.

2.4.3.5 DXN, DXP

The Junction Temperature of the FPGA is measured by a MAX1618 using the DXP and DXN pins of the FPGA. The temperature is obtained by the Cerfcube from the MAX1618 using the I2C bus of the Cerfcube. Note that the bus must be run at <100kHz since the MAX1618 uses the SMBus. The SMBus is not designed to run at more than 100kHz. It is compatible with the I2C bus otherwise.

Leaving the address pins of the MAX1618 unconnected gives the chip an I2C address of b0101010.

2.4.3.6 RocketIO for PCIeXpress

The COMeXpress module's PCIE0 is connected to the FPGA's RocketIO.

2.4.3.6.1 PCIe TX Signal AC Signal Coupling

The COMeXpress specification[1] requires that the TX lines from the RocketIO have AC coupling capacitors. The AC coupling capacitor value is determined from the equation obtained from the Maxim-IC app note 292 [2] where:

$C = 7.8N_{CID}T_b/R$

- N_{CID} is number of consecutive bits of same value. PCIeXpress uses 8b/10b encoding so that the maximum number of consecutive bits in a byte/10b is 5. With 2 consecutive bytes the number of consecutive bits with the same value is 10.
- T_b is time per bit in seconds
- R is termination resistance in ohms.
- C is AC coupling capacitor value in F

C = 7.8 * 10 * (1/2.5Gbps) / 50 = 624pF. Since 1nF capacitors are already used on the board 1nF is used of the AC coupling capacitors for the PCIexpress transmit lines.

The Xilinx RocketIO User Guide[3] recommends 0.01uF for the AC coupling capacitors.

2.4.3.6.2 Termination Voltage Vt

The Vttx voltage is 2.5V. The Vtrx is 1.8V per the Rocket IO Userguide[[3]] for AC coupled signals

2.4.3.6.3 Power Conditioning

The 2.5V need for RocketIO power is generated using a 2.5V linear regulator fed from the Vcc3.3 board voltage. The Xilinx Rocket IO User Guide [3] lists several proven Linear Regulators. The TI TPS79625 is a reasonable choice.

The 2.5V power is used for AVCCAUX TX and RX and for VTTX. See below for VTRX.

Maximum power draw for a RocketIO is 350mW which gives a current of 0.35mW/2.5V=140mA. The dissipated power in the linear regulator is (3.3V – 2.5V) * 140mA =

180mW. This is well below the heat dissipation capability of the TPS79625 in the SOT-223 package with no air flow and no copper heat sink.

The RocketIO User Guide recommends eight 1uF capacitors on the output of the linear regulator. Since the Digital Board is only using one transceiver this board will only use four of the 1uF capacitors.

The RocketIO User Guide recommends a 0.22uF capacitor in a 603 package on each power line into the transceiver. Since the board already is using many 0.1uF capacitors this design uses two 0.1uF capacitors in 402 packages instead of the 0.22uF in a 603 package.

For the VTRX voltage the Rocket IO User Guide recommends 1.6V to 1.8V when AC coupling is used (which is the case for PCIe). The Texas Instruments TPS79518 is used for the VTRX regulator.

2.4.3.6.4 PCIe Reference Clock

Since the PCIe data rate is greater than 2.5Gsps the BREFCLK of the RocketIO must be used.

2.4.3.7 Configuration of FPGA by Desktop/Laptop computer.

Use JTAG for programming by a desktop computer. This means that the dedicated JTAG pins are connected to a 14in header with 2mm pitch. This is the same pin position as with the Xilinx Parallel Cable IV connector.

Table 25 FPGA JTAB Header Pinout

JTAG Header Pin	TJAG Signal
2	Vref (3.3V)
4	TMS
6	TCK
8	TDO
10	TDI
12	NC
14	NC

The connectors are placed on the edge of the Digital Board. The header is right angle so that it can be accessed when the Digital Board is in a stack of boards. There is no need for the connectors to be accessible when the front and back panels of the radio are in place (no panel mount connectors for JTAG needed).

2.4.3.8 Configuration of FPGA by CPH

The CPH configures the FPGA using the FPGA Slave SelectMAP configuration mode. This allows 8 bit parallel configuration. The FPGA (Virtext II Pro) can be programmed at up to 50Mbytes per second in SlaveMAP mode. The Cypress CY7C68014A has its interface clock (IFCLK) set to 48MHz.

The mapping of CPH to FPGA pins are as follows:

FPGA pin	**USB Cntlr signal name**	**FPGA Signal level**	**Notes**
D0 (MSB)	FD7	3.3V	
D1	FD6	3.3V	
D2	FD5	3.3V	
D3	FD4	3.3V	
D4	FD3	3.3V	
D5	FD2	3.3V	
D6	FD1	3.3V	
D7 (LSB)	FD0	3.3V	
CS_B	CTL0	3.3V	
BUSY	RDY0	3.3V	
RDWR_B	CTL1	3.3V	
INIT_B	RDY1	3.3V, Open Drain	4.7k pullup 3.3V
CCLK	IFCLK(inverted)	2.5V	100ohm series
DONE	PA1	2.5V	470 ohm pullup 3.3V

PROG_B	CTL2	2.5V	100 ohm series 4.7k pull-up 3.3V

The CCLK signal is run at <=50MHz (Fcc_SelectMAP from FPGA datasheet, DC and Switching Characteristics p.37) so that the BUSY line from the FPGA can be ignored.

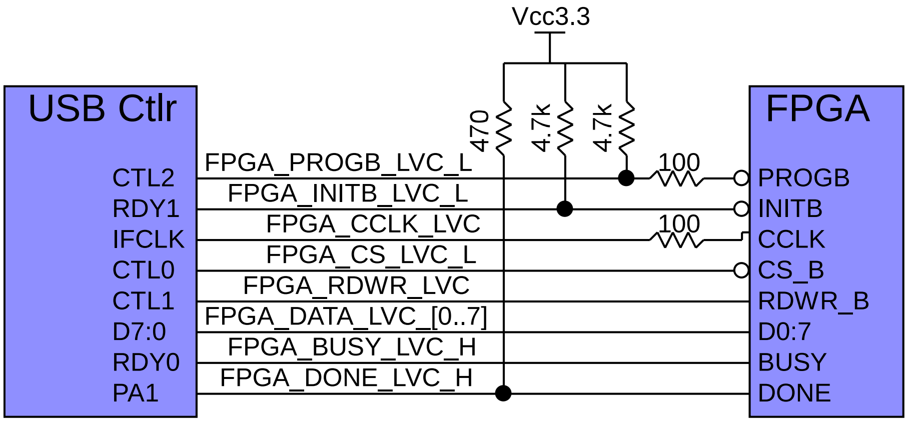


Figure 2 FPGA Configuration Signals

Read the FPGA User Guide for how to use the CerfCube GPIO6, 7, and 8 signals (FPGAINITB_L_V, FPGAPROGB_L_V and FPGADONE_L_V) to initiate a configuration and how to detect that it is complete.

2.4.3.9 FPGA IO Pin Assignments

2.4.3.10 FPGA Bank Summary

This section contains the totals for the number of pins used in each FPGA bank and gives the general purpose of the bank and groups of pins within the banks. The purpose of this section during design was to ensure that pins in a bank were not over allocated. This section also provides a quick reference for future designs to determine which banks have available pins.

Bank0 of the FPGA is connected to the DAC and SRAM0. There are a maximum of 43 IO pads on bank 0.

Lines	Count
DAC TX I Data	16
DAC TX Q Data	16
DAC CLK (diff)	2
DAC RST	1
DAC PLL LOCK	1
GCLK (16MHz)	1
ADC Sleep	1
VRN,VRP	2
Empty	3
Total	**43**

Table 26 Bank 0 Line Count

Bank1 of the FPGA is connected to the dual ADC. There are a maximum of 43 IO pads on bank 1.

Lines	Count	
ADC RX I Data	14	
ADC RX Q Data	14	
ADC CLK (diff)	2	
ADC OVR (I&Q)	2	
Test Point	9	
Empty	2	
Total	**43**	

Table 27 FPGA Bank1 Line Count

Bank2 of the FPGA is connected to SRAM0. There are a maximum of 58 IO pads on bank 2.

Table 28FPGA Bank2 Line Count

Lines	Count
SRAM0 Addr 2-17	16
SRAM0 Data 0-31	32
SRAM0 BWE 0-3	4
SRAM0 CLK	1
SRAM0 RDRW	1
SRAM0 CE	1
SRAM0_ADV/LD	1
VRN, VRP	2
Total	**58**

Bank 3 of the FPGA is connected to SRAM1. There are a maximum of 58 IO pads on bank 3.

Table 29 Bank 3 Line Count

Lines	Count
SRAM1 Addr 2-17	16
SRAM1 Data 0-31	32
SRAM1 BWE 0-3	4
SRAM1 CLK	1
SRAM1 RDRW	1
SRAM1 CE	1
SRAM1_ADV/LD	1
VRN, VRP	2
Total	**58**

Bank 4 of the FPGA is connected to the USB controller and the Kontron PCI bus. There are a maximum of 43 IO pads on bank 4. Note that the DONE configuration signal is not considered part of the bank so is not counted in the IO pins.

Table 30 Bank 4 Line Count

Lines
FPAG Cnfg 0:3/USB Data 7:4
FPGA Cnfg INIT_B
FPGA Cnfg BUSY
PCI_AD22:31
PCI_C/BE3#
PCI_IRQA#
PCI_CLKRUN#
PCIe_REFCLK
WAKE0# (PCIe wake)
WAKE1#
USB_CLK
USB_DATA[8:15]
USB_ADDR[0..2]

Bank5 of the FPGA is connected to the USB Controller and the Kontron PCI bus. There are a maximum of 43 IO pads on bank 5.

Lines
FPGA Cnfg D7:4
FPGA Cnfg CS_B
FPGA Cnfg RWWRB
PCI_PME#
PCI_Reset#
PCI_AD 0:21
PCI_C/BE#0:2
PCI_PAR
PCI_SERR#
PCI_PERR#
PCI_STOP#
PCI_TRDY#
PCI_DEVLSEL#
PCI_FRAME#

Table 31 Bank 5 Line Count

Bank 6 of the FPGA is connected to SRAM2. There are a maximum of 58 IO pads on bank 3.

Table 32 Bank 6 Line Count

Lines	Count	
SRAM2 Addr 2-17	16	
SRAM2 Data 0-31	32	
SRAM2 BWE 0-3	4	
SRAM2 CLK	1	
SRAM2 RDRW	1	
SRAM2 CE	1	
SRAM2_ADV/LD	1	
VRN, VRP	2	
Total	**58**	

Bank 7 of the FPGA is connected to SRAM3. There are a maximum of 58 IO pads on bank 3.

Table 33 Bank 7 Line Count

Lines	Count
SRAM3 Addr 2-17	16
SRAM3 Data 0-31	32
SRAM3 BWE 0-3	4
SRAM3 CLK	1
SRAM3 RDRW	1
SRAM3 CE	1
SRAM3_ADV/LD	1
VRN, VRP	2

2.5 Memory

The memory on the board consists of 4 SRAM chips. Each SRAM is configured as 256K x 36bits. 32 of the bits are for tables, CPU instructions, etc. and 4 of the bits are for parity but are not connected. Each SRAM is connected to its own bank of the FPGA. Each memory devices has a dedicated bank of the FPGA, banks 3, 4, 6 and 7.

The address bus and data bus for each memory had independent traces on the board so they can be used independently or they can be tied together within the FPGA. Various FPGA configurations for the memory are:

- One SRAM for each CPU to hold instructions, stack and data segments. One SRAM for an input Tx buffer and the last for an Rx buffer.

- Two SRAMs for each CPU configured within the FPGA to be adjacent in memory. In this case it may be necessary to make the memory dual ported so that tables for the FPGA can also be stored on them. Some table memory could be stored in FPGA Select RAM.

The SRAM chosen for the design is the Cypress CY7C1354A-166BGC. This chip is available from Digikey for $16.35 for quantity 1.

2.5.1 Signals

The ADV/LD line is connected between the FPGA and the SRAM so that burst access is available. The A0 and A1 lines are run for the same reason although if bursts always start on a word boundary A0 and A1 could be tied low.

The following lines are tied as follows:

- CEN tied LOW – There should be no need to disable the clock (and other inputs) with this line. The clock to the memory can always be stopped in the FPGA

- OE tied LOW – Since the memory chip does not require this line to be high for write operations and the chips do not share a data bus so we can tie it low.

- CE is pulled HIGH – If the FPGA is not configured to control the memory then this pullup prevents the memory from ever enabling. Being enabled by a floating CE input could cause the memory to use a lot of power.
- CE3 tied LOW – We will let the FPGA do all chip selections with the CE line so tie this one low.
- CE2 tied HIGH - We will let the FPGA do all chip selections with the CE line so tie this one high.
- MODE tied LOW – Lets use linear mode for all burst traffic.
- TCK tied LOW.

Banks 0 and 1 have a common ZZ line from bank3. Banks 2 and 3 have a common sleep line from Bank 6.

NOTE: The clock pin should be routed so that it cannot cross talk with any other pin.

The following lines are left floating:

- TDO
- TDI
- TMS

2.5.2 Support Components

Bypass capacitors must be added to the VCC and VCCQ pins of the memory chips.

Much of the following is based on information from the SRAM_GUIDELINES_APPNOTE3 at http://www.cypress.com/cfuploads/support/app_notes/sram_guidelines_appnote3.pdf.

To prevent voltage sage due to the output buffers, capacitors on the VCCQ lines are needed. There are 36 output buffers (36 output data lines). The Capacitance needed to prevent voltage sage is I * dt/dV. I = #output * V/impedance. Dt is the amount of time to rise from Vol to Voh. This is not specifically specified by the Cypress datasheet or the FPGA datasheet so a worst case must be calculated. With a 166MHz clock maxium rise time of the outputs has to be < ‘Clock to Output Valid’ – ‘Clock to Output Invalid’ (tKQ – tKQX, see the Cypress data sheet, 3.6ns – 1.0nx) = 2.5ns. The Impedance in the equation is the characteristic impedance of the trace = 56 ohm (matches a standard resistor value).

With a 2.5V IO voltage the total capacitance needed on VCCQ is as follows: the lowest VCCQ voltage is 2.375 (allowable voltage drop is then 2.5 – 2.375 = 0.125). The current for a 2.25 voltage High output is then 2.25V / 56ohm = 40mA. The total capacitance needed is then 36 lines * (2.25V / 56 ohm) * (2.5nS / 125 mV) = 30nF.

The recommended frequency to decouple is 0.5/(fastest rise time). The Cypress memory used in this design was tested (per the datasheet) with input rise/fall times < 1nS. A 1nS rise/fall time gives a 0.5/1nS = 500MHz resonant frequency. The rise/fall time calculated earlier (2.5ns) would require a resonant frequency of 200MHz. The capacitor chosen should have a resonant frequency close to 500MHz be but more than 200MHz. Possible capacitors:

- AVX. 270pF, ceramic, X7R, 50V, 0402, SRF=484MHz, ESR at SRF=0.275Ohm, ESL=0.4nH
- AVX, 220pF, ceramic, X7R, 50V, 0603, SRF=480MHz, ESR at SRF=0.501Ohm, Z=3.8 at 166MHz, ESL=0.5nH (Mfg#=0603TC221KAT2A, $0.16).
- Kemet, 180pF, ceramic, X7R, 50V, 0402, SRF=501MHz, ESR at SRF=1.076Ohm, ESL=0.580nH (Mfg#=C0402C181K5RAC7867, $0.37)
- Kemet, 220pF, ceramic, X7R, 50V, 0402, SRF=446MHz, ESR at SRF=1.001Ohm, ESL=0.610nH (Mfg#=C0402C221K5RAC7867, $0.37).
- Kemet, 220pF, ceramic, X7R, 50V, 0603, SRF=467MHz, ESR at SRF=1.226, Z=4.49 at 166MHz, ESL=0.540nH (Mfg#=C0603C221K5RAC7867, $0.09)
- Kemet, 120pF, ceramic, C0G, 50V, 0603, SRF=457MHz, ESR at SRF=0.164, Z=7.0 at 166MHz, ESL=0.925nH, (Mfg#=C0603C121J5GAC7867, $0.13).
- Vishay, 330pF, ceramic, X7R, 50V, 0402, SRF=477mHz, ESR at SRF=1.184ohm, ESL 0.34nH
- Vishay, 180pF, ceramic, NP0, 50V, 0603, SRF=499.5mHz, ESR at SRF=0.214ohm, Z=4.7 at 166MHz, ESL 0.56nH (Mfg#=VJ0603A181JXBAC, $0.16).

Since the VCCQ lines are all on the edge of the memory BGA, using a 0603 package on the VCCQ lines instead of the 0402 packages can reduce the board cost. On the internal VCC lines the 0402 package should be used.

The Kemet, 220pF, ceramic X7R, 50V 0603 is selected for the VCCQ lines. At a peak current of (2.25V/56ohm)=40mA the voltage drop in the capacitor is 40mA * 1.225 ohm (capacitor impedence) = 48mV (single capacitor). This still keeps us close to the input voltage tolerance (125mV drop) until near the time the capacitors are discharged.

10 of the Kemet 220pF capacitors on the VCCQ lines (1 per line) provide 2.2nF of capacitance. This does not meet the 0.01uF requirement that was calculated earlier. To provide the remaining capacitance 3.3nF capacitors shall be added (1 per line).

2.6 Digial To Analog Converter (DAC)

2.6.1 DAC Introduction

The DAC system is implemented with the Analog Devices AD9777. The purpose of the DAC is to take a digital base-band signal from the FPGA and convert it into an analog base-band signal to be provided to the RF section. A pin-out of the AD9777 is supplied below.

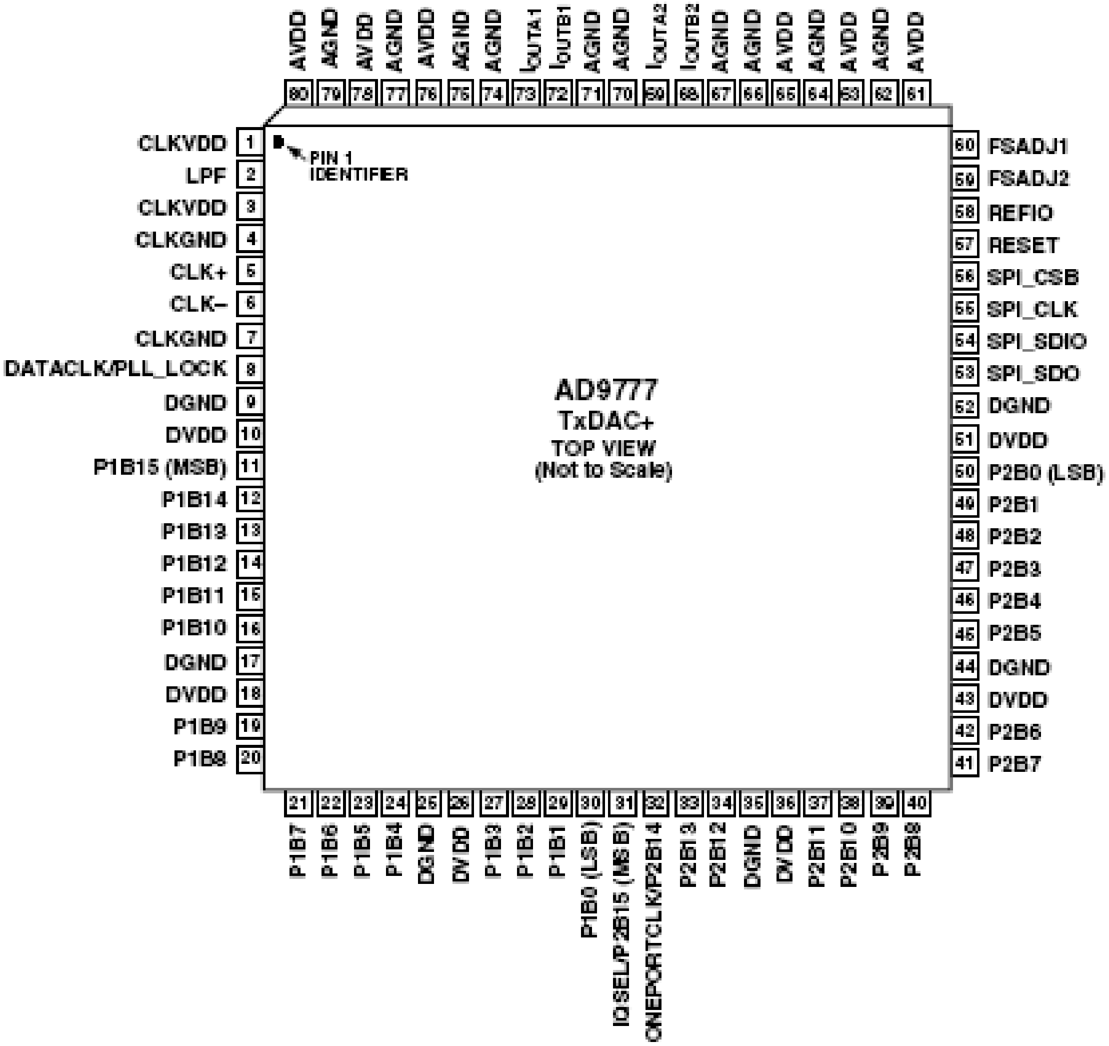


Figure 3 AD9777 Pinout

2.6.2 DAC Signals

The following is a description of the pin usage on the AD9777 for this project. Note that the pin usage for some pins is determined by the particular configuration of the SPI registers. Please refer to the Analog Devices AD9777 datasheet for more information.

2.6.2.1 DAC Digital Input

Digital Input is composed of 32 Data lines (I + Q), 2 CMOS clock lines (differential) and 1 SPI reset line.

2.6.2.1.1 DAC Data Input

The data is provided on two 16-bit ports, the in-phase data on port 1 and the quadrature data on port 2. Port 1 data is input on pins 11-16, 19-24, and 27-30., with pin 11 being the most significant bit and pin 30 being the least significant bit. Port 2 data is input on pins 33, 34, 37-42 and 45-50, with pin 33 being the most significant bit and pin 50 being the least significant bit.

2.6.2.1.2 DAC Clock

The data is clocked into registers via the differential clock signals, CLK+ and CLK- on pins 5 and 6, respectively. The DAC clock is driven with differential LVDCI signals from the FPGA. The DAC_CLK_LVC_P signal from the FPGA is driven to CLK+. The DAC_CLK_LVC_N signal from the FPGA is driven to CLK-.

The clock lines are terminated with parallel RC network. The RC time constant must be larger then 2 times the propagation delay of the clock signal. The signal length is approximately 2 inches. With a propagation delay of 0.14 ns/in the RC time constant must be > than 0.56 ns. With R=75 ohm and C=10pF the time constant is 0.75ns. This is sufficient.

2.6.2.2 DAC Analog Output

The analog output of the DAC is a differential signal for both in-phase (I) and quadrature (Q) channels. The in-phase channel is supplied on pins 73 and 72 and the quadrature channel is supplied on pins 69 and 68. The gain and the DC offset of the output are determined in terms of current, which is discussed later in the SPI configuration.

A resistor network is used to set the center voltage and the Vp-p of the differential output signals.

The Vbias DC occurs when both sides of the output are at 10mA (signal mid swing). Vbias = 400mV is desirable.

The max voltage on one line and min voltage on the other line occurs when one line is 20mA (signal full swing) and the other is 0mA (signal min swing). Vmax = 693mV is desirable.

The min voltage = 108mV is desirable.

The voltage swing on one line is them Vmax – Vmin = 585mV. The differential Vp-p is then 2 *

585mV.

Vp-p= 1.170V

2.6.2.3 DAC Control

A majority of the control signals for this device must be programmed through the SPI interface. There are, however, a few that are not. Pin 57 resets all of the SPI port registers when asserted logic high. This is in contrast to the SPI reset bit which resets all SPI port registers except the register. Pin 60 (FSADJ1) controls the I_{REF} current by placement of the appropriate value resistor from pin 60 to ground. Pin 60 has a nominal voltage output of 1.2 V which drives the I_{REF} current.

2.6.2.4 DAC SPI

The SPI interface consists of pins 53 (SPI_SDO), 54 (SPI_SDIO), 55 (SPI_CLK), and 56 (SPI_CSB). SPI_SDIO is used for the serial data input to program all required registers. SPI_CSB is an enable signal that must be asserted low during the entire serial data writing process. SPI_CLK stores data inputs at the rising clock edge and reads data out on the falling clock edge.

Description	**DAC-FPGA line count**
I & Q Digital lines	32
Reset	1
CLK	2
Total	**35**

Figure 4 DAC FPGA line count

2.6.3 Power Conditioning

The data has separate 3.3V analog and 3.3V digital IO power.

2.6.3.1 Vadd

The Analog power is isolated from the digital power VCC3.3 by a ferrite bead. It is desired to obtain the highest impedance device as possible with the lowest DC resistance. The high impedance reduces voltage fluctuations from the VCC.3 from entering the Analog section of the DAC and visa-versa (the reason for using the bead). A high impedance over a broad range is desired since switching regulator ripple is typically in the 100kHz-700kHz range while digital clock noise second harmonic can be around 350MHz. The DC resistance of the ferrite bead also lowers the DC voltage delivered to the DAC (undesirable).

From the DAC specification sheet:

- 76mA max Iadd
- 3.1V min Vacc

A TDK MMZ2012R102A has impedance @ 100MHz of 1.0 kohm and a maximum DC resistance of 0.35ohm (0.05ohm is typical).

Assuming a mean VCC3.3 of 3.3V and a ripple voltage of 100mV (typical maximum ripple of switching regulators) the DC voltage drops by 0.35ohm * 76mA = 26.6mV. The ripple voltage drops to (3.3V/0.076A = 42ohm load), 100mV * (42ohm/(42ohm+~75ohm)) = 35.9mV.

With a voltage drop of 26.6mV the Vadd becomes 3.3-0.0266 = 3.2734V. This is 0.1734V above the 3.1 minimum Vadd needed by the DAC.

2.6.3.2 Vclkcc

The clock Vcc is isolated from the Analog side and the digital side by a ferrite bead.

Use the same bead as with the RocketIO ferrites.

Current through the bead is the Iclkcc and the current through the two parallel termination resistors = (10mA + 2 * 3.3V/200ohm) = 43mA. The voltage drop through the bead is 42mA * 0.36ohm = 15.1mV. This gives a Vclkcc of 3.3V-0.0151mV = 3.2849V. This is above the 3.1V Vclkccc minimum.

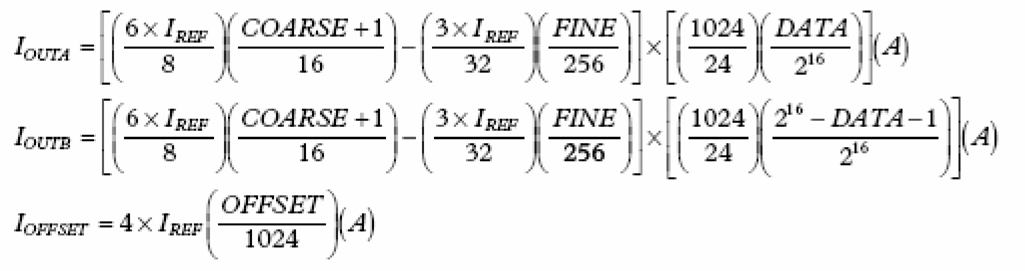
2.6.4 DAC Configuration Via SPI

The SPI interface is used to program thirteen registers, each having a one bye capacity. A comprehensive chart of the SPI port registers can be found on page 14 of the AD9777 datasheet. Nearly all of the bits are left at default settings that are clearly explained in the datasheet. The following is a brief description of the bits that were not left at default.

Address 00h bit 2: This bit determines whether the reference current I_{REF} is set independently for both the in-phase and quadrature output channels or by one setting for both channels. The default of logic ‘0’ uses two separate pins, 60 and 59, and their corresponding resistors to set the reference current values.

Address 01h bits 6 and 7: The datasheet does not specify whether these two bits have a default value. These bits control the interpolation rate: 00 for 1x, 01 for 2x, 10 for 4x, and 11 for 8x. For simplicity, the phase 1 implementation of this design will use 1x interpolation.

The SPI registers allow for gain adjustment and DC offset in terms of the current supplied by the differential outputs. The equations below are copied from page 16 of the AD9777 datasheet. I_{OUTA} and I_{OUTB} represent the differential in-phase or quadrature analog outputs. COARSE, FINE OFFSET, and DATA are 4, 8, 10, and 16-bit straight binary numbers, respectively.



$$I_{OUTA} = \left[\left(\frac{6\times I_{REF}}{8}\right)\left(\frac{COARSE+1}{16}\right)-\left(\frac{3\times I_{REF}}{32}\right)\left(\frac{FINE}{256}\right)\right]\times\left[\left(\frac{1024}{24}\right)\left(\frac{DATA}{2^{16}}\right)\right](A)$$

$$I_{OUTB} = \left[\left(\frac{6\times I_{REF}}{8}\right)\left(\frac{COARSE+1}{16}\right)-\left(\frac{3\times I_{REF}}{32}\right)\left(\frac{FINE}{256}\right)\right]\times\left[\left(\frac{1024}{24}\right)\left(\frac{2^{16}-DATA-1}{2^{16}}\right)\right](A)$$

$$I_{OFFSET} = 4\times I_{REF}\left(\frac{OFFSET}{1024}\right)(A)$$

We want a full 20mA output when the Data=32767. We can get that by using Rset=1.96kOhm. This gives us an Iset of 1.2V/1.96kOhm = 0.6122mAmp. The full scale current is then 32 * 0.6122 mA = 19.59 mA. Maximum Ifullscale allowed is 20mA.

We get the full current output for COURSE=15, FINE=0 at DATA=32767.

Address 00h:

- SDIO always input
- MSB first
- 2R Mode for reference current

- Normal = 04h
- Sleep = 14h
- PowerDown = 0Bh
- Reset = 24h.

Address 01h:
- No modulation
- No Zero stuffing
- Pin 8 is a PLL lock indicator

- 1x interpolation = 04h
- 2x interpolation = 44h
- 4x interpolation = 84h
- 8x interpolation = B4h

Address 02h: 00h

- Two's compliment inputs
- Two port input mode

Address 03h: 00h

VCO clock/1.

Address 04h: 80h
- Enable PLL
- Automatic Charge Pump Control

Address 05h: 00h
- IDAC No FINE gain.

Address 06h: 0Fh
- IDAC Full COARSE gain.

Address 07h, 08h: 000h
- IDAC No OFFSET adjustment

Address 09h: 00h
- QDAC No FINE gain.

Address 0Ah: 0Fh
- QDAC Full COARSE gain.

Address 0Bh, 0Ch: 00h
- QDAC No OFFSET adjustment

To fully program the DAC we send 7 transfers of 3 bytes each (3 bytes was chosen because that is the size of the registers on the Local Oscillators on the RF board. This simplifies the first configuration of the FPGA where the SPI data is hard coded into the FPGA.

DAC Addresses	**Value(s) 24bits**
00h, 01h	2004B4h
02h, 03h	220000h
04h, 05h	248000h
06h, 07h	260F00h
08h, 09h	280000h
0Ah, 0Bh	2A0F00h
0C, 0Dh	2C0000h

2.7 *Analog to Digital Converter (ADC)*

The Digital Board uses a dual Linear Techcnologies LTC2284 14bit ADC to convert the base-band analog receive signal from the RF board into a digital signal. The ADC can sample at up to 105MSPS.

The output of the ADCs feeds into the FPGA. The FPGA supplies the sample clock (encode signal) to a LVDS to CMOS converter that then feeds the ADC.

2.7.1 ADC Output Signals and Mode (Data Format)

The Data and OVR lines from the ADC run directly to the FPGA through series termination resistors. The series termination resistors must be placed as close to the corresponding ADCs pins as possible.

The Power dissipated in the Rs series termination resistor of the Data signals is:

Pd = (IpeakLoad**2) * Rs

Rs = ~33 ohm (Zo=75 ohm, Ro of CMOS driver = 7 + 43ohm),

IpeakLoad = Vddo / (2 * Zo) = 1.5V / (2 * 75ohm) = 0.01A (see lvcmos_power_dissipation.pdf).

So Pd = (0.01A ** 2) * 33ohm = 3.3mW. This is low enough to use 1/16W resistors.

The Data Format of the ADC output is set to 2’s compliment by tying the MODE line to 2/3 Vdd.

2.7.2 ADC Clock(Encode)

The Encode signal from the FPGA is a pair of LVCMOS_15 lines (NOT LVDCI_25) from Bank 1. The pair is driven differentially (one line has an inverter on it in the FPGA). Care must be taken to ensure that the two clock outputs have the same timing.

The differential clock lines have termination to reduce line ringing. The termination method is parallel with a capacitor coupling the AC to ground between the two parallel resistors.

The differential pair is connected to a LVDS to CMOS converter. The output of the converted is tied to both A and B clock pins. The output of the convert is placed as close as possible to the A and B clock pins so that no termination is required.

2.7.3 Analog Input

The LTC2284 has a common mode offset Vcm of 1.5V with a Vp-p of 2V maximum.

The 2Vp-p input range is set by connecting each Sense input to AVcc (Vdd).

The Vcm output of the ADC must be used to set the common mode offset of the device on the RF board that produces the differential baseband signal. The Vcm(Vref) voltage is present on the RF Digital Interface connector.

The datasheet for the ADC shows a 24 (standard 5% value) ohm input series resistor (Rs) to each analog input for some measure of isolation.

2.7.4 AVcc Power Conditioning

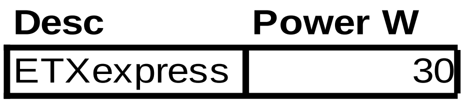
The AVcc power of the ADCs are conditioned with a ferrite bead. The bead is a TDK MMZ2012R102A. DC resistance is 0.35 ohm maximum (0.05 ohm typical). With a maximum ADC I AVcc of 180mA the voltage drop across the bead is 0.180A * 0.35 ohm = 0.063V. Power

This section contains the estimated power used by the Digital Board. The Summary section provides a summary for the total maximum sustained power used by the board. This is not the typical power usage.

2.8 Power Usage Summary

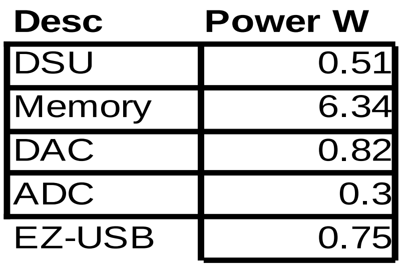
The Digital Board requires 5V, 3.3V, 2.5V and 1.5V inputs from the Power board. The following tables summarize the maximum power usages for these voltage levels.

Table 34 5.0 V Maximum Power Usage.



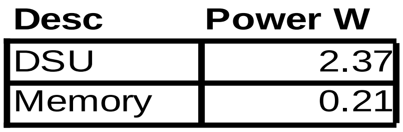
Desc	Power W
ETXexpress	30

Table 35 3.3V Maximum Power Usage.



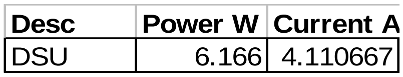
Desc	Power W
DSU	0.51
Memory	6.34
DAC	0.82
ADC	0.3
EZ-USB	0.75

Table 36 2.5V Maximum Power Usage



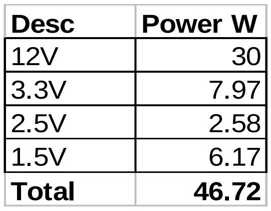
Desc	Power W
DSU	2.37
Memory	0.21

Table 37 Maximum 1.5V Power Usage



Desc	Power W	Current A
DSU	6.166	4.110667

Table 38 Total Maximum Power Usage



Desc	Power W
12V	30
3.3V	7.97
2.5V	2.58
1.5V	6.17
Total	**46.72**

2.8.1 ETXeXpress Power Usage

The ETXeXpress requires regulated 10.8 – 13.2V power at 2.5A (30Watts).

Empirical measurements show that the current into the ETXeXpress shows TBS current draw.

Description	Voltage	Current	Power
ETXeXpress Maximum	12.0V	2.5A	30W
ETXeXpress Typical	12.0V	2.5A	30W

Table 39 ETXeXpress Power Usage

2.8.2 EZ-USB Power Usage

Description	Voltage	Current	Power
EZ-USB Maximum	3.3V	85mA	280mW
EZ-USB Typical	3.3V	50mA	165W

Table 40 EZ-USB Power Usage

2.8.3 DSU

From the data sheet for the FPGA it looks like the worst-case power consumption is at power startup.

Table 41 FPGA Power On Power Usage

Description	Voltage	Current	Power
Vcco	3.3	100mA	0.33W
VccAUX	2.5	250mA	0.625W
VccINT	1.5	600mA	0.90W

Total	1.850W

The maximum heat that can be dissipated by the bare FG676 package is 3.0 watts in ambient temperature of 50 degrees C. Adding a simple heat spreader allows dissipation of up to 6 watts. The most that can be dissipated is with a finned heat sink is up to 10W.

From www.xilinx.com/cgi-bin/power_tool/power_Virtex2p the power used by the FPGA can be roughly estimated. In the following subsection the power for various aspects of the FPGA were estimated. The results are summaries in the following table:

Table 42 DSU Maximum Power Usage Summary

Description	**Max Power Used Vccint mW**	**Max Power Used Vcco (3.3V) mW**	**Max Power Used Vcco (2.5V) mW**	**Total Power mW**	
CLBs	2583	0			
Block SelectRAM	0	0			
Block Multipler	2534	0			
Processor	668	0			
Clock DCM	9	0			
Bank0 I/O	4	42			
Bank1 I/O	37	439			
Bank1,2,6,7 I/O	328		1948		
Bank4&5 I/O	3	29			
Vccaux Quiescent			417		
MAX1618		3			
Total	**6166**	**513**	**2365**	**9044**	

2.8.3.1 CLB Power Usage

Assume that 65% of the CLBs are used. 65% of 9280 slices of Virtex II Pro P20 = 6032. Assume that the clock frequency of the CLBs averages out to be twice the 80Mhz input/output data rate.

Table 43 CLB Power Usage

Desc	Freq MHz	Num of Slices	Num of FF	Num of LUT Shift Reg	Num of LUT Select RAM	Avg Toggle Rate	Amount of Routing	Vccint mW
Summary	160MHz	6032	9000	5000	2000	25	Low	2583

2.8.3.2 Block Multiplier Power Usage

The usage of the Block Multipliers is a wild guess at this time. Assume the following:

- 64 point FFT. Requires 32 radix 2 butterflies. 1, 2, 4 or 8 multipliers per butterfly.
- 64 point IFFT. Requires 32 radix 2 butterflies. 1, 2, 4 or 8 multipliers per butterfly.
- DSP Windowing. Requires 1 multiplier.

The Virtex II Pro P20 has 88 18x18 multipliers.

To have 1 FFT and 1 IFFT operate simultaneously and independently the IFFT and FFT can be configured to use 32 multipliers each. In a 64 point there are 64 * 4 * 6 = 1536 multiplies. Each multiplier then has 1536/32 = 48 multiplies. The FFT must be done in 1/80Mhz (sample Rate) * 64 = 800nS. Assuming that multiplies take up 25% of the FFT processing time then each multiply must occur in 800/48/4 = 4.167 nS. The Data frequency would be 240 Mhz.

Table 44 Multiplier Power Usage

Desc	Num Multipliers	Data Freq MHz	Data Toggle Rate	Vccint mW
FFT&IFFT	64	240	Medium	2534
Total				2534

2.8.3.3 405EP Power Usage

Assume that a –5 speed Virtex II is used. The max CPU speed for the –6 is 300MHz. The max CPU speed for the –5 speed is 300MHz.

Assume that for peak power both processors are running at 300MHz. Try to operate the OCM (On Chip Memory) at full rate of 300Mhz. The PLB (Processor Local Bus) runs at the SRAM data rate of 300MHz. The DCR (Device Control Register) runs at 133MHz.

Table 45 405EP Power Usage

Desc	Proc Freq MHZ	PBL Freq MHz	DCR Freq MHZ	OCM Freq MHz	Vccint mW
405EP 0	300	300	133	300	334
405EP 1	300	300	133	300	334
Total					668

2.8.3.4 DCM Power Usage

For now take a guess at the number of clocks needed.

- A 80 Mhz clock is needed for ADCs and DAC. This can be generated from the GCLK (16 MHz) using DCM low frequency mode and the CLKFX and CLKFX180 DCM outputs. The multiplier is 5 and the divisor is 1.
- A 300MHz clock is needed to power the 405EP CPUs. The highest frequency possible with the 16Mhz global clock would be 240MHz (from spec sheet for –6 speed Virtex Pro II FPGA). This is not high enough to fully utilize the 405Eps (running at 350Mhz (-6) or 300MHz(-5 speed). One way to get the 300Mhz clock is to use the 80Mhz TXRX clock and two DCMs. The first DCM inputs the 80Mhz clock, multiplies by 15 and divides by 8 to get 150Mhz. The 150Mhz clock is then run through second DCM. Its CLK2X output provides the 300Mhz clock for the 405EP. (The 350Mhz clock can be obtainted from in intermiate frequency of 175Mhz.
- 500kHz is used for the SPI bus. This can be obtained by dividing the GCLK (16MHz) by 32.

Table 46 DCM Power Usage

Desc	DCM Freq MHz	DCM Mode	DCM mW
GCLK(16Mhz)-> 80Mhz	16	Low	0
80Mhz->150Mhz	80	Low	3
150Mhz->300Mhz	150	Low	6
GCLK(16Mhz)-> 500kHz	16	Low	0
Total			9

2.8.3.5 Input/Output Power

Assume that transmit and receive clocks are run matched and run at 80MHz.

Bank0 ADC Lines

Since this bank does not use DCI two series source termination resistors are added to the SRAM3 A0 and A1 lines outside of the FPGA. The power dissipated by these resistors must be included.

The power dissipated by the parallel sink termination on the clock lines is found in the DAC, ADC and Memory power usage sections.

Table 47 Bank0 (ADC) Power Usage

Desc	Freq (MHz)	IO Standard	Num Inputs	Num Outputs	Avg IOB Toggle Rate	Avg IOB Enable Rate	Avg Ouput Load pF	IOB Registers	Vccint mW
Rx Data	80	LVCMOS33_24	28	0	25	100	10	SDR	4
Clocks	80	LVCMOS33_24	0	4	100	100	10	SDR	0
Data Ready	80	LVCMOS33_24	1	0	50	100	10	SDR	0
OVR	80	LVCMOS33_24	2	0	1	100	10	SDR	0
SRAM3A0,1	133	LVCMOS33_24	0	2	1	100	10	SDR	0
Total									4

Table 48 Bank1 (DAC) Power Usage

Desc	Freq (MHz)	IO Standard	Num Inputs	Num Outputs	Avg IOB Toggle Rate	Avg IOB Enable Rate	Avg Ouput Load pF	IOB Registers	Vccint mW
DAC Data	80	LVDCI_33	0	32	25	100	10	SDR	13
DAC Clk	80	LVCMOS33_24	0	2	100	100	10	SDR	0
DAC Rst	80	LVDCI_33	0	1	1	100	10	SDR	12
SRAM0A0,1	133	LVDCI_33	0	2	1	100	10	SDR	12
Total									37

Table 49 Bank2 (SRAM0) Power Usage 2.5V

Desc	Freq (MHz)	IO Standard	Num Inputs	Num Outputs	Avg IOB Toggle Rate	Avg IOB Enable Rte	Avg Output Load pF	IOB Registers	Vccint mW
SRAM0 A2-17	133	LVDCI_33(50)	0	16	25	100	10	SDR	13
SRAM0 D0-31	133	LVDCI_33(50)	32	32	25	50	10	SDR	21
SRAM0 BW0-3	133	LVDCI_33(50)	0	4	25	100	10	SDR	12
SRAM0 CLK	133	LVCMOS33_24	0	1	100	100	10	SDR	0
SRAM0_RDWR	133	LVDCI_33(50)	0	1	25	100	10	SDR	12
SRAM0_CE	133	LVDCI_33(50)	0	1	1	100	10	SDR	12
SRAM0_ADV/LD	133	LVDCI_33(50)	0	1	1	100	10	SDR	12
Total									82

Bank 3 (SRAM1) Power Usage is identical to Bank2.

Table 50 Bank4-5 (CPH, SPI) Power Usage

Desc	Freq (MHz)	IO Standard	Num Inputs	Num Outputs	Avg IOB Toggle Rate	Avg IOB Enable Rate	Avg Output Load pF	IOB Registers	Vccint mW
CPH Addr	44	LVCMOS33_24	20	0	25	100	10	SDR	1
CPH Data	44	LVCMOS33_24	16	16	25	50	10	SDR	2
CPH_Clk	44	LVCMOS33_24	1	0	100	100	10	SDR	0
CPH Ready	44	LVCMOS33_24	0	1	10	100	10	SDR	0
CPH CE	44	LVCMOS33_24	1	0	10	100	10	SDR	0
CPH RDWR	44	LVCMOS33_24	1	0	25	100	10	SDR	0
CPH WBE	44	LVCMOS33_24	1	0	25	100	10	SDR	0
FPGA Intr	0	LVCMOS33_24	0	1	0	100	10	SDR	0
SRAM A0,1	133	LVCMOS33_24	0	4	25	100	10	sdr	0
SPI CLK	0.4	LVCMOS33_24	0	1	100	1	50	SDR	0
SPI MISO,MOSI	0.4	LVCMOS33_24	1	1	50	1	50	SDR	0
SPI Enables	0.4	LVCMOS33_24	0	10	1	1	10	SDR	0
Global Clk	16	LVCMOS33_24	1	0	100	100	10	SDR	0

Bank6 (SRAM2) Power Usage is identical to Bank2.

Bank7 (SRAM3) Power Usage is identical to Bank2.

2.8.4 Memory

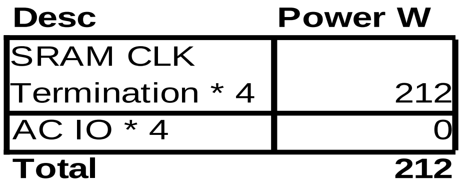
The memory consists of 4 Cypress CY7C1354A-166MGC ICs. The data sheet for this chip shows a maximum current draw of 480mA when operating at 166MHz with a typical current draw of 200mA. When not operating, but with the clock running, the Vcc current is 200mA maximum with 50mA typical. The Vccq voltage is 2.5V.

Table 51 Memory 3.3V Power Usage

Desc	Power	Current
SRAM Max * 4	6.336W	1920mA
SRAM Typical * 4	2.640W	800mA

The clocks to the memories are parallel destination terminated to obtain the best clock. The DC current draw of a clock termination is 2.3V / 100 ohm = 23mA. The power dissipated is 53mW. For 4 memory devices the power in the parallel clock termination is 212mW.

Table 52 Memory 2.5V Maximum Power Usage



Desc	Power W
SRAM CLK Termination * 4	212
AC IO * 4	0
Total	**212**

2.8.5 DAC

The DAC (AD_9777), in its initial usage is expected to run with a data input rate of 5MHz and a data output rate of 40MHz (interpolation of 8x). The higher the input data rate and interpolation rate is the higher the power usage is. The highest expected future data rate input is 100MHz with an interpolation rate of 2x. There is no intention of using the internal modulator of the DAC.

The data in the following table is derived from figures 15, 16 and 17 of the AD9777 datasheet for the 100MHz input rate and 2x interpolation. These numbers are being used so that there will be no need to redesign the power system when the DAC is finally run at this speed.

Table 53 DAC Power Usage

Description	**Voltage**	**Current**	**Power**
AVdd max	3.3	73mA	241mW
DVdd max	3.3	160mA	528mW
ClkVdd max	3.3	16mA	51mW
Total			0.821W

2.8.6 ADC

There is a dual Analog to Digital converter for the baseband RF signal to digital conversion. The device is a Linear Technologies LTC2284. The maximum sample speed is 105Msps.

There are two Analog to Digital converters. One for the I receive channel and one for the Q receive channel. Each ADC is an Analog Devices AD6645. The maximum speed is 105MSPS.

Table 54 ADC Power Usage

Description	Voltage	Current	Power

AVcc maximum	3.3	210mA	693mW
AVcc typical	3.3	180mA	594mW
DVcc maximum	3.3	?	?
DVcc typical	3.3	13mA	60mW

2.8.7 Compact Flash Power Usage

The Compact Flash is a Hitachi 6GB Microdrive in a CF+ II package, model #HMS3060606006CF00.

Description	**Voltage**	**Current**	**Power**
Vdd max	3.3	230mA	759mW
Vdd standby	3.3	13mA	42.9mW

2.9 Interfaces

2.9.1 FPGA Interface

This section contains the pin assignments for the FPGA. The pin assignments were made while considering the pin layout of the devices to be interfaced with and the layers that the signals would have to be placed on.

See the layout section for the reasoning behind the layout of the signals.

2.9.1.1 COMeXpress PCI

The COMexpress PCI interface is connected to FPGA banks 4 and 5. The FPGA only acts as PCI target so many of the PCI signals are not used. The FPGA is given PCI signals for PCI Device 0.

The following lists how the COMexpress PCI signals are NOT used:

- INTB#, INTC#, INTD# – Only the INTA signal is used
- REQ0:3 – not needed by a target only device
- GNT0:3 – not needed by a target only device
- LOCK# - not needed by non memory target only device

The COMexpress specification [1] identifies PCI_AD[20] as the IDSEL signal for PCI Device 0.

The PCI_M66EN shall be pulled go GND by a 0ohm resistor. The resistor can be removed for 66MHz operation.

2.9.1.2 Bank 0

Bank 0 is primarily used to connect to the DAC. The IO voltage on this bank is CMOS 3.3V. DCI is used on this bank.

Table 55 FPGA Bank 0 Pin Assignments

Signal Name	FPGA Bin	IO Standard
DAC_I_LVC_0	U100-H10	LVDCI_33
DAC_I_LVC_1	U100-D9	LVDCI_33
DAC_I_LVC_2	U100-F9	LVDCI_33
DAC_I_LVC_3	U100-E9	LVDCI_33
DAC_I_LVC_4	U100-9G	LVDCI_33
DAC_I_LVC_5	U100-E8	LVDCI_33
DAC_I_LVC_6	U100-D7	LVDCI_33
DAC_I_LVC_7	U100-F7	LVDCI_33
DAC_I_LVC_8	U100-E7	LVDCI_33
DAC_I_LVC_9	U100-G7	LVDCI_33
DAC_I_LVC_10	U100-D6	LVDCI_33
DAC_I_LVC_11	U100-E6	LVDCI_33
DAC_I_LVC_12	U100-B13	LVDCI_33
DAC_I_LVC_13	U100-C12	LVDCI_33
DAC_I_LVC_14	U100-C10	LVDCI_33
DAC_I_LVC_15	U100-C9	LVDCI_33
DAC_Q_LVC_0	U100-J12	LVDCI_33
DAC_Q_LVC_1	U100-G11	LVDCI_33
DAC_Q_LVC_2	U100-H11	LVDCI_33

DAC_Q_LVC_3	U100-H9	LVDCI_33
DAC_Q_LVC_4	U100-C13	LVDCI_33
DAC_Q_LVC_5	U100-E13	LVDCI_33
DAC_Q_LVC_6	U100-D13	LVDCI_33
DAC_Q_LVC_7	U100-F13	LVDCI_33
DAC_Q_LVC_8	U100-D12	LVDCI_33
DAC_Q_LVC_9	U100-F12	LVDCI_33
DAC_Q_LVC_10	U100-E12	LVDCI_33
DAC_Q_LVC_11	U100-G12	LVDCI_33
DAC_Q_LVC_12	U100-E11	LVDCI_33
DAC_Q_LVC_13	U100-F11	LVDCI_33
DAC_Q_LVC_14	U100-D10	LVDCI_33
DAC_Q_LVC_15	U100-E10	LVDCI_33
DAC_CLK_LVC_P	U100-C7	LVCMOS33
DAC_CLK_LVC_N	U100-B8	LVCMOS33
DAC_RST_LVC_H	U100-H12	LVDCI_33
DAC_LOCK_LVC_H	U100-A8	LVCMOS33
SRAM3_Addr_LVC_0	U100-G8	LVCMOS33
SRAM3_Addr_LVC_1	U100-H8	LVCMOS33
SRAM3_Z_LVC	U100-F8	LVCMOS33

2.9.1.3 Bank 1

Bank 1 connects to the dual Analog to Digital converter and to the status LEDs (indirectly). It does not use Digital Controlled Impedance since there are only 4 outputs (clocks).

Note that the LSB of the I and Q data is numbered ‘2’. The ADC only supplies 14 bits but the FPGA processes 16 bit words so the MSB of the ADC (13) is assigned to FPGA MSB 15. Inside the FPGA bits 0 and 1 must be tied LOW (or HIGH).

Table 56 FPGA Bank 1 Pin Assignments

Signal Name	FPGA Pin	IO Standard
ADC_I_LVC_2	U100-D17	LVCMOS33
ADC_I_LVC_3	U100-H17	LVCMOS33
ADC_I_LVC_4	U100-E17	LVCMOS33
ADC_I_LVC_5	U100-F18	LVCMOS33
ADC_I_LVC_6	U100-D18	LVCMOS33
ADC_I_LVC_7	U100-E18	LVCMOS33
ADC_I_LVC_8	U100-G18	LVCMOS33
ADC_I_LVC_9	U100-E19	LVCMOS33
ADC_I_LVC_10	U100-F20	LVCMOS33
ADC_I_LVC_11	U100-D20	LVCMOS33
ADC_I_LVC_12	U100-G20	LVCMOS33
ADC_I_LVC_13	U100-E20	LVCMOS33
ADC_I_LVC_14	U100-E21	LVCMOS33
ADC_I_LVC_15	U100-D21	LVCMOS33
ADC_Q_LVC_2	U100-C14	LVCMOS33
ADC_Q_LVC_3	U100-E14	LVCMOS33
ADC_Q_LVC_4	U100-D14	LVCMOS33
ADC_Q_LVC_5	U100-F14	LVCMOS33
ADC_Q_LVC_6	U100-J15	LVCMOS33
ADC_Q_LVC_7	U100-G16	LVCMOS33
ADC_Q_LVC_8	U100-H16	LVCMOS33
ADC_Q_LVC_9	U100-H18	LVCMOS33
ADC_Q_LVC_10	U100-D15	LVCMOS33

ADC_Q_LVC_11	U100-F15	LVCMOS33
ADC_Q_LVC_12	U100-E15	LVCMOS33
ADC_Q_LVC_13	U100-G15	LVCMOS33
ADC_Q_LVC_14	U100-E16	LVCMOS33
ADC_Q_LVC_15	U100-F16	LVCMOS33
ADC_I_OVR_LVC_H	U100-A19	LVCMOS33
ADC_Q_OVR_LVC_H	U100-H15	LVCMOS33
ADC_RDY_LVC_H	U100-C15	LVCMOS33
ADC_I_CLK_LVC_P	U100-B19	LVCMOS33
ADC_I_CLK_LVC_N	U100-C20	LVCMOS33
ADC_Q_CLK_LVC_P	U100-C17	LVCMOS33
ADC_Q_CLK_LVC_N	U100-C18	LVCMOS33
GCLK_LVC	U100-B14	LVCMOS33
SRAM0_Addr_LVC_0	U100-G19	LVCMOS33
SRAM0_Addr_LVC_1	U100-H19	LVCMOS33
SRAM0_Z_LVC	U100-F19	LVCMOS33

2.9.1.4 Bank

The Bank 2 pins are dedicated to SRAM0.

Table 57 Bank 2 Pin Assignments

Signal Name	**FPGA Pin**	**IO Standard**
SRAM0_ADDR_LVC_2	U100-N19	LVDCI_25
SRAM0_ADDR_LVC_3	U100-N23	LVDCI_25
SRAM0_ADDR_LVC_4	U100-N22	LVDCI_25
SRAM0_ADDR_LVC_5	U100-N25	LVDCI_25
SRAM0_ADDR_LVC_6	U100-N18	LVDCI_25

SRAM0_ADDR_LVC_7	U100-M23	LVDCI_25
SRAM0_ADDR_LVC_8	U100-M21	LVDCI_25
SRAM0_ADDR_LVC_9	U100-N21	LVDCI_25
SRAM0_ADDR_LVC_10	U100-M22	LVDCI_25
SRAM0_ADDR_LVC_11	U100-M26	LVDCI_25
SRAM0_ADDR_LVC_12	U100-L21	LVDCI_25
SRAM0_ADDR_LVC_13	U100-G21	LVDCI_25
SRAM0_ADDR_LVC_14	U100-D25	LVDCI_25
SRAM0_ADDR_LVC_15	U100-F21	LVDCI_25
SRAM0_ADDR_LVC_16	U100-E23	LVDCI_25
SRAM0_ADDR_LVC_17	U100-F22	LVDCI_25
SRAM0_DATA_LVC_0	U100-E25	LVDCI_25
SRAM0_DATA_LVC_1	U100-F25	LVDCI_25
SRAM0_DATA_LVC_2	U100-E26	LVDCI_25
SRAM0_DATA_LVC_3	U100-F26	LVDCI_25
SRAM0_DATA_LVC_4	U100-G25	LVDCI_25
SRAM0_DATA_LVC_5	U100-G26	LVDCI_25
SRAM0_DATA_LVC_6	U100-H25	LVDCI_25
SRAM0_DATA_LVC_7	U100-D26	LVDCI_25
SRAM0_DATA_LVC_8	U100-H26	LVDCI_25
SRAM0_DATA_LVC_9	U100-J26	LVDCI_25
SRAM0_DATA_LVC_10	U100-J25	LVDCI_25
SRAM0_DATA_LVC_11	U100-K25	LVDCI_25
SRAM0_DATA_LVC_12	U100-K26	LVDCI_25
SRAM0_DATA_LVC_13	U100-L25	LVDCI_25

SRAM0_DATA_LVC_14	U100-M25	LVDCI_25
SRAM0_DATA_LVC_15	U100-L26	LVDCI_25
SRAM0_DATA_LVC_16	U100-M19	LVDCI_25
SRAM0_DATA_LVC_17	U100-M18	LVDCI_25
SRAM0_DATA_LVC_18	U100-M20	LVDCI_25
SRAM0_DATA_LVC_19	U100-K22	LVDCI_25
SRAM0_DATA_LVC_20	U100-J20	LVDCI_25
SRAM0_DATA_LVC_21	U100-L20	LVDCI_25
SRAM0_DATA_LVC_22	U100-J22	LVDCI_25
SRAM0_DATA_LVC_23	U100-L24	LVDCI_25
SRAM0_DATA_LVC_24	U100-J24	LVDCI_25
SRAM0_DATA_LVC_25	U100-J19	LVDCI_25
SRAM0_DATA_LVC_26	U100-J23	LVDCI_25
SRAM0_DATA_LVC_27	U100-H22	LVDCI_25
SRAM0_DATA_LVC_28	U100-H20	LVDCI_25
SRAM0_DATA_LVC_29	U100-H21	LVDCI_25
SRAM0_DATA_LVC_30	U100-L19	LVDCI_25
SRAM0_DATA_LVC_31	U100-G23	LVDCI_25
SRAM0_BW_LVC_L_0	U100-G22	LVDCI_25
SRAM0_BW_LVC_L_1	U100-K23	LVDCI_25
SRAM0_BW_LVC_L_2	U100-K24	LVDCI_25
SRAM0_BW_LVC_L_3	U100-J21	LVDCI_25
SRAM0_CLK_LVC	U100-G24	LVCMOS25
SRAM0_RW_LVC	U100-K19	LVDCI_25
SRAM0_CE_LVC_L	U100-L22	LVDCI_25

SRAM0_ADV/LD_LVC	U100-N24	LVDCI_25

2.9.1.5 Bank 3

Bank 3 connects to a 256Kx32 bit Synchronous Static Ram device. Lines A0, A1 and Z for the device come from bank 4.

Table 58 Bank 3 Pin Assignments

Signal Name	FPGA Pin	IO Standard
SRAM1_ADDR_LVC_2	U100-P25	LVDCI_25
SRAM1_ADDR_LVC_3	U100-P22	LVDCI_25
SRAM1_ADDR_LVC_4	U100-P23	LVDCI_25
SRAM1_ADDR_LVC_5	U100-P19	LVDCI_25
SRAM1_ADDR_LVC_6	U100-R23	LVDCI_25
SRAM1_ADDR_LVC_7	U100-P18	LVDCI_25
SRAM1_ADDR_LVC_8	U100-R26	LVDCI_25
SRAM1_ADDR_LVC_9	U100-R22	LVDCI_25
SRAM1_ADDR_LVC_10	U100-P21	LVDCI_25
SRAM1_ADDR_LVC_11	U100-R21	LVDCI_25
SRAM1_ADDR_LVC_12	U100-T21	LVDCI_25
SRAM1_ADDR_LVC_13	U100-AC25	LVDCI_25
SRAM1_ADDR_LVC_14	U100-AB23	LVDCI_25
SRAM1_ADDR_LVC_15	U100-AD25	LVDCI_25
SRAM1_ADDR_LVC_16	U100-AC24	LVDCI_25
SRAM1_ADDR_LVC_17	U100-AA22	LVDCI_25
SRAM1_DATA_LVC_0	U100-T19	LVDCI_25
SRAM1_DATA_LVC_1	U100-W20	LVDCI_25
SRAM1_DATA_LVC_2	U100-W21	LVDCI_25

SRAM1_DATA_LVC_3	U100-W22	LVDCI_25
SRAM1_DATA_LVC_4	U100-V23	LVDCI_25
SRAM1_DATA_LVC_5	U100-V19	LVDCI_25
SRAM1_DATA_LVC_6	U100-V23	LVDCI_25
SRAM1_DATA_LVC_7	U100-Y23	LVDCI_25
SRAM1_DATA_LVC_8	U100-V22	LVDCI_25
SRAM1_DATA_LVC_9	U100-V20	LVDCI_25
SRAM1_DATA_LVC_10	U100-T20	LVDCI_25
SRAM1_DATA_LVC_11	U100-U22	LVDCI_25
SRAM1_DATA_LVC_12	U100-18R	LVDCI_25
SRAM1_DATA_LVC_13	U100-R18	LVDCI_25
SRAM1_DATA_LVC_14	U100-R19	LVDCI_25
SRAM1_DATA_LVC_15	U100-T24	LVDCI_25
SRAM1_DATA_LVC_16	U100-R25	LVDCI_25
SRAM1_DATA_LVC_17	U100-T25	LVDCI_25
SRAM1_DATA_LVC_18	U100-U26	LVDCI_25
SRAM1_DATA_LVC_19	U100-U25	LVDCI_25
SRAM1_DATA_LVC_20	U100-V26	LVDCI_25
SRAM1_DATA_LVC_21	U100-V25	LVDCI_25
SRAM1_DATA_LVC_22	U100-W26	LVDCI_25
SRAM1_DATA_LVC_23	U100-T26	LVDCI_25
SRAM1_DATA_LVC_24	U100-W25	LVDCI_25
SRAM1_DATA_LVC_25	U100-Y26	LVDCI_25
SRAM1_DATA_LVC_26	U100-Y25	LVDCI_25
SRAM1_DATA_LVC_27	U100-AA26	LVDCI_25

SRAM1_DATA_LVC_28	U100-AA25	LVDCI_25
SRAM1_DATA_LVC_29	U100-AB26	LVDCI_25
SRAM1_DATA_LVC_30	U100-AB25	LVDCI_25
SRAM1_DATA_LVC_31	U100-AC26	LVDCI_25
SRAM1_BW_LVC_L_0	U100-V21	LVDCI_25
SRAM1_BW_LVC_L_1	U100-U24	LVDCI_25
SRAM1_BW_LVC_L_2	U100-U23	LVDCI_25
SRAM1_BW_LVC_L_3	U100-Y22	LVDCI_25
SRAM1_CLK_LVC	U100-Y24	LVCMOS25
SRAM1_RW_LVC	U100-U19	LVDCI_25
SRAM1_CE_LVC_L	U100-T22	LVDCI_25
SRAM1_ADV/LD_LVC	U100-P24	LVDCI_25

2.9.1.6 Bank 4

Bank 4 carries roughly half of the signals that are connected to the CPH (Cerfcube) plus SRAM1 A1, A0 and Z.

Table 59 FPGA Bank 4 Pin Assignments

Signal Name	FPGA Bin	IO Standard
SRAM1_Addr_LVC_0	U100-Y19	LVCMOS33
SRAM1_Addr_LVC_1	U100-W19	LVCMOS33
SRAM1_Z_LVC_H	U100-AA19	LVCMOS33
FPGA_BUSY_LVC_H	U100-AB22	LVCMOS33
FPGA_INITB_LVC_L	U100-AC22	LVCMOS33
FPGA_DONE_LVC_L	U100-AD23	LVCMOS33
FPGA_INTR_LVC_L	U100-AB20	LVCMOS33
FPGA_CCLK_LVC	U100-AE24	LVCMOS33

CPH_CLK_LVC	U100-AE19	LVCMOS33
CPH_RST_LVC_L	U100-W17	LVCMOS33
CPH_WBE_LVC_L	U100-AB19	LVCMOS33
CPH_DATA_LVC_7	U100-AB21	LVCMOS33
CPH_DATA_LVC_6	U100-AC21	LVCMOS33
CPH_DATA_LVC_5	U100-Y20	LVCMOS33
CPH_DATA_LVC_4	U100-AA20	LVCMOS33
CPH_DATA_LVC_9	U100-AC18	LVCMOS33
CPH_DATA_LVC_11	U100-AA18	LVCMOS33
CPH_DATA_LVC_13	U100-AB18	LVCMOS33
CPH_DATA_LVC_15	U100-Y18	LVCMOS33
CPH_ADDR_LVC_4	U100-AD14	LVCMOS33
CPH_ADDR_LVC_5	U100-AB14	LVCMOS33
CPH_ADDR_LVC_6	U100-AC14	LVCMOS33
CPH_ADDR_LVC_7	U100-AA14	LVCMOS33
CPH_ADDR_LVC_8	U100-AC15	LVCMOS33
CPH_ADDR_LVC_9	U100-AA15	LVCMOS33
CPH_ADDR_LVC_10	U100-AB15	LVCMOS33
CPH_ADDR_LVC_11	U100-19AF	LVCMOS33
CPH_ADDR_LVC_12	U100-15Y	LVCMOS33
CPH_ADDR_LVC_13	U100-18AD	LVCMOS33
CPH_ADDR_LVC_14	U100-16AB	LVCMOS33
CPH_ADDR_LVC_15	U100-17AD	LVCMOS33
CPH_ADDR_LVC_16	U100-16AA	LVCMOS33
CHP_ADDR_LVC_17	U100-15AD	LVCMOS33

CPH_ADDR_LVC_18	U100-17AC	LVCMOS33
CPH_ADDR_LVC_19	U100-14AE	LVCMOS33
CPH_ADDR_LVC_20	U100-17AB	LVCMOS33

2.9.1.7 Bank 5

Note that some of the pins in bank 5 are for SRAM2. This is because Bank 6 did not have enough pins for all of the SRAM pins. The SRAM2 pins put on this bank are the pins that are least likely to be used. The parity bits are not likely to be used for parity. It is unlikely that they will be used for other purposes either. If word all addressing is done on word boundaries then Addr 0 and 1 are not needed.

Table 60 Bank 5 Pin Assignments

Signal Name	FPGA Bin	IO Standard
SRAM2_Addr_LVC_0	U100-Y8	LVCMOS33
SRAM2_Addr_LVC_1	U100-W8	LVCMOS33
SRAM2_Z_LVC_H	U100-AA8	LVCMOS33
FPGA_CS_LVC_L	U100-AB5	LVCMOS33
CPH_RDWR_LVC	U100-AC5	LVCMOS33
CPH_DATA_LVC_0	U100-AB6	LVCMOS33
CPH_DATA_LVC_1	U100-AC6	LVCMOS33
CPH_DATA_LVC_2	U100-Y7	LVCMOS33
CPH_DATA_LVC_3	U100-AA7	LVCMOS33
CPH_DATA_LVC_8	U100-AE13	LVCMOS33
CPH_DATA_LVC_10	U100-AD12	LVCMOS33
CPH_DATA_LVC_12	U100-AD10	LVCMOS33
CPH_DATA_LVC_14	U100-AD9	LVCMOS33
CPH_ADDR_LVC_0	U100-AA13	LVCMOS33
CPH_ADDR_LVC_1	U100-AD13	LVCMOS33

CPH_ADDR_LVC_2	U100-AB13	LVCMOS33
CPH_ADDR_LVC_3	U100-AC13	LVCMOS33
SPI_CLK_LVC	U100-AB7	LVCMOS33
SPI_MISO_LVC	U100-AB9	LVCMOS33
SPI_MOSI_LVC	U100-AB8	LVCMOS33
SPI_EN_LVC_L_0	U100-Y9	LVCMOS33
SPI_EN_LVC_L_1	U100-AB12	LVCMOS33
SPI_EN_LVC_L_2	U100-W9	LVCMOS33
SPI_EN_LVC_L_3	U100-W11	LVCMOS33
SPI_EN_LVC_L_4	U100-Y11	LVCMOS33
SPI_EN_LVC_L_5	U100-AA12	LVCMOS33
SPI_EN_LVC_L_6	U100-AC12	LVCMOS33
SPI_EN_LVC_L_7	U100-V12	LVCMOS33
SPI_EN_LVC_L_8	U100-W12	LVCMOS33
SPI_EN_LVC_L_9	U100-V13	LVCMOS33
I2C_SCL_LVC	U100-AF8	LVCMOS33
I2C_SDA_LVC	U100-AE8	LVCMOS33
TP0_LVC	U100-AC9	LVCMOS33
TP1_LVC	U100-AA9	LVCMOS33
TP2_LVC	U100-AB10	LVCMOS33
TP3_LVC	U100-W10	LVCMOS33
TP4_LVC	U100-AC10	LVCMOS33
TP5_LVC	U100-AA11	LVCMOS33
TP6_LVC	U100-AB11	LVCMOS33
TP7_LVC	U100-Y12	LVCMOS33

GPS_PPS	U100-W13	LVCMOS33

2.9.1.8 Bank 6

Note that the SRAM2 CLK signal is on Mid layer 2 where there are few signals. This allows extra space to be placed between the CLK signal and adjacent signals on the same layer to prevent cross talk. On Mid layer 1 then there should be a gap between the two signals closest to the CLK signal to put as much distance between the CLK signal and the closest signals on Mid layer 2.

Table 61 Bank 6 Pin Assignments

Signal Name	FPGA Pin	IO Standard
SRAM2_ADDR_LVC_2	U100-P8	LVDCI25
SRAM2_ADDR_LVC_3	U100-P4	LVDCI25
SRAM2_ADDR_LVC_4	U100-P5	LVDCI25
SRAM2_ADDR_LVC_5	U100-P2	LVDCI25
SRAM2_ADDR_LVC_6	U100-P9	LVDCI25
SRAM2_ADDR_LVC_7	U100-R4	LVDCI25
SRAM2_ADDR_LVC_8	U100-R6	LVDCI25
SRAM2_ADDR_LVC_9	U100-P6	LVDCI25
SRAM2_ADDR_LVC_10	U100-R5	LVDCI25
SRAM2_ADDR_LVC_11	U100-R1	LVDCI25
SRAM2_ADDR_LVC_12	U100-T6	LVDCI25
SRAM2_ADDR_LVC_13	U100-AB4	LVDCI25
SRAM2_ADDR_LVC_14	U100-AC2	LVDCI25
SRAM2_ADDR_LVC_15	U100-AA5	LVDCI25
SRAM2_ADDR_LVC_16	U100-AC3	LVDCI25
SRAM2_ADDR_LVC_17	U100-AD2	LVDCI25

SRAM2_DATA_LVC_0	U100-AB2	LVDCI25
SRAM2_DATA_LVC_1	U100-AA2	LVDCI25
SRAM2_DATA_LVC_2	U100-AB2	LVDCI25
SRAM2_DATA_LVC_3	U100-AA1	LVDCI25
SRAM2_DATA_LVC_4	U100-Y2	LVDCI25
SRAM2_DATA_LVC_5	U100-Y1	LVDCI25
SRAM2_DATA_LVC_6	U100-W2	LVDCI25
SRAM2_DATA_LVC_7	U100-AC1	LVDCI25
SRAM2_DATA_LVC_8	U100-W1	LVDCI25
SRAM2_DATA_LVC_9	U100-V1	LVDCI25
SRAM2_DATA_LVC_10	U100-V2	LVDCI25
SRAM2_DATA_LVC_11	U100-U2	LVDCI25
SRAM2_DATA_LVC_12	U100-U1	LVDCI25
SRAM2_DATA_LVC_13	U100-T2	LVDCI25
SRAM2_DATA_LVC_14	U100-R2	LVDCI25
SRAM2_DATA_LVC_15	U100-T1	LVDCI25
SRAM2_DATA_LVC_16	U100-R8	LVDCI25
SRAM2_DATA_LVC_17	U100-R9	LVDCI25
SRAM2_DATA_LVC_18	U100-R7	LVDCI25
SRAM2_DATA_LVC_19	U100-U5	LVDCI25
SRAM2_DATA_LVC_20	U100-V7	LVDCI25
SRAM2_DATA_LVC_21	U100-T7	LVDCI25
SRAM2_DATA_LVC_22	U100-V5	LVDCI25
SRAM2_DATA_LVC_23	U100-T3	LVDCI25
SRAM2_DATA_LVC_24	U100-V3	LVDCI25

SRAM2_DATA_LVC_25	U100-V8	LVDCI25
SRAM2_DATA_LVC_26	U100-V4	LVDCI25
SRAM2_DATA_LVC_27	U100-W5	LVDCI25
SRAM2_DATA_LVC_28	U100-W7	LVDCI25
SRAM2_DATA_LVC_29	U100-W6	LVDCI25
SRAM2_DATA_LVC_30	U100-T8	LVDCI25
SRAM2_DATA_LVC_31	U100-Y4	LVDCI25
SRAM2_BW_LVC_L_0	U100-Y5	LVDCI25
SRAM2_BW_LVC_L_1	U100-U4	LVDCI25
SRAM2_BW_LVC_L_2	U100-U3	LVDCI25
SRAM2_BW_LVC_L_3	U100-V6	LVDCI25
SRAM2_CLK_LVC	U100-Y3	LVCMOS25
SRAM2_RW_LVC	U100-U8	LVDCI25
SRAM2_CE_LVC_L	U100-T5	LVDCI25
SRAM2_ADV/LD_LVC	U100-P3	LVDCI25

2.9.1.9 Bank 7

Note that the SRAM3 CLK signal is on Mid layer 2 where there are few signals as close to the edge of the FPGA as possible. This allows extra space to be placed between the CLK signal and adjacent signals on the same layer to prevent cross talk. On Mid layer 1 then there should be a gap between the two signals closest to the CLK signal to put as much distance between the CLK signal and the closest signals on Mid layer 2 to reduce crosstalk.

Table 62 Bank 7 Pin Assignments

Signal Name	**FPGA Pin**	**IO Standard**
SRAM3_ADDR_LVC_2	U100-N2	LVDCI25
SRAM3_ADDR_LVC_3	U100-N5	LVDCI25
SRAM3_ADDR_LVC_4	U100-N4	LVDCI25

SRAM3_ADDR_LVC_5	U100-N8	LVDCI25
SRAM3_ADDR_LVC_6	U100-M4	LVDCI25
SRAM3_ADDR_LVC_7	U100-N9	LVDCI25
SRAM3_ADDR_LVC_8	U100-M1	LVDCI25
SRAM3_ADDR_LVC_9	U100-M5	LVDCI25
SRAM3_ADDR_LVC_10	U100-N6	LVDCI25
SRAM3_ADDR_LVC_11	U100-M6	LVDCI25
SRAM3_ADDR_LVC_12	U100-L6	LVDCI25
SRAM3_ADDR_LVC_13	U100-D2	LVDCI25
SRAM3_ADDR_LVC_14	U100-G6	LVDCI25
SRAM3_ADDR_LVC_15	U100-F5	LVDCI25
SRAM3_ADDR_LVC_16	U100-E4	LVDCI25
SRAM3_ADDR_LVC_17	U100-F6	LVDCI25
SRAM3_DATA_LVC_0	U100-L8	LVDCI25
SRAM3_DATA_LVC_1	U100-H7	LVDCI25
SRAM3_DATA_LVC_2	U100-H6	LVDCI25
SRAM3_DATA_LVC_3	U100-H5	LVDCI25
SRAM3_DATA_LVC_4	U100-J4	LVDCI25
SRAM3_DATA_LVC_5	U100-J8	LVDCI25
SRAM3_DATA_LVC_6	U100-J3	LVDCI25
SRAM3_DATA_LVC_7	U100-G4	LVDCI25
SRAM3_DATA_LVC_8	U100-J5	LVDCI25
SRAM3_DATA_LVC_9	U100-J7	LVDCI25
SRAM3_DATA_LVC_10	U100-L7	LVDCI25
SRAM3_DATA_LVC_11	U100-K5	LVDCI25

SRAM3_DATA_LVC_12	U100-M7	LVDCI25
SRAM3_DATA_LVC_13	U100-M9	LVDCI25
SRAM3_DATA_LVC_14	U100-M8	LVDCI25
SRAM3_DATA_LVC_15	U100-L3	LVDCI25
SRAM3_DATA_LVC_16	U100-M2	LVDCI25
SRAM3_DATA_LVC_17	U100-L2	LVDCI25
SRAM3_DATA_LVC_18	U100-K1	LVDCI25
SRAM3_DATA_LVC_19	U100-K2	LVDCI25
SRAM3_DATA_LVC_20	U100-J1	LVDCI25
SRAM3_DATA_LVC_21	U100-J2	LVDCI25
SRAM3_DATA_LVC_22	U100-H1	LVDCI25
SRAM3_DATA_LVC_23	U100-L1	LVDCI25
SRAM3_DATA_LVC_24	U100-H2	LVDCI25
SRAM3_DATA_LVC_25	U100-G1	LVDCI25
SRAM3_DATA_LVC_26	U100-G2	LVDCI25
SRAM3_DATA_LVC_27	U100-F1	LVDCI25
SRAM3_DATA_LVC_28	U100-F2	LVDCI25
SRAM3_DATA_LVC_29	U100-E1	LVDCI25
SRAM3_DATA_LVC_30	U100-E2	LVDCI25
SRAM3_DATA_LVC_31	U100-D1	LVDCI25
SRAM3_BW_LVC_L_0	U100-J6	LVDCI25
SRAM3_BW_LVC_L_1	U100-K3	LVDCI25
SRAM3_BW_LVC_L_2	U100-K4	LVDCI25
SRAM3_BW_LVC_L_3	U100-G5	LVDCI25
SRAM3_CLK_LVC	U100-G3	LVCMOS25

SRAM3_RW_LVC	U100-K8	LVDCI25
SRAM3_CE_LVC_L	U100-L5	LVDCI25
SRAM3_ADV/LD_LVC	U100-N3	LVDCI25

2.9.2 Power Interface

Using the maximum power usage for each voltage it is possible to determine the connector to use between the Battery Board and the digital board. Assuming that each connector pin can carry 3 amps maximum but using a maximum of 1.5A-2A per pin (so the pins will not get hot and there is a safety margin) the following is needed:

Table 63 Required Power Pins

Voltage	Current	Required Number of Pins
12	2.50	2
3.3	2.36	2
2.5	1.03	1
1.5	4.11	3
GND		4
Total		10

The power connector is a dual row Hirose DF11 18 pin right angle connector.

I2C serial communication is added to the power interface so that if a “smart” battery charger with SMBus or I2C interfaces is added to the Battery Board then the Cerfcube can monitor the battery charger. The I2C signals are on one end of the connector separated from the Voltage pins by GND lines. The I2C farthest from the 1.5V lines and closest to the 5V line since crosstalk would have a larger impact on the low voltage lines than the higher voltage lines.

Table 64 Power Connector Pinout

Pin #	Voltage	Voltage	Pin #
1	I2C SDA	I2C SCL	2
3	12	GND	4
5	12	GND	6
7	12	GND	8

9	3.3	GND	10
11	3.3	GND	12
13	3.3	GND	14
15	2.5	GND	16
17	2.5	GND	18
19	1.5	GND	20
21	1.5	GND	22
23	1.5	GND	24

2.9.3 RF 5GHz Board Interface

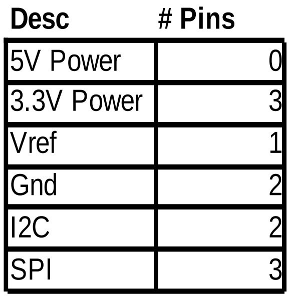
The Interface to the RF board consists of Power, Control, Status and Base-band Analog signals.

Since the RF board is mounted directly to the Digital Board the connectors between the boards are board-to-board.

The RF connectors carrying the base-band analog signals are 50 ohm MCX connectors. There are 4 connectors for the transmitted signal and 4 connectors for the received signal. These connectors determine the spacing between the two boards. Using Johnson Components 50 ohm Straight Jack Receptacle on the Digital Board (part # 133-3701-211) and Johnson Components 50 ohm Straight Plug Receptacle – Low Profile (part # 133-3801-211) the distance between the boards is 7.24mm (0.285 in).

The Digital Power, I2C and SPI signals are on a Hirose FX6 20 pin connector. The height of the connector is 7mm. The connector has 1.7mm long contacts the 7.24 mm board-to-board height is not a problem. The Digital Board should use the FX6-20S-0.8SV2. The RF board should use the FX6-20P-0.8SV.

Table 65 Digital Connector Pin Count



Desc	# Pins
5V Power	0
3.3V Power	3
Vref	1
Gnd	2
I2C	2
SPI	3

Table 66 Digital Connector Pinout

Pin #	Signal Name	Signal Name	Pin #
1	3.3V	3.3V	2
3	Vref	3.3V	4
5	GND	GND	6
7	N.C. (SPIEN1)	N.C. (SPIEN2)	8
9	N.C. (SPIEN3)	N.C. (SPIEN4)	10
11	N.C. (SPIEN5)	N.C. (SPIEN6)	12
13	N.C. (SPIEN7)	N.C. (SPIEN8)	14
15	N.C. (SPIEN9)	N.C. (SPI_MISO)	16
17	N.C. (SPI_MOSI)	N.C. (SPICLK)	18
19	I2C SDA	I2C SCK	20

2.10 Thermal

2.10.1 FPGA

FPGA has maximum power usage of 9 watts (see power section of this document).

The BGA package can dissipate up to 3 watts unaided (with sufficient heat dissipation by the board ground plane).

Try passive heat sink Aavid Thermalloy part number 374324B00035.

2.11 Physcial PC Board

2.11.1 Layers

The Printed Circuit board shall be 6 layers. The total thickness shall not exceed 0.066” (so that it can fit in the slots in the rails of our case).

Cooper layer thicknesses are as follows:

Copper oz per square ft.	**Thinkness in MILs**
½	0.7
1	1.4
2	2.8
3	4.2

Figure 5 Copper layer thickness

To keep costs down the maximum line width possible while routing lines out of the FPGA (between FPGA pads and Via within the boundaries of the FPGA) are used. The FPGA line width is thus 6mil. A 5mil width increases the board cost by 10% (for a 6 layer board). The small 6 mil line with also helps to increase the spacing between adjacent trace (reduce crosstalk) for traces outside the boundary of the FPGA.

The following table was obtained from the Impedance Calculator at http://www.emulab.umr.edu/pcbtlc .

Table 67 Microstrip Impedance (trace width =6mils, trace thickness t=1.4 mils (1 oz.)).

Dielectric Height (mil)	**Zo(ohm), er=4.48, f=33MHz**	**Zo(ohm), er=4.42, f=80MHz**	**Zo(ohm), er=4.27, f=480MHz**	**Zo (ohm), er=4.13, f=2.5Ghz**
5		56.98		
8	73.54	73.54	74.89	75.83
10		81.96		
12		88.53		

Table 68 Microstrip Impedance (Ht=8mil, dielectric=4.42, copper t=1oz).

Trace Width (mil)	**Zo (ohm)**	**Lo (nH/in)**	**Co(pF/in)**	**Td(ns/in)**
5.7	75	10.56	1.877	0.1409
7.372	68	9.571	2.07	0.1409
9.013	62	8.726	2.27	0.1409
13.24	50	7.037	2.815	0.1409

The two middle signal layers do not have a plane between them so the impedance for each signal layer is calculated as an Asymmetric Strip-line ignoring the other signal layer. The "Large Height" is then the middle pre-preg thickness, the thickness of the other signal layer and the pre-preg thickness between the other signal layer and its plane.

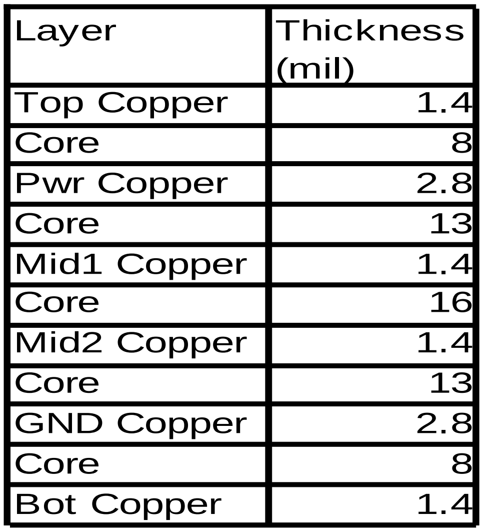
Table 69 Asymactric Stripline Impedance (copper t=1oz, er=4.42, small Ht =13mil, large H1=30.4mil)

Trace Width (mil)	Zo (ohm)	Lo (nH/in)	Co(pF/in)	Td(ns/in)
6	72.53	12.98	2.458	2.136

The layer thicknesses and trace widths are adjusted to attempt to match the impedance of the internal and external layers. The middle prepreg should be as thick as possible to separate the two mid signal layers. Also to reduce crosstalk the core between the mid layers and their plane should be as small as is reasonable.

The PWR layer should be at least 1oz copper to carry the power current. 2oz copper would also be fine (even better). The 4 paths to carry the 1.5V power to the interior of the FPGA carry 4 amps at maximum expected load. That is approximately 1 amp per paths. The shorter paths will carry slightly more current than the long paths but for this design it is assume that they all carry 1A. Each 1.5V path bisects each of the 4 sides of the FPGA at the middle of the side. This helps reduce the number of signals on the Top layer and Mid2 layers that have to cross the plane split between 1.5V and the Vcco of the banks. A signal trace crossing an adjacent plane split causes a characteristic impedance increase at the split thus causing a reflection on the signal. The cross section of each path has approximately 66mil wide copper (where 3 vias across the path reduce the amount of copper). Using the PCB trace width calculator at http://www.geocities.com/CapeCanaveral/Lab/9643/TraceWidth.htm an internal layer with 2oz copper will raise temperature by 2 degrees C. Copper of 1oz weight will increase temperature by 5 degrees C (resistance will be 7m ohm).

The GND layer should be 2oz copper to help transfer heat to the edge of the board but to save cost 1oz copper would work.



Layer	Thickness (mil)
Top Copper	1.4
Core	8
Pwr Copper	2.8
Core	13
Mid1 Copper	1.4
Core	16
Mid2 Copper	1.4
Core	13
GND Copper	2.8
Core	8
Bot Copper	1.4

Figure 6 Printed Circuit Board Stack Thicknesses

2.11.1.1 MicroStrip Trace Widths

Single ended traces on the top and bottom of the board have widths as follows:

Signal Type	Height (mils)	Signal Frequency (MHz)	Dielectric constant	Impedance Z0	Trace Width (mils)
Tx/Rx Analog	8	50MHz	4.45	50	12.8
Dig DAC	8	100MHz	4.41	73	6
Dig ADC	8	100MHz	4.41	50	12.8

Differential traces on top and bottom of the board have the spacing as follows.

Signal Type	Height (mils)	Signal Freq (MHz)	Dielectric constant	Z0	Trace Width (mils)	Zdiff	Trace edge-edge (mils)
Tx/Rx Analog	8	50	4.45	50	12.8	97/99	20/25
Clk DAC	8	100	4.41	73.5	6	143/145	25/30
USB	8	480	4.27	45	15.74	89	20
PCIe	8	2500	4.13	75.8	6	147/149	25/30

2.11.1.2 Impedance Controlled Vias

Controlled impedance vias are situated with a central signal via and 4 equally spaced reference vias. For our 6 layer board two of the vias are connected to the VCC plane and two are connected to the GND plane. Capacitors connected the reference vias to provide a signal return path between the planes.

The impedance of the configuration is determined by [4]:

$Z = \sqrt{(L / (4 * C))}$

$L = \mu/\pi * \mathrm{ACOSH}\ (D / (2 * a))$

$C = \pi * \varepsilon / \mathrm{ACOSH}(D / (2 * a))$

a = via radius

D = signal via center to reference via center distance

General rules:

- Signal via clearance ($D – 2a$)
- Trace width should be nearly same size as signal via diameter.
- Layer height <= distance between signal trace and GND via.

With 50ohm trace (13.2mil wide) the equations become a=6.6mil, D=38mil.

With a 75 ohm trace (5.7mil wide) the equations become a=4mil (smallest fabricated), D=52mil

2.11.2 Layout

This section contains board layout considerations.

The RF connector placement is determined by factors from both Digital and RF boards. The TX connectors have been arbitrarily assigned the left side of the board. They are near the front of the board to accommodate the layout of the RF board (base-band at the front of the board, high frequency RF at the back of the board). Rx connectors are on the right side of the board. One pair of the RX connectors are near the middle of the board to accommodate the placement of the placement of analog base-band pins on the demodulator IC on the RF board.

2.11.2.1 USB Data

There must be 90 ohm impedance between the data differential lines and 30 ohms to ground. The

USB Organization states that with typical FR4 and 4 layers that 12mil trace widths and 33mil between traces is appropriate.

TBS Calculate actual impedances for our board.

2.11.2.2 EZ-USB

The 56 pin QFN package must have a heat sync pad under the device. The recommended via array is 5x5 with finished hole size of 13 mils.

2.11.2.3 FPGA

Signal layer trace assignments are largely determined by the configuration of the pins on a bank. Bottom layer pins are near the outside edge of a bank. Top layer pins are near the inside edge of the bank. Mid1 layer pins are next to the top layer pins and Mid2 layer pins are between the bottom layer and Mid1 layer pins.

Blind vias are required for nearly all pad to layer transitions within the boundaries of the FPGA. Since through vias are cheaper they should be used where possible.

Each Bank has its own split power plane. Power for Vccint is run between banks on each side of FPGA. This gives Vccint 4 paths into the FPGA (see the Stack Layer section for more information on split plane placement and thickness.

2.11.2.3.1 Bank 0

Bank0 traces are routed such that all bottom layer traces are grouped together at the DAC. All top layer trace are grouped together at the DAC. Mid1 layer and Mid2 layer traces alternate where possible so that Mid1 and Mid2 layer traces to not cross except possibly within the boundry of the FPGA.

With grouped traces for the top and bottom layers it is more likely that other traces (example: SPI) can be routed between the DAC and FPGA by alternating between the top and bottom layers near the DAC.

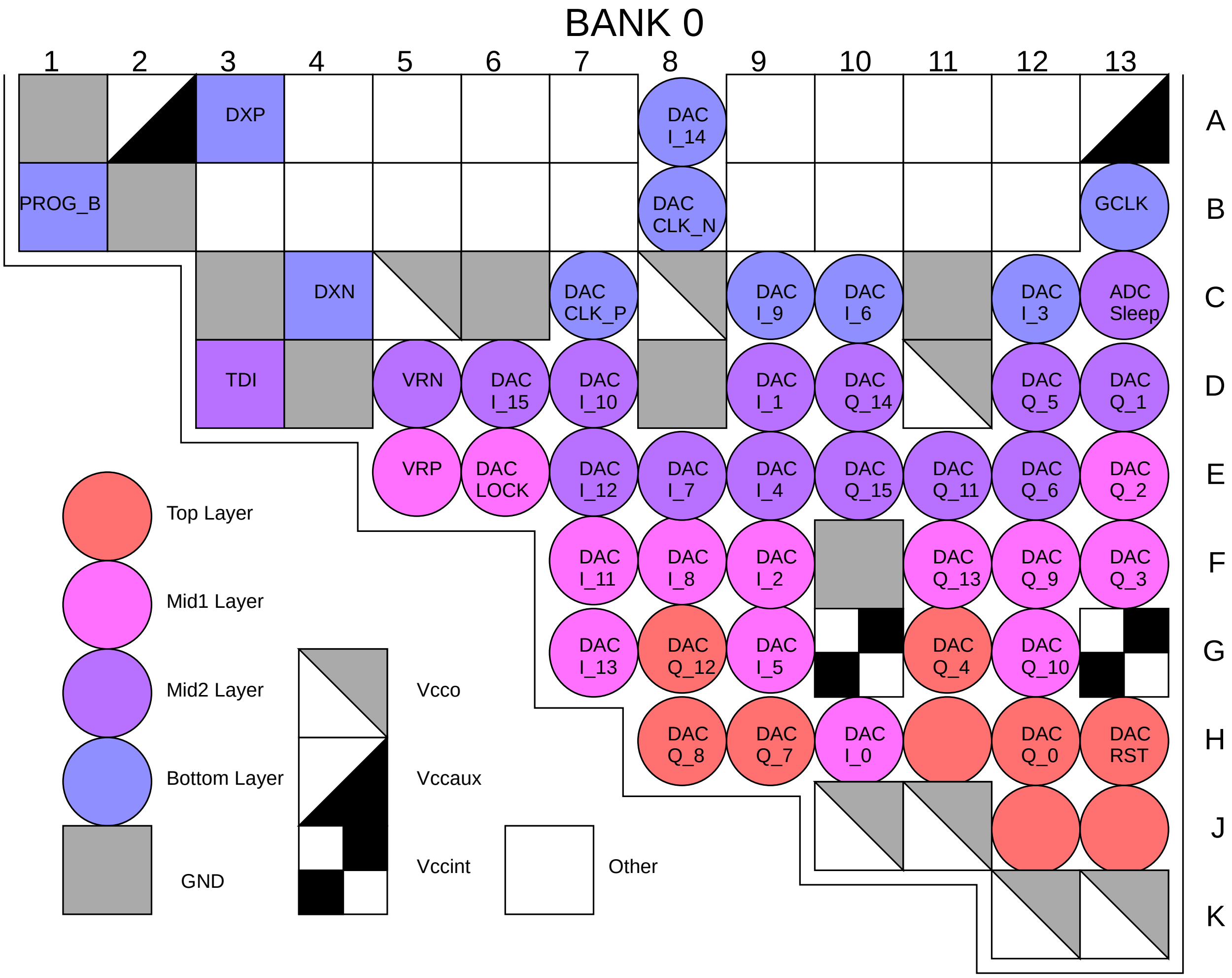


Figure 7 Bank0 Pin and Layer Assignment

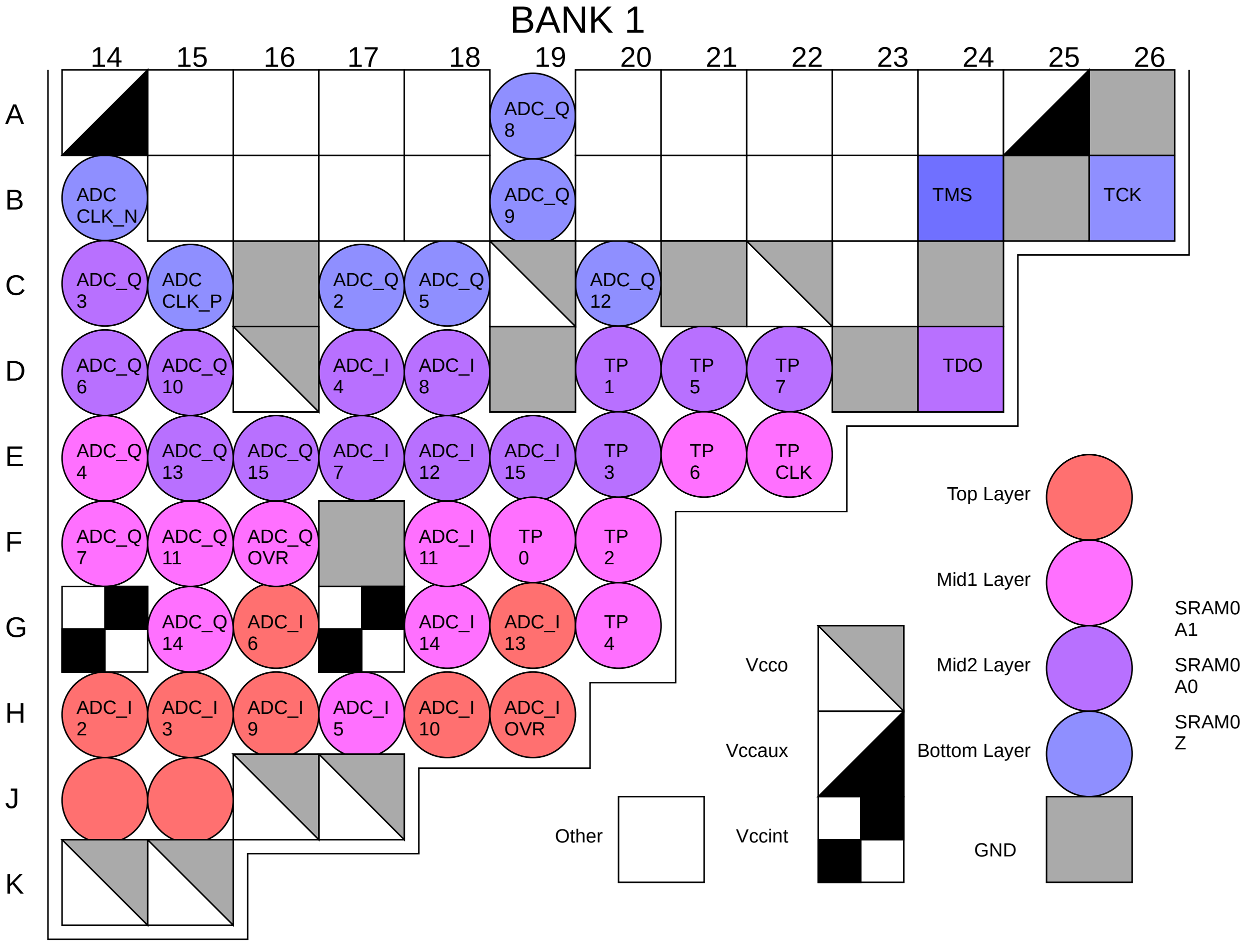
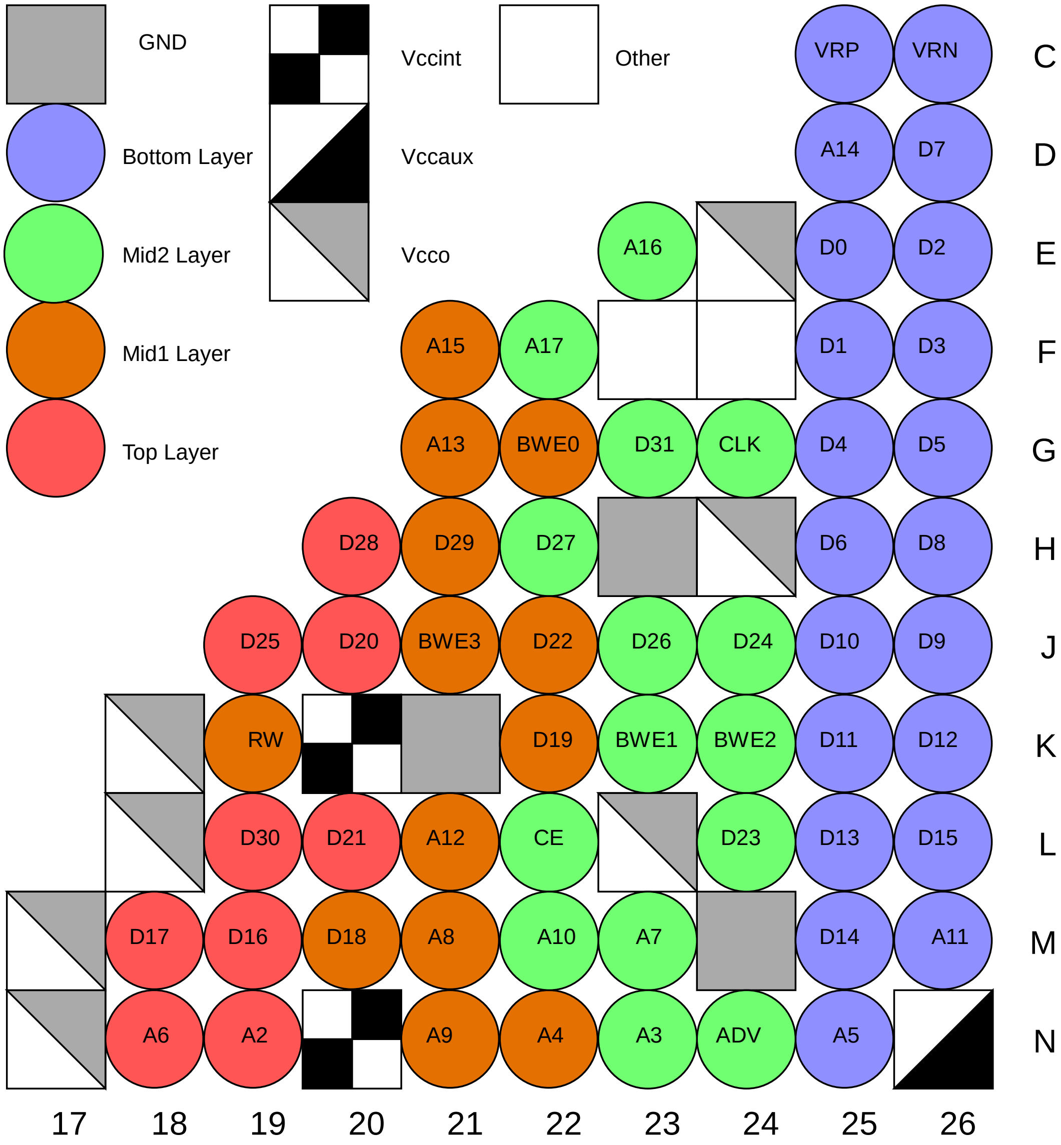


Figure 8 Bank1 Pin and Layer Assignments

BANK 2



▨ GND	▚ Vccint	□ Other
🔵 Bottom Layer	◪ Vccaux	
🟢 Mid2 Layer	◹ Vcco	
🟠 Mid1 Layer		
🔴 Top Layer		

17	18	19	20	21	22	23	24	25	26	
								🔵 VRP	🔵 VRN	C
								🔵 A14	🔵 D7	D
						🟢 A16	◹	🔵 D0	🔵 D2	E
				🟠 A15	🟢 A17	□	□	🔵 D1	🔵 D3	F
				🟠 A13	🟠 BWE0	🟢 D31	🟢 CLK	🔵 D4	🔵 D5	G
			🔴 D28	🟠 D29	🟢 D27	▨	◹	🔵 D6	🔵 D8	H
		🔴 D25	🔴 D20	🟠 BWE3	🟠 D22	🟢 D26	🟢 D24	🔵 D10	🔵 D9	J
	◹	🟠 RW	▚	▨	🟠 D19	🟢 BWE1	🟢 BWE2	🔵 D11	🔵 D12	K
	◹	🔴 D30	🔴 D21	🟠 A12	🟢 CE	◹	🟢 D23	🔵 D13	🔵 D15	L
◹	🔴 D17	🔴 D16	🟠 D18	🟠 A8	🟢 A10	🟢 A7	▨	🔵 D14	🔵 A11	M
◹	🔴 A6	🔴 A2	▚	🟠 A9	🟠 A4	🟢 A3	🟢 ADV	🔵 A5	◪	N

Figure 9 FPGA Bank2 Pin and Layer Assignments

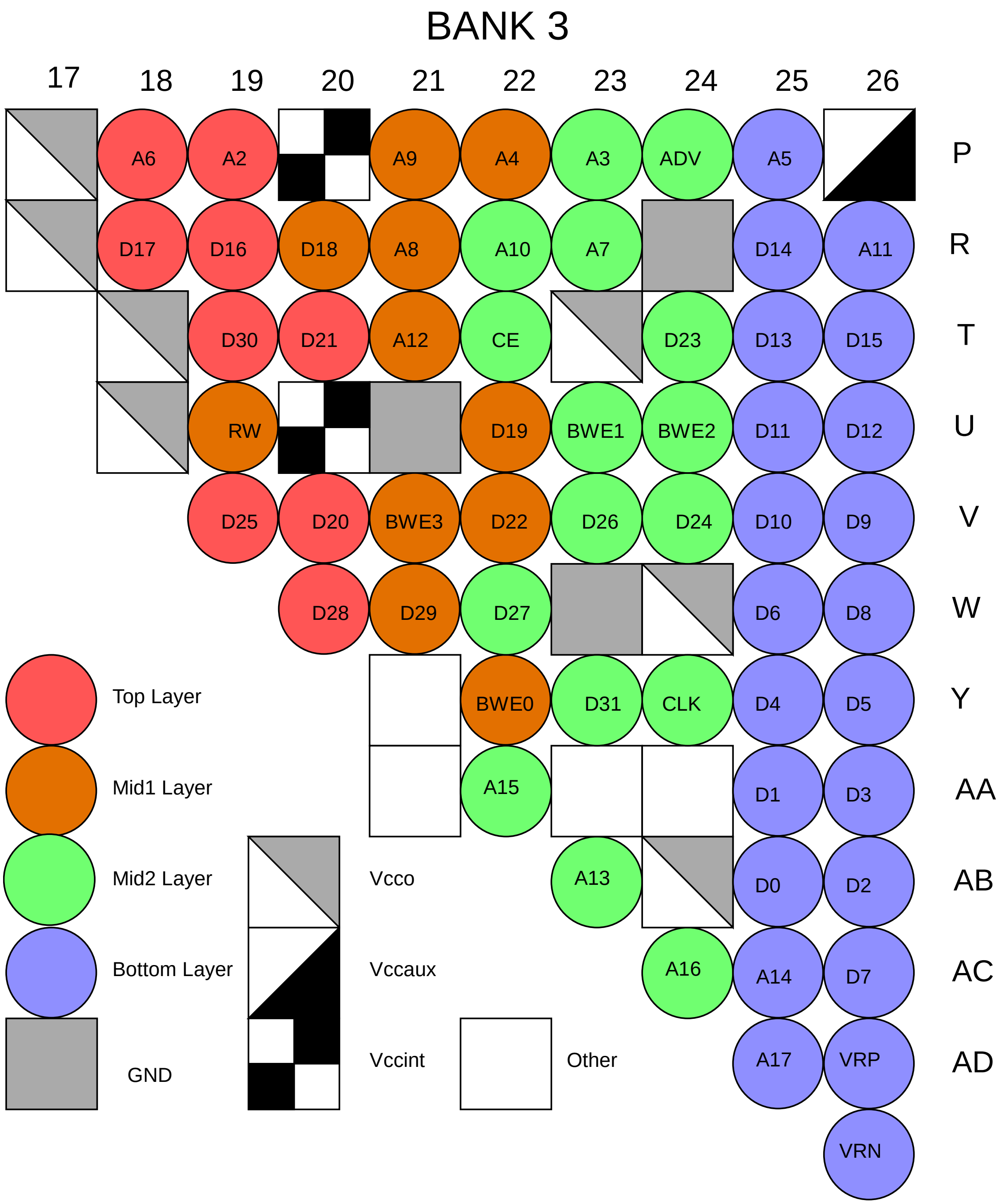


Figure 10 FPGA Bank3 Pin and Layer Assignments

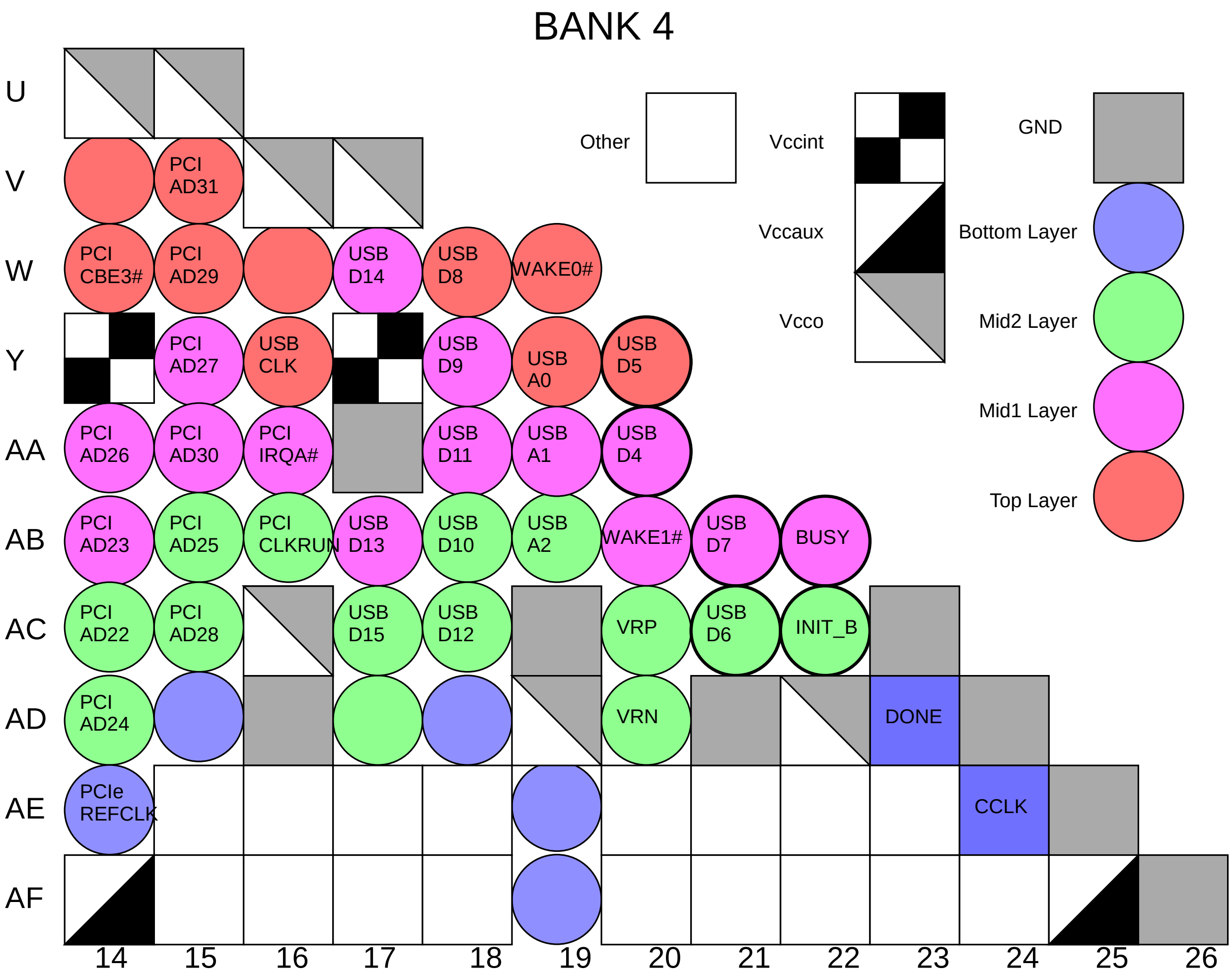
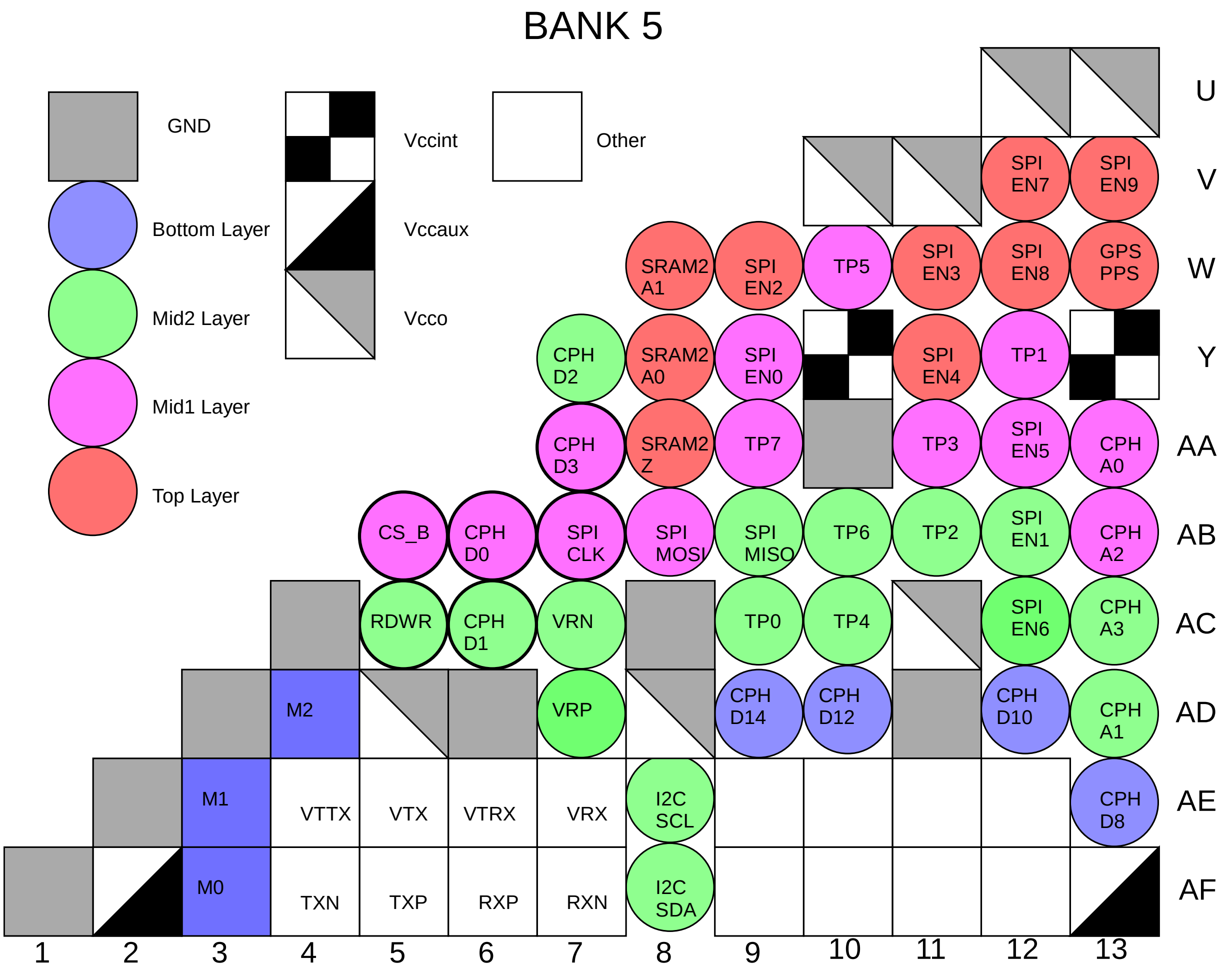
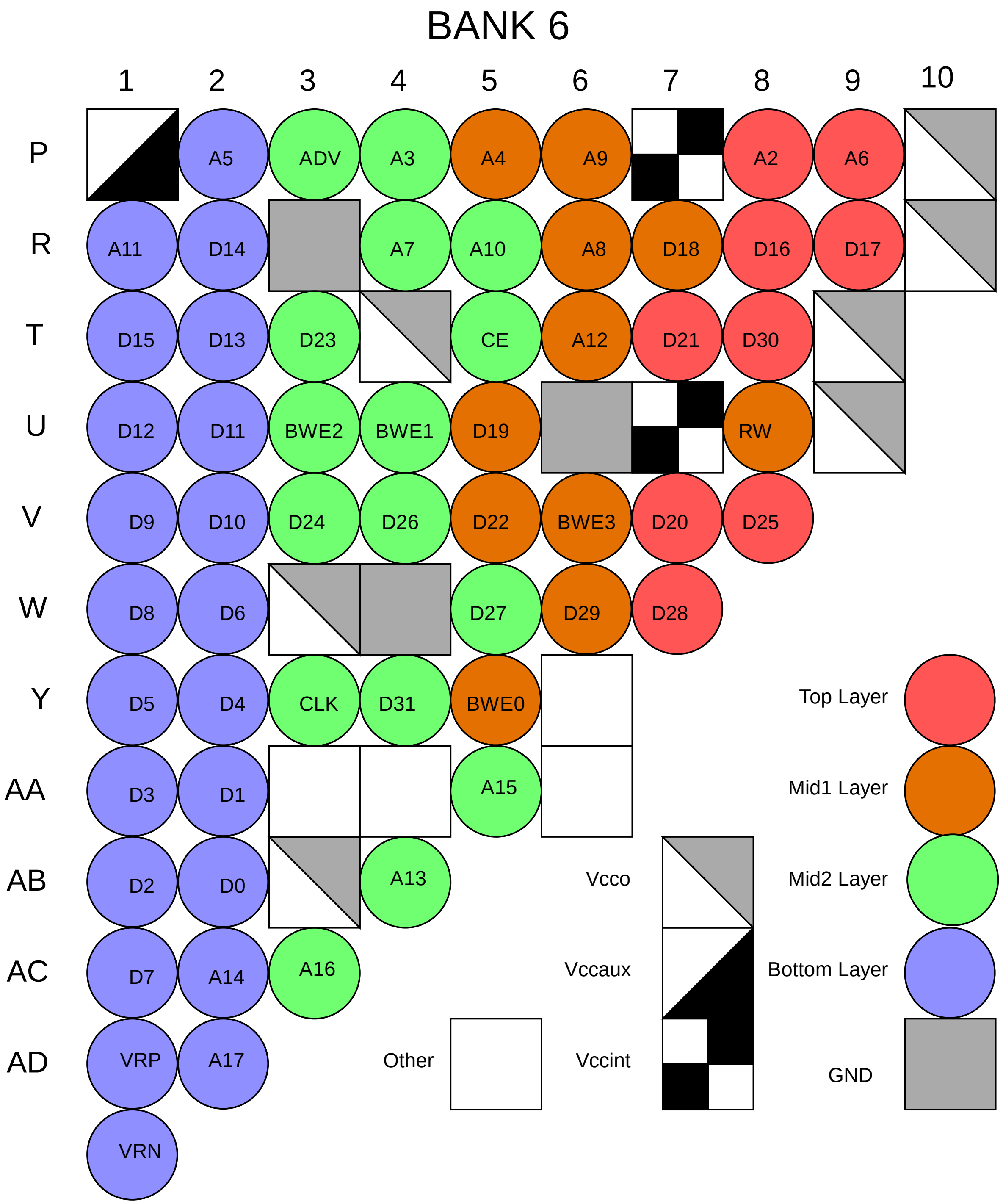


Figure 11 Bank4 Pin and Layer Assignments



	1	2	3	4	5	6	7	8	9	10	11	12	13
U													
V												SPI EN7	SPI EN9
W								SRAM2 A1	SPI EN2	TP5	SPI EN3	SPI EN8	GPS PPS
Y							CPH D2	SRAM2 A0	SPI EN0		SPI EN4	TP1	
AA							CPH D3	SRAM2 Z	TP7		TP3	SPI EN5	CPH A0
AB					CS_B	CPH D0	SPI CLK	SPI MOSI	SPI MISO	TP6	TP2	SPI EN1	CPH A2
AC					RDWR	CPH D1	VRN		TP0	TP4		SPI EN6	CPH A3
AD				M2			VRP		CPH D14	CPH D12		CPH D10	CPH A1
AE			M1	VTTX	VTX	VTRX	VRX	I2C SCL					CPH D8
AF			M0	TXN	TXP	RXP	RXN	I2C SDA					

Figure 12 Bank5 Pin and Layer Assignments

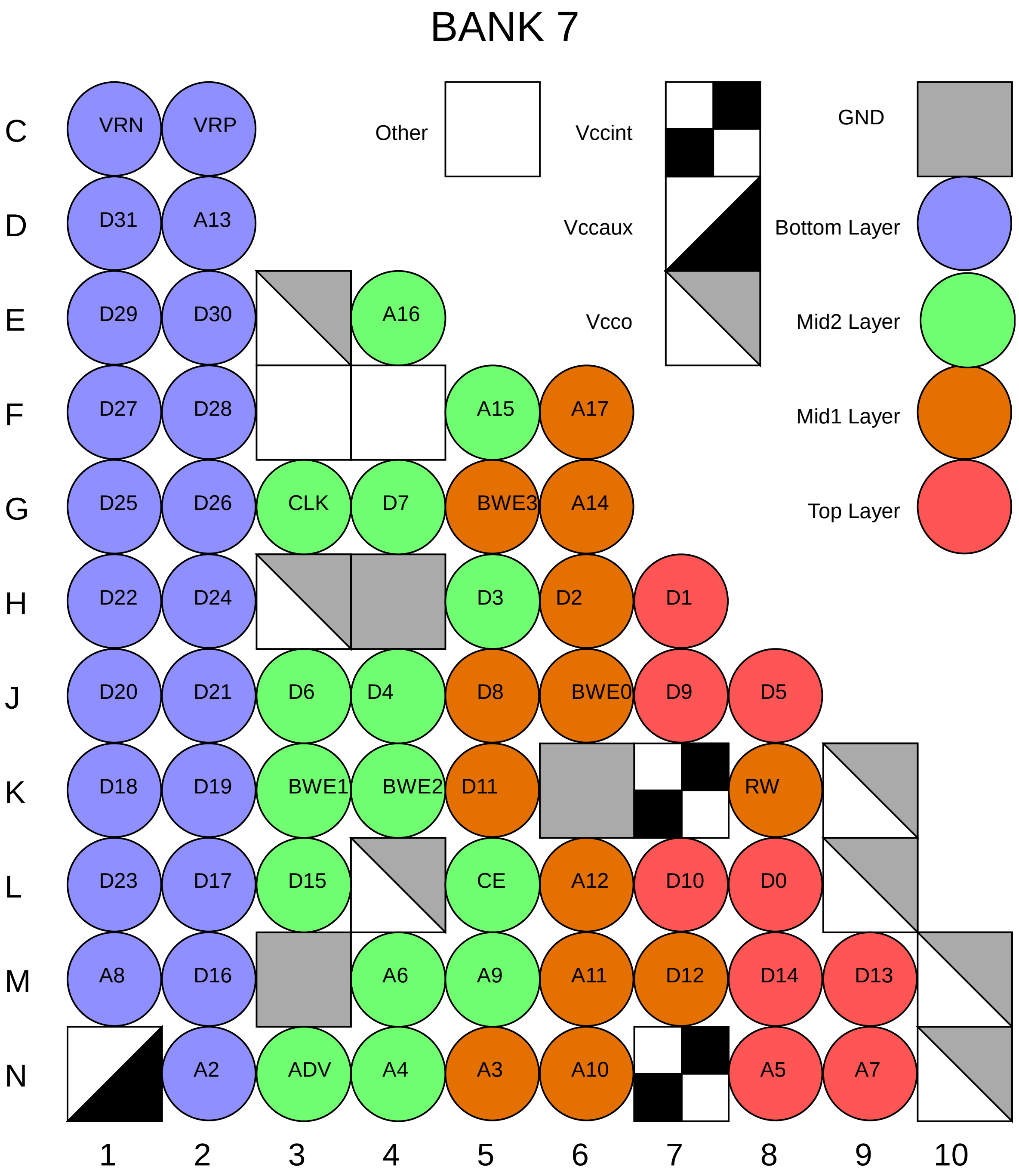


BANK 6

	1	2	3	4	5	6	7	8	9	10
P	◢	🟦 A5	🟩 ADV	🟩 A3	🟧 A4	🟧 A9	▚	🟥 A2	🟥 A6	◹
R	🟦 A11	🟦 D14	■	🟩 A7	🟩 A10	🟧 A8	🟧 D18	🟥 D16	🟥 D17	◹
T	🟦 D15	🟦 D13	🟩 D23	◹	🟩 CE	🟧 A12	🟥 D21	🟥 D30	◹	
U	🟦 D12	🟦 D11	🟩 BWE2	🟩 BWE1	🟧 D19	■	▚	🟧 RW	◹	
V	🟦 D9	🟦 D10	🟩 D24	🟩 D26	🟧 D22	🟧 BWE3	🟥 D20	🟥 D25		
W	🟦 D8	🟦 D6	◹	■	🟩 D27	🟧 D29	🟥 D28			
Y	🟦 D5	🟦 D4	🟩 CLK	🟩 D31	🟧 BWE0	□				
AA	🟦 D3	🟦 D1	□	□	🟩 A15	□				
AB	🟦 D2	🟦 D0	◹	🟩 A13						
AC	🟦 D7	🟦 A14	🟩 A16							
AD	🟦 VRP	🟦 A17								
	🟦 VRN									

Top Layer	🟥
Mid1 Layer	🟧
Mid2 Layer	🟩
Bottom Layer	🟦
GND	■
Vcco	◹
Vccaux	◢
Vccint	▚
Other	□

Figure 13 FPGA Bank6 Pin and Layer Assignments



BANK 7

	1	2	3	4	5	6	7	8	9	10
C	🟦 VRN	🟦 VRP								
D	🟦 D31	🟦 A13								
E	🟦 D29	🟦 D30	◥	🟩 A16						
F	🟦 D27	🟦 D28	□	□	🟩 A15	🟧 A17				
G	🟦 D25	🟦 D26	🟩 CLK	🟩 D7	🟧 BWE3	🟧 A14				
H	🟦 D22	🟦 D24	◥	▨	🟩 D3	🟧 D2	🟥 D1			
J	🟦 D20	🟦 D21	🟩 D6	🟩 D4	🟧 D8	🟧 BWE0	🟥 D9	🟥 D5		
K	🟦 D18	🟦 D19	🟩 BWE1	🟩 BWE2	🟧 D11	▨	▚	🟧 RW	◥	
L	🟦 D23	🟦 D17	🟩 D15	◥	🟩 CE	🟧 A12	🟥 D10	🟥 D0	◥	
M	🟦 A8	🟦 D16	▨	🟩 A6	🟩 A9	🟧 A11	🟧 D12	🟥 D14	🟥 D13	◥
N	◢	🟦 A2	🟩 ADV	🟩 A4	🟧 A3	🟧 A10	▚	🟥 A5	🟥 A7	◥

Other	□
Vccint	▚
Vccaux	◢
Vcco	◥
GND	▨
Bottom Layer	🟦
Mid2 Layer	🟩
Mid1 Layer	🟧
Top Layer	🟥

Figure 14 FPGA Bank7 Pin and Layer Assignments

2.11.2.4 Memory

The CLK signal trace must be isolated from the other memory signals to prevent crosstalk. The VRP and VRN shall be used to set the bank DCI impedances.

Since the clock signal terminates in the middle row of balls on the memory IC the clock signal should be on layer Mid2 close to the edge of the FPGA. As soon a practical adjacent signals on Mid2 and Mid1 layers should be moved as far away from the CLK signal as possible to reduce crosstalk. Use a 50 ohm trace characteristic impedance and destination parallel termination on the clock to reduce cross talk.

To prevent signal ringing the FPGA's memory output ports should have their DCI impedance set close to the trace characteristic impedance of 62 ohm. The only resistor values in 402x2 packages close to this value are either 56 ohm or 68 ohm. Choose the resistor values that work the best for the board in testing.

2.12 Solder Paste Mask Apertures

On a IC package with small pitch pads the solder paste mask has to be smaller than the pad to prevent bridging between the pads. The following table from http://www.tkb-4u.com/articles/printing/stencildesignguide/stencildesignguide.php gives recommended aperture sizes.

Component Pitch	Industry Standard Pad Width	Industry Standard Aperture Width
50 mil	25 mil	25 mil
40 mil	20 mil	20 mil
31 mil	17 mil	16 mil
25 mil	15 mil	12 mil
20 mil	12 mil	10 mil
16 mil	10 mil	8 mil
12 mil	8 mil	6 mil

Table 70 Recommended Pad Aperture Sizes

3 Implementation Restrictions

The board dimensions are restricted to those dimensions required to fit within the radio enclosure. Board dimensions are 7.3" x 6.0".

4 Glossary

<Refer to a project glossary for terms used throughout the project>

(TBS)

5 Change Log

Version	Date	By	Changes
0.1	<date>	<Name>	Initial Working Version (J. Guffy)
1.0	<date>	<Name>	Initial Released Version (J. Guffy)
2.0	<date>	Leon S. Searl	Revised for board with Tx and Rx. (L. Searl)

6 Notes

7 References

[1] Integrated Circuit Systems, Inc., “HiPerClockS Application Note, High Speed LVCMOS Driver Termination Design Guide”. PDF FileName=”lvcmos_termination.pdf”.

[2] Integrated Circuit Systems, Inc., “HiPerClockS Application Note, Power Dissipation for High Speed LVCMOS Buffer”. PDF Filename=”lvcmos_power_dissipation.pdf”

[1] COMexpress Module Base Specification Revision 1.0, PICMG, July 10, 2005

[2] HFAN-01.1: Choosing AC-Coupling Capacitors, http://www.maxim-ic.com/appnotes.cfm/appnote_number/292

[3] RocketIO Transciever User Guide, Version 2.5, Dec 9, 2004, Xilinx Inc., http://direct.xilinx.com/bvdocs/userguides/ug024.pdf

[4] Designing Controlled Impedance Vias, Thomas Neu, www.eda.com, October 2, 2003, p. 67.