Technical Report

KU Agile Radio 5 GHz 3.0 RF Module Description

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KU Agile Radio 5 GHz 3.0 RF Module Description

1. Overview

The KU Agile Radio (KUAR) is a modular design, consisting of separate power supply, digital processing, and radio frequency (RF) sections. The KUAR system has been specifically designed to address the particular needs of wireless networking and radio frequency research efforts, and offers the capability to conduct tests in a variety of frequency bands through the use of a range of RF module sections.

The RF module designs have been tailored for experimental use. KUAR features include the ability to set independent transmit and receive frequencies, as well as digital control of the transmit power output and receive gain levels. The RF modules incorporate standard SMA-style RF input and output connectors to allow the use of a variety of antenna types and configurations.

Digital control of transmitter output power, receiver front end attenuation, and IF amplifier gain should prove to be useful for fading channel experiments, and also allows researchers to configure the system to accommodate a variety of experiments and test environments.

The RF modules currently in use offer a frequency range of 5.25-5.85 GHz, and are designed for operation in the 5 GHz Unlicensed National Information Infrastructure (UNII) and Industrial, Scientific and Medical (ISM) bands. A 2.05-2.70 GHz design is in process.

It is assumed that researchers operating KUAR transceivers have a through understanding of pertinent rules and regulations. It is important to note that the KUAR 5 GHz RF module is capable of operation outside the boundaries of 5 GHz UNII / ISM band frequency allocations (UNII 1: 5.25-5.35 GHz, UNII 2: 5.47-5.725 GHz, UNII 3: 5.725-5.825 GHz, 5.8 GHz ISM Band: 5.725-5.875 GHz) mandated by the Federal Communications Commission (FCC).

The 5 GHz RF module is a hybrid direct conversion design that makes use of a traditional superheterodyne frequency conversion to and from an intermediate frequency (IF) range of 1.85-2.45 GHz, which is directly converted to baseband using a quadrature demodulator, and from baseband using a direct conversion quadrature modulator. The RF modules are currently configured to select 30 MHz sections of the frequency band, in 4 MHz tuning steps.

2. Local Oscillators

The design incorporates three local oscillator (LO) sections; an IF receive (RX) LO (RX LO1), an IF transmit (TX) LO (TX LO2) and a common 3.4 GHZ fixed frequency LO (RX+TX LO3) which is supplied to separate receive and transmit front-end mixers. All three LOs share a buffered 16MHz reference frequency generated by a Fox 801BE-160 temperature compensated crystal oscillator (TCXO), and distributed using a Pericom PI49FCT805ATS dual 1:5 CMOS clock fanout buffer. The 16 MHz reference frequency is also provided to the digital processing section of the transceiver.

RX LO1 and TX LO2 are two-stage differential output designs, with each LO comprised of a pair of integrated synthesizer / voltage controlled oscillator (VCO) devices; an Analog Devices 1.85-2.15 GHz ADF4360-2 is coupled with an Analog Devices 2.05-2.45 GHz ADF4360-1 to provide an effective tuning range of 600 MHz.

RX+TX LO3 components consist of an Analog Devices ADF4113 PLL synthesizer device controlling the tuning port of a Z-Comm SMV3300A VCO. The SMV3300A RF output is passed through a 5th order Chebychev interdigital band-pass filter (BPF), centered at 3.4 GHz with a -3dB bandwidth (BW) of 200 MHz, to the input of an Agilent MGA-82563 (+10dB Gain, +17dBm P1dB, 2.4dB NF @ 4.0 GHz) amplifier, which feeds into a Wilkinson 3dB splitter, providing a 3.4 GHz LO to the RX and TX chain frequency mixers.

3. Programming

A Freescale MC68HC08 8-bit microcontroller unit (MCU) is used to interface the digital processing section to the programmable components of the 5 GHz RF module. All frequency settings and amplifier gain controls are programmed using a Serial Peripheral Interface (SPI) bus, while the RX chain variable attenuator is controlled with 3V logic levels. The MCU is used to pass control register data and collect device status information, and is connected to the digital processing section using an inter-integrated circuit (I2C) bus. Refer to the KU Agile Radio 5 GHz 3.0 Digital Interface section of this document for detailed programming information.

4. Receiver

Starting at the input SMA RF connector, the RX chain consists of a 5th order Chebychev interdigital BPF, centered at 5.5 GHz with a -3dB BW of 600 MHz, followed by a 6-bit programmable GaAs 0-31.5dB Hittite HMC425LP3 variable attenuator, and an Agilent MGA-85676 (+19dB Gain, +4.3dBm $_{P1dB}$, 1.8dB NF @ 6.0 GHz) Low Noise Amplifier (LNA). The output of the LNA feeds the RF input of a Hittite HMC488MS8G GaAs double balanced mixer, which features an integrated LO amplifier, and mixes the fixed frequency 3.4 GHz input from RX+TX LO3, down-converting frequencies from the 5.250-5.850 GHz range to the 1.850-2.450 GHz intermediate frequency (IF) range of the receive section.

Down-converted IF frequencies are passed through a 5th order Chebychev interdigital BPF centered at 2.15 GHz with a -3dB BW of 600 MHz, and are then fed into an Analog Devices AD8347 direct conversion quadrature demodulator. The AD8347 amplifies the IF signal with two stages of variable gain amplification before frequency conversion via two Gilbert-cell mixers, which perform a direct conversion to baseband using the differential 1.850-2.450 GHz output from RX LO1.

The RX LO1 inputs to the AD8347 are internally conditioned using a poly-phase filtered phase splitter, and then connect to the Gilbert-cell mixer inputs. The baseband outputs of the mixers are followed by separate in-phase (I) and quadrature-phase (Q) channel variable gain amplifiers (VGA). A user may select either automatic gain control (AGC), which employs baseband level detectors integral to the AD8347, or manually control the RX IF VGA gain levels with the output from an Analog Devices 6-bit AD5601 RX Digital-to-Analog converter (DAC).

The AD8347 internal IF and baseband VGAs provide a cumulative 69.5 dB of gain control. The baseband VGA outputs are brought out of the device to allow filtering before final amplification. Baseband I and Q signals are passed through a pair of 30 MHz -3dB BW low-pass filters (LPF), before being amplified and output as differential I and Q signals to a pair of Analog Devices AD6645 12-bit 80MSPS Analog-to-Digital converters (ADC) in the digital processing section.

5. Transmitter

The 5 GHz module TX chain begins with differential I and Q inputs from an Analog Devices AD9777 16-bit 160 MSPS dual DAC located in the digital processing section, which are low-

pass filtered with a pair of 30 MHz -3dB BW differential LPFs, then passed to I and Q inputs of an Analog Devices AD8349 direct conversion quadrature modulator.

The modulator uses the differential 1.850-2.450 GHz output of TX LO2 to up-convert baseband I and Q signals. The differential TX LO2 input signal is buffered, and then split into I and Q signals using a poly-phase phase splitter. These two LO signals are amplified, then mixed with the corresponding I channel and Q channel baseband input signals in two Gilbert cell mixers. The mixer outputs are then summed together in the AD8349 output amplifier.

The 1.85-2.45 GHz output of the AD8349 is passed through the TX IF BPF; a 5th order Chebychev interdigital design centered at 2.15 GHz with a -3dB BW of 600 MHz. The TX IF BPF output is then amplified by the programmable TX IF VGA. The TX IF VGA consists of a Phillips BGA2031/1 VGA (+23dB Gain, +11dBm P1dB @ 1.9 GHz) combined with an Analog Devices AD5601 6-bit DAC; the DAC output voltage sets the gain level of the BGA2031/1, which has a gain control range of 56dB.

The output of the TX IF VGA is connected to the IF port of the TX mixer (Hittite HMC488MS8G), which uses the 3.4 GHz input from RX+TX LO3 to up-convert TX IF frequencies to the 5.25-5.850 GHz range. The RF output of the TX mixer is amplified by a Mini-Circuits ERA-1SM (+6dB Gain, +12dBm P1dB, 4.3dB NF @ 6.0 GHz) RF amp, then passed through a 5th order Chebychev interdigital BPF, centered at 5.5 GHz with a -3dB BW of 600 MHz. The band-pass filtered signal is fed into the input of an Agilent MGA-83563 (+17dB G, +15dBm P1dB, +18dBm PSAT@6.0 GHz) amplifier, with the amplifier output connected to the TX output SMA connector, providing an output of up to 15 dBm (32mW) of RF signal power in the 5.25-5.85 GHz frequency range.

6. Antennas

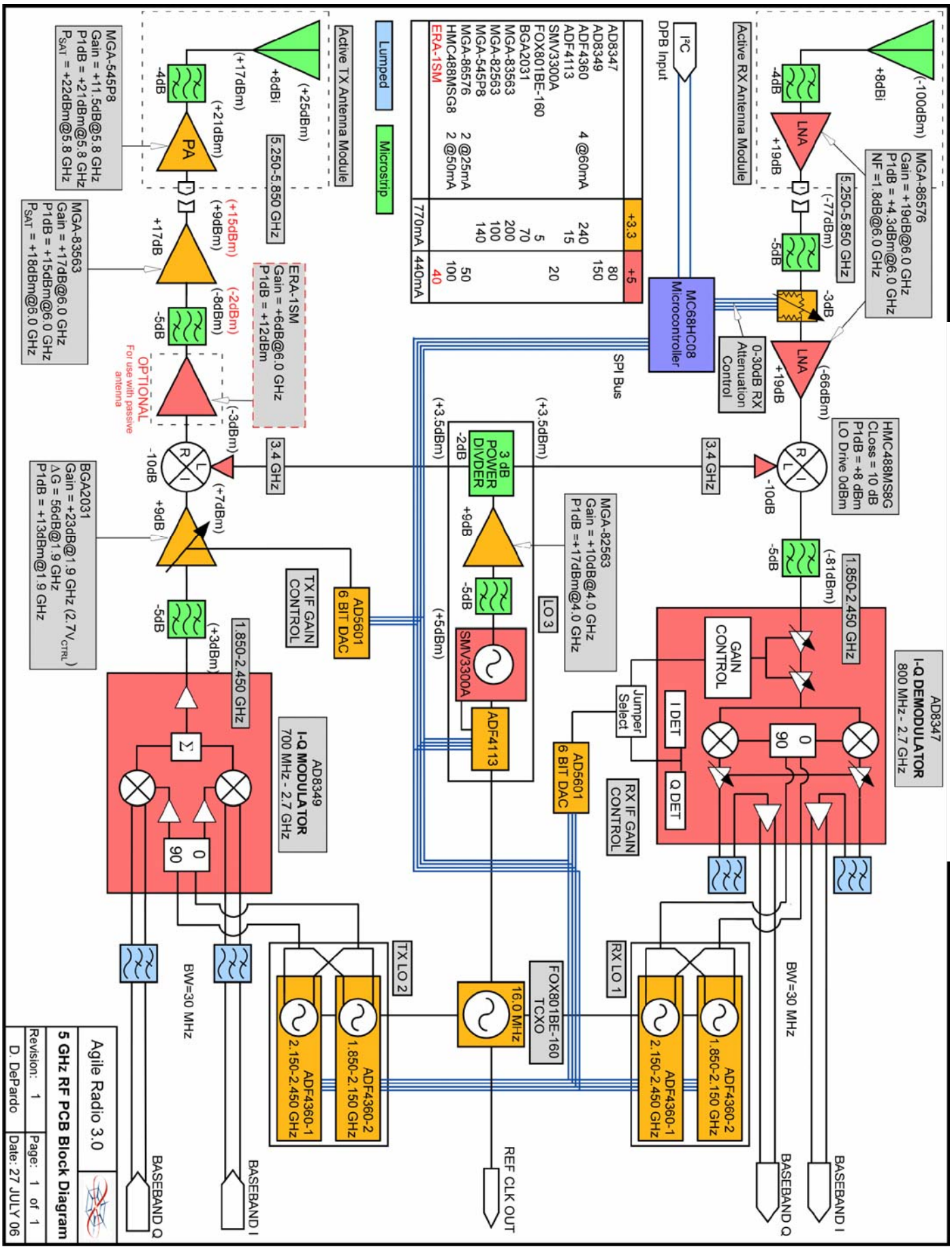
Three basic configurations of Broadband 5 GHz directional planar antennas have been designed and constructed to complement the KUAR system; basic passive, active RX, and active TX. The passive antennas are intended for use in indoor or short range outdoor test environments, while the active versions utilize integrated RF amplification and filtering to provide longer range outdoor test performance.

The active and passive antennas share the same basic planar element design, consisting of an air dielectric patch element and feed structure that exhibits a 1.5:1 VSWR BW of 1.5 GHz, centered at 5.5 GHz. The element design provides 8.5dB of directive gain, with respective E and H plane -3dB beam-widths of 80° and 70°. The passive antenna element feed structure is directly connected to an SMA-style RF connector, and is suitable for use on either the KUAR RX or TX port, or both, depending upon testing needs.

In the case of the active RX antenna, the feed structure connects to a 5.5 GHz 3rd order Chebychev interdigital BPF with a -3dB BW of 600 MHz. The filtered signal is then passed through an Agilent MGA-86576 LNA to the antenna SMA-style RF output connector.

The active TX antenna design uses an SMA-style RF connector as an RF input. The input signal is fed into an Agilent MGA-545P8 (+11.5 dB Gain, +21dBm $_{P1dB}$, +22dBm P_{SAT}) RF power amp, then passed through a 3rd order Chebychev interdigital BPF centered at 5.5 GHz, with a -3dB BW of 600 MHz. The output of the BPF is connected to the antenna element feed.

A KUAR 5 GHz transceiver, equipped with the previously described active RX and TX antennas, is capable of recovering signal levels as low as -100dBm, and can transmit an Effective Isotropic Radiated Power (EIRP) level of up to +25dBm (354mW) .


Active RX Antenna Module
(-100dBm)
+8dBi
MGA-86576
Gain = +19dB@6.0 GHz
P1dB = +4.3dBm@6.0 GHz
NF =1.8dB@6.0 GHz
-4dB
LNA
+19dB
5.250-5.850 GHz
(-77dBm)
-5dB
-3dB
LNA
+19dB
(-66dBm)
I²C
DPB Input
MC68HC08
Microcontroller
SPI Bus
0-30dB RX
Attenuation
Control
AD8347
I-Q DEMODULATOR
800 MHz - 2.7 GHz
HMC488MS8G
CLoss = 10 dB
P1dB = +8 dBm
LO Drive 0dBm
3.4 GHz
-10dB
-5dB
(-81dBm)
1.850-2.450 GHz
GAIN
CONTROL
I DET
Q DET
0
90
Jumper
Select
AD5601
6 BIT DAC
RX IF GAIN
CONTROL
BASEBAND I
BASEBAND Q
BW=30 MHz
AD8347
I-Q DEMODULATOR
800 MHz - 2.7 GHz
+3.3
+5
770mA
440mA
80
150
240
15
20
5
70
200
100
140
50
100
40
4 @60mA
2 @25mA
2 @50mA
Lumped
Microstrip
Active TX Antenna Module
(+25dBm)
+8dBi
5.250-5.850 GHz
-4dB
(+17dBm)
PA
(+21dBm)
MGA-545P8
Gain = +11.5dB@5.8 GHz
P1dB = +21dBm@5.8 GHz
PSAT = +22dBm@5.8 GHz
(+15dBm)
(+9dBm)
+17dB
-5dB
(-2dBm)
(-8dBm)
OPTIONAL
For use with passive
antenna
(-3dBm)
ERA-1SM
Gain = +6dB@6.0 GHz
P1dB = +12dBm
MGA-83563
Gain = +17dB@6.0 GHz
P1dB = +15dBm@6.0 GHz
PSAT = +18dBm@6.0 GHz
3.4 GHz
-10dB
(+7dBm)
+9dB
BGA2031
Gain = +23dB@1.9 GHz (2.7VCTRL)
ΔG = 56dB@1.9 GHz
P1dB = +13dBm@1.9 GHz
TX IF GAIN
CONTROL
AD5601
6 BIT DAC
(+3.5dBm)
3 dB
POWER
DIVDER
-2dB
+9dB
-5dB
(+5dBm)
MGA-82563
Gain = +10dB@4.0 GHz
P1dB =+17dBm@4.0 GHz
LO 3
SMV3300A
ADF4113
AD8349
I-Q MODULATOR
700 MHz - 2.7 GHz
1.850-2.450 GHz
(+3dBm)
Σ
0
90
TX LO 2
RX LO 1
FOX801BE-160
TCXO
16.0 MHz
ADF4360-2
1.850-2.150 GHz
ADF4360-1
2.150-2.450 GHz
REF CLK OUT
BASEBAND I
BASEBAND Q
BW=30 MHz
Agile Radio 3.0
5 GHz RF PCB Block Diagram
Revision: 1
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D. DePardo
Date: 27 JULY 06

7. Digital Interface and Programming

The KU Agile Radio Digital Processing Board (DPB) sends control signals to a microcontroller on the KU Agile Radio RF Board (RF-5GHz) using an interface based on the Inter-IC bus, commonly known as the I²C bus (http://www.semiconductors.philips.com/markets/mms/protocols/i2c/) interface. The DPB also provides the RF-5GHz section with +3.3V digital supply voltages and an ADC reference level as an optional input to the AD8347 Demodulator baseband output amplifiers via the S900-H900 connector.

Table 1 - Interface between the DPB and RF-5GHz. (S900-H900)

Signal	Pin	Description
+3.3 V (Digital)	1	+3.3 Volt power for digital components
+3.3 V (Digital)	2	+3.3 Volt power for digital components
ADC_VREF	3	Reference voltage for AD8347 Demodulator
+3.3 V (Digital)	4	3.3 Volt power for digital components
Ground	5,6	Digital ground
I2C_SDA_LVC	19	I²C Serial Data I/O
I2C_SCL_LVC	20	I²C Serial Clock I/O

The Freescale MC68HC908AP64CFA microcontroller sends enable signals to various devices on the RF-5GHz board via an SPI bus interface. The enable signals and the associated devices are listed in Table 2.

Table 1 - RF-5GHz board SPI Enable Signals

Signal	Device	Section
SPI_EN_SVC_L1	RX Local Oscillator A VCO/Synthesizer ADF4360-2 (U5)	7.3
SPI_EN_SVC_L2	RX Local Oscillator B VCO/Synthesizer ADF4360-1 (U4)	7.3
SPI_EN_SVC_L3	Demodulator Gain Control DAC AD5601 (U2)	7.5
SPI_EN_SVC_L4	TX Local Oscillator B VCO/Synthesizer ADF4360-1 (U6)	7.3
SPI_EN_SVC_L5	TX Local Oscillator A VCO/Synthesizer ADF4360-2 (U7)	7.3
SPI_EN_SVC_L6	RX & TX 3.4 GHz Local Oscillator Synthesizer ADF4113BRU (U11)	7.4
SPI_EN_SVC_L7	TX IF Gain Control DAC AD5601 (U9)	7.5

7.1. RX Step Attenuator

The Freescale MC68HC908AP64CFA microcontroller (U13) provides a set of four (4) signals used to control the Hittite HMC425LP3 RX front end attenuator (U1) on the RF-5GHz board. The control signals are implemented with general purpose I/O ports of the microcontroller. Each signal enables or disables an associated attenuation weight in dB. A low setting on the signal inserts the associated attenuation. The attenuation is the sum of the enabled weights, plus 1.5 dB, which is the through insertion loss of the device.

Table 2 – RX Front End Step Attenuator Enable Control Signals

Signal	MC68HC908 (U13) Pin# + I/O	Attenuation Weight	HMC425LP3 (U1) Pin# + Label
RF_CTRL1	8 PTB4/T1CH0	2 dB	9 (V1)
RF_CTRL2	3 PTB5/T1CH1	4 dB	8 (V2)
RF_CTRL3	1 PTB6/T2CH0	8 dB	7 (V3)
RF_CTRL4	47 PTB7/T2CH1	16 dB	6 (V4)

Table 3 - RX Front End Step Attenuator Default Settings

RF_CTRL1	RF_CTRL2	RF_CTRL3	RF_CTRL4
0	0	0	0

These default settings set the RX attenuation to maximum (30 dB + 1.5 dB IL).

7.2. RF-5GHz Frequency Synthesizer Muxout Lines

Each of the five frequency synthesizers on the RF-5GHz board has a multiplexed monitor output (muxout) line that can be read by the microcontroller. Each muxout line can provide 8 different selectable outputs. The digital lock detect output is the primary muxout signal of interest.

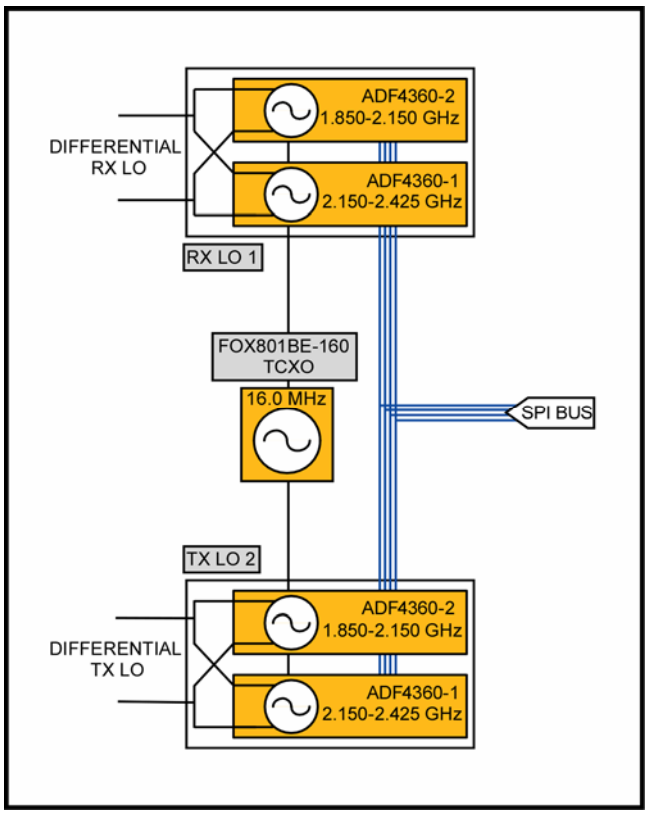
Table 4 – Frequency Synthesizer Monitor Lines

Signal	Device
SPI_MISO_PLL_1	RX LO1 A U5 Pin-20 Low Range (1.850-2.150 GHz)
SPI_MISO_PLL_2	RX LO1 B U4 Pin-20 High Range (2.150-2.425 GHz)
SPI_MISO_PLL_3	TX LO2 A U7 Pin-20 Low Range (1.850-2.150 GHz)
SPI_MISO_PLL_4	TX LO2 B U6 Pin-20 High Range (2.150-2.425 GHz)
SPI_MISO_PLL_5	RX & TX LO3 U11 Pin-14 (3.4 GHz)

7.3. RX LO1 and TX LO2 VCO / Synthesizers

The received (RX) and transmit (TX) frequency bands are determined by separate and independent local oscillators (LOs). The RX and TX LOs are constructed from two Voltage Controlled Oscillator / Frequency Synthesizer (VCO/Synth) circuits. Two VCO/Synth circuits are needed in each LO to cover the desired frequency range. The RX and TX LOs are identical in construction and programming.

Figure 5 – RX LO1 and TX LO2 VCO/Synthesizer Block Diagram



RX LO1 and TX LO2 each use a pair of VCO/Synthesizers to generate the LO frequencies supplied to the KUAR modulator and demodulator circuitry. RX LO1 and TX LO2 are comprised of a 1.850-2.150 GHz Low Range (sometimes called the A component) frequency synthesizer circuit and a 2.150-2.425 GHz High range (sometimes called the B component) frequency synthesizer circuit. RX LO1 and RX LO2 frequency synthesis circuits are independently selected and programmed via the I²C bus and RF-5GHz PCB microcontroller. RX LO1 and TX LO2 share a common 16 MHz TCXO, which is also used by LO3 and the Digital Processing Board.

The core of each of the four RX LO1 and TX LO2 frequency synthesizers is an Analog Devices ADF4360 component. For the Low Range, an ADF4360-2 is used, and for the High Range, an ADF4360-1 is used.

A brief overview of the ADF4360 programming and operation is as follows:

The output frequency of the VCO/Synth is given by:

$$f_{VCO} = [(P \times B) + A \times f_{REF}] / R$$

Where:
f_{VCO} is the VCO output frequency
P is the preset modulus of the prescaler
B is the divide ratio of the 13-bit counter (3 – 8191)
A is the divide ration of the 5-bit “swallow” counter (0 – 31)

f_{REF} is the external reference frequency
R is the reference clock divisor to determine the output frequency spacing

There are a number of constraints on the configuration values.

1. The output frequency can be stepped in units of f_{REF} /R. The RF-5GHz board uses a 16 MHz reference frequency. We will set R to a value of 16 to obtain a frequency spacing of 1 MHz.
2. The output of the prescaler, f_{VCO} /P must be less than 300 MHz. Our maximum f_{VCO} is 2450 MHz so we will set P to a value of 16. The maximum prescaler output is then 153.125 MHz.
3. The minimum N, where N = PB + A, is $N_{min} = P^2-P$. For P = 16, N_{min} = 240. Since A_{max} = 31, PB_{min} = 209. With P = 16, B_{min} = 14.
4. To generate our minimum f_{VCO} = 1.850 GHz, B = 115 and A = 10.
5. To generate our maximum f_{VCO} = 2.450 GHz, B = 153 and A = 2.

The VCO/Synths are controlled with three 24-bit registers called the Control Latch, the N-Counter Latch, and the Reference Counter (R-Counter) Latch. These are loaded via the SPI. The latches must be loaded in the order: R-Counter Latch, Control Latch, and N-Counter Latch. Latch bits are numbered DB00 (LSB) through DB23 (MSB). DB23 (MSB) is loaded first. Data is shifted into an internal holding register on the rising edge of the clock. When the component Load Enable (LE) signal goes from low to high, the held data is loaded into the register specified by DB01…DB00.

Table 6 – Basic RX LO1 and TX LO2 VCO/Synthesizer Control Latch Settings

Latch Bits	Description	Default Value and Setting
DB00 – DB01	Latch select	00 Select Control Latch
DB02 – DB03	Core power setting	11 20 mA (Recommended)
DB04	Counter reset	0 Normal Operation
DB05 – DB07	Multiplexer output select	001 Select Digital Lock Detect
DB08	Phase detector polarity	1 Use on-chip VCO with passive loop filter
DB09	Charge Pump Output	0 (Charge Pump Active)
DB10	Charge Pump Gain	0 (Selects Charge Pump Current Setting 1 or 2)
DB11	Mute Until Lock Detected	1 (Enabled)
DB12 –	Output Power Level	11 (-3 dBm)

DB13		
DB14 – DB16	Charge Pump Current Setting #1	111 (2.5 mA)
DB17 – DB19	Charge Pump Current Setting #2	111 (2.5 mA
DB20 – DB21	Power down state	00 (Normal Operation) (Unused AD4360s should be set to 11 Synchronous Powerdown)
DB22 – DB23	Prescaler value	00 (8/9)

Table 7 – Basic RX LO1 VCO/Synthesizer N-Counter Latch Settings

Latch Bits	Description	Default Value and Setting
DB00 – DB01	Latch select	10 Select N-Counter Latch
DB02 – DB06	A-Counter	00000 Determined by Desired Output Frequency See Tables 13A and 13B for Default Settings
DB07	Reserved	0
DB08 – DB20	N-Counter	0x00080 128, mid-range Determined By Desired Output Frequency See Tables 13A and 13B for Default Settings
DB21	Charge Pump Gain	0
DB22	Divide by 2	0 (Fundamental Output)
DB23	Prescaler Input select	0 (Fundamental Output)

Table 8 - Basic RX LO1 VCO/Synthesizer R-Counter Latch Settings

Latch Bits	Description	Default Value and Setting
DB00 – DB01	Latch select	01 Select R-Counter Latch
DB02 – DB15	R-Counter	0x0010 16, sets frequency step to 1 MHz
DB16 – DB17	Anti-backlash pulse width	00 (3.0 ns)
DB18	Lock detect precision	0 (3 consecutive cycles of phase delay less than 15 ns)
DB19	Test mode	0 Normal operation
DB20 – DB21	Band select clock divider	11 (Divide by 8)
DB22 - DB23	Reserve	00

The preceding default settings lead to the following values for the LO1 and LO2 VCO/Synthesizers.

Table 9 - Default values for the LO1A and LO2A ADF4360-2 (U5, U7 1.850-2.150 GHz)

(2000 MHz VCO Output, 4 MHz PFD, 16 MHz Reference Input, 8/9 RF Prescaler)

Latch	Default Values (Binary/Hex)
VCO/PLL Control Latch	DB00 – DB07: 00110100 (0x28) DB08 – DB15: 10011111 (0x01) DB16 – DB23: 11110000 (0x40)
VCO/PLL N-Counter Latch	DB00 – DB07: 01001000 (0x42) DB08 – DB15: 01111100 (0x80) DB16 – DB23: 00000100 (0x00)
VCO/PLL R-Counter Latch	DB00 – DB07: 10001000 (0x41) DB08 – DB15: 00000000 (0x00) DB16 – DB23: 00001100 (0x00)

(DB00, DB08, and DB16 are LSB)

Table 10 - Default values for LO1B and LO2B ADF4360-1 (U4, U6 2.150-2.425 GHz)

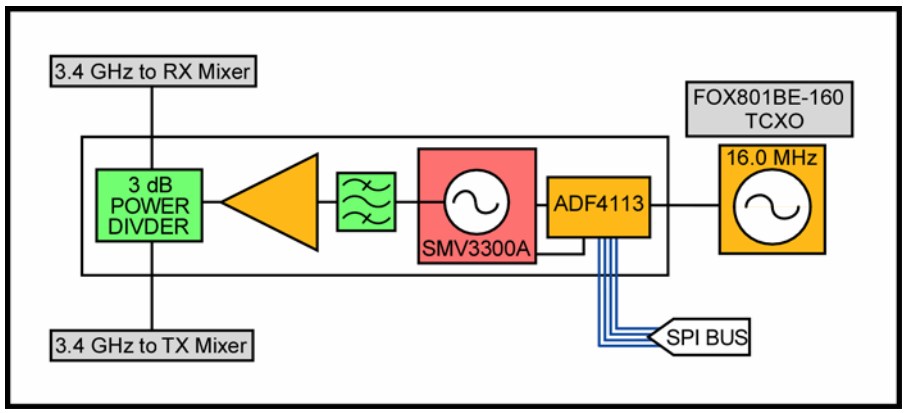
(2400 MHz VCO Output, 4 MHz PFD, 16 MHz Reference Input, 8/9 RF Prescaler)

Latch	Default Values (Binary/Hex)
VCO/PLL Control Latch	DB00 – DB07: 00110100 (0x28) DB08 – DB15: 10011111 (0x01) DB16 – DB23: 11110000 (0x40)
VCO/PLL N-Counter Latch	DB00 – DB07: 01000000 (0x42) DB08 – DB15: 11010010 (0x80) DB16 – DB23: 00000100 (0x00)
VCO/PLL R-Counter Latch	DB00 – DB07: 10001000 (0x41) DB08 – DB15: 00001100 (0x00) DB16 – DB23: 00001100 (0x00)

(DB00, DB08, and DB16 are LSB)

3.4 RX and TX LO3 PLL Frequency Synthesizer

The 1.850-2.425 GHz TX and RX IF frequencies are respectively up-converted to and down-converted from the 5.250 – 5.825 GHz band by a third local oscillator, called the RX and TX LO3. RX and TX LO3 is comprised of a Temperature Compensated Crystal Oscillator (TXCO), a Voltage Controlled Oscillator (VCO), and an Analog Devices ADF4113 Phased Locked Loop (PLL) frequency synthesizer device. LO3 is configured to output a fixed 3.4 GHz signal. The buffered 16 MHz output of the TCXO is also shared by RX LO1 and TX LO2.



The operation of the ADF4113 is briefly described here. For details and governing information, see the Analog Devices ADF4113 datasheet.

The output frequency of the PLL synthesizer is given by:

$$f_{VCO} = [(P \times B) + A \times f_{REF}] / R$$

Where:
f_{VCO} is the VCO output frequency
P is the preset modulus of the prescaler
B is the divide ratio of the 13-bit counter (3 – 8191)
A is the divide ration of the 6-bit “swallow” counter (0 – 63)
f_{REF} is the external reference frequency
R is the reference clock divisor (14-bits) to determine the output frequency spacing

There are a number of constraints on the configuration values.

1. The output frequency can be stepped in units of f_{REF} /R. The RF-5GHz board uses a 16 MHz reference frequency. We will set R to a value of 32 to obtain a frequency spacing of 1 MHz.
2. The output of the prescaler, f_{VCO} /P must be less than 200 MHz. Our maximum f_{VCO} is 3400 MHz so we will set P to a value of 32. The maximum prescaler output is then 106.25 MHz.
3. To generate our primary frequency f_{VCO} = 3.400 GHz, B = 26 and A = 18.

The synthesizer is controlled with four 24-bit registers called the Reference Counter Latch, the N-Counter Latch, the Function Latch, and the Initialization Latch. These are loaded via the SPI. The latches must be loaded in the order: Function Latch, Reference Counter Latch, and N-Counter Latch. Latch bits are numbered DB00 (LSB) through DB23 (MSB). DB23 (MSB) is loaded first. Data is shifted

into an internal holding register on the rising edge of the clock. When the component Load Enable (LE) signal goes from low to high, the held data is loaded into the register specified by DB01…DB00.

Table 10 - Default RX and TX LO3 Synthesizer Reference Counter Latch Settings

Latch Bits	Description	Default Value and Setting
DB00 – DB01	Latch select	00 (Select Reference Counter Latch)
DB02 – DB15	Reference Counter	00000000010000 (16 MHz) TCXO Reference Input Frequency
DB16 – DB17	Anti-backlash pulse width	00 3.0 ns
DB18 – DB19	Test Mode Bits (Reserved)	00 (Must be 00 for normal operation)
DB20	Lock detect precision	0 (3 cycles of phase delay less than 15 ns)
DB21 -DB22	Delay and Sync	01 (Delay Disabled Sync Enabled)
DB23	Reserved	0

Table 11 – Basic RX and TX LO3 Synthesizer N-Counter Latch Settings

Latch Bits	Description	Default Value and Setting
DB00 – DB01	Latch select	10 Select N-Counter Latch
DB02 – DB07	A-Counter	000100 Default value = 18
DB08 – DB20	B-Counter	010011000000 Default = 26
DB21	Charge pump gain	1 Charge pump current setting #2
DB22 – DB23	Reserved	00

Table 12 – Basic RX and TX LO3 Synthesizer Function Latch Settings

Latch Bits	Description	Default Value and Setting
DB00 – DB01	Latch select	11 Select Function Latch
DB02	Counter Reset	0 Normal operation
DB03	Power Down	0 Normal Operation (with DB21)
DB04 – DB06	Multiplexer output select	001 Select Digital Lock Detect
DB07	Phase detector polarity	1 Use on-chip VCO with passive loop filter
DB08	Charge pump output	0 Normal
DB09 – DB10	Fastlock enable and mode	10 Fastlock enabled Mode #1

DB11 – DB14	Timer Counter Control	0000 3 cycles
DB15 – DB17	Charge Pump Current Setting #1	111 0.29 – 8.7 mA depending on R R = 4700 Ohms CP current = 5mA
DB18 – DB20	Charge Pump Current Setting #2	111 0.29 – 8.7 mA depending on RR = 4700 Ohms CP current = 5mA
DB21	Power down state	0 Normal Operation (with DB03)
DB22 – DB23	Prescaler value	10 32/33

The preceding settings lead to the following values for the VCO/PLL latches:

Table 13 - Default RX and TX LO3 Synthesizer Settings

Latch	Default Values (Binary/Hex)
Reference Counter Latch	DB00 – DB07: 00000010 (0x40) DB08 – DB15: 00000000 (0x00) DB16 – DB23: 00000100 (0x00)
N-Counter Latch	DB00 – DB07: 10000100 (0x21) DB08 – DB15: 01010110 (0x6A) DB16 – DB23: 00000100 (0x00)
Function Latch	DB00 – DB07: 01001001 (0x92) DB08 – DB15: 01000001 (0x00) DB16 – DB23: 11111001 (0x80)
Initialization Latch	DB00 – DB07: 11001001 (0x92) DB08 – DB15: 01000001 (0x00) DB16 – DB23: 11111001 (0x80)

(DB00, DB08, and DB16 are LSB)

RX Intermediate Frequency Gain Control

A digital to analog convert (DAC) can be used to control the RF gain of the AD8347 Receiver Demodulator. Selection of Automatic Gain Control (AGC), or manual Intermediate Frequency (IF) gain control using DAC U2 is determined by the position of switch S1 on the 5 GHz RF PCB.

The Analog Devices AD8347 demodulates the first RX IF (1.850 – 2.450 GHz) into baseband quadrature signals RX_I and RX_Q). The frequency setting of RX LO1 determines the portion of the first IF range that is converted to baseband. The AD8347 has a RF gain control input (VGIN signal). The gain can be adjusted between -30 dB and +39.5 dB by setting the voltage on

the VGIN input to between 1.2 V and 0.2 V, respectively. Note, the higher voltage corresponds to a lower gain.
The RX IF gain control DAC is an Analog Devices AD5601, 8-bit device, with "rail-to-rail" DC output capability, controlled via a three wire SPI interface. The input shift register for the AD56X1 device family is 16 bits wide (see Table 15). The first two bits are control bits, which control the operating mode of the part (normal mode or any one of three power-down modes). The next 8 bits are the data bits, which are transferred to the DAC register on the 16th falling edge of SCLK. The information in the last six bits is ignored by the AD5601.
The input coding to the DAC is straight binary; therefore the ideal output voltage is given by:

$$V_{OUT} = V_{DD} \times \left[\frac{D}{2^N} \right]$$

where D is the decimal equivalent of the binary code that is loaded into the DAC register and ^{N} is the bit resolution of the DAC. V_{DD} is set by a resistive voltage divider (5.0 V analog power supply) and is nominally set to 3.3 V, providing the potential to vary the DC output from 0 V to 3.3 V, however DAC programming should limit the output to a maximum of 1.2V.

TX Gain Control DAC

A digital to analog convert (DAC) can be used to control the gain of the Transmit IF amplifier. The TX IF amplifier gain setting is used to adjust the TX RF Output Power level present at J2. The output of the DAC U9 is connected to the gain control of the BGA2031 TX IF amplifier.

The Phillips BGA2031 accepts a gain control voltage between 0 V and 2.7 V. The gain varies from approximately -33 dB (0.0 V) to +23 dB (~2.7 V).

The TX gain control DAC is another Analog Devices AD5601 8-bit device, which is the same part used to manually control the RX IF gain. The DAC is programmed via a three wire SPI interface in the same manner as the RX IF gain control DAC, as described in section 3.4.

The ideal output voltage is given by:

$$V_{OUT} = V_{DD} \times \left[\frac{D}{2^N} \right]$$

where D is the decimal equivalent of the binary code that is loaded into the DAC register and ^{N} is the bit resolution of the DAC.

V_{DD} is connected directly to the analog 3.3V power supply, providing the potential to vary the DC output from 0 V to 3.3 V; device programming should be implemented to limit the output to a maximum of 2.7 V.