Noise Performance of Gallium Arsenide Field-Effect Transistors

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Abstract—The Schottky-barrier gate gallium arsenide field-effect transistor (GaAs FET) is the first three-terminal, solid-state amplifying device to have demonstrated low-noise performance at X-band and higher. For example, noise figures approaching 3 dB at 10 GHz have been reported, while theory predicts still lower values.

After a brief review of the noise-generating mechanisms intrinsic to the GaAs FET, an enumeration is given of the various parasitic elements associated with the FET which affect the noise performance. These elements include, among others, the gate metallization and source contact resistances, drain-gate feedback capacitance, and source lead inductance. Numerous graphs are presented to illustrate the effects of these elements and the various design parameters on the noise performance.

A comparison is made between the theoretically predicted and the measured noise performance of microwave GaAs FET's.

The best state-of-the-art noise performance as reported by various laboratories is illustrated graphically for single-stage and multistage FET amplifiers.

Finally, some speculation is attempted in regard to the possible reductions in noise figure to be expected from technological and design improvements of GaAs FET's.

I. Introduction

THE GALLIUM arsenide Schottky-barrier field-effect transistor (FET) is the first three-terminal solid-state device to exhibit linear power amplification at X-band frequencies and higher. Its unique signal-handling capabilities and low-noise properties have been demonstrated by many workers. For example, noise figures approaching 3 dB at 10 GHz have been reported, while theory predicts still lower values.

The GaAs FET is now being used in low-noise amplifiers from low C-band and up. As such it nicely supplements the silicon bipolar transistor which still dominates at frequencies below C-band. However, with the noise reductions now being achieved with buffered-layer FET's, this frequency range will not long remain the sole province of bipolars. Fig. 1 is a comparison of the state-of-the-art performance of low-noise, narrow-band amplifiers using silicon bipolar transistors and GaAs FET's as of July 1975.

Gallium arsenide field-effect transistors also show potential as low-noise microwave mixers and oscillators [1]–[3]. In this paper we shall restrict ourselves to their performance as small-signal amplifiers.

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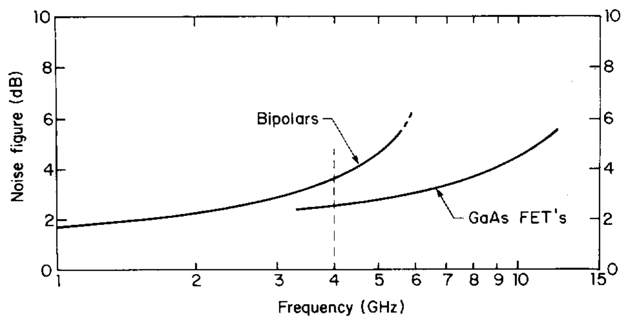


Fig. 1. Noise performance of cascaded (narrow-band) transistor amplifier stages as of July 1975.

As an introduction only a brief review of the present theory of noise of microwave GaAs FET's will be given, since a comprehensive description of the development of this theory has been given [4], [5]. Using this theory we shall assess the relative contributions to the noise performance by sources both intrinsic and extrinsic to the FET. With this as a background, we shall show how these contributions depend on the various material and design parameters at one's disposal. This will allow us to estimate the improvements in noise performance likely to be made in the future with advances in materials and device technology.

Finally, we will compare the theoretical predictions and measured results, and present a summary of the best noise performance obtained with FET devices and multistage amplifiers as of the writing of this paper.

II. Synopsis of the Noise Theory of the GaAs FET

The basic principle of operation of the field-effect transistor was first described by Shockley [6] who assumed a constant mobility throughout the conducting channel region. Van der Ziel, in a series of classic papers, used Shockley's model to derive the small-signal parameters [7] and intrinsic noise properties of the FET [8], [9]. Van der Ziel showed that the intrinsic noise is thermal in origin, and can be represented by two white noise generators, one in the drain circuit, and one in the gate circuit. The gate noise generator, which represents the noise induced on the gate electrode by the passing thermal fluctuations in the drain current, is partially correlated with the drain noise generator.

The constant mobility model of Shockley and van der Ziel, though applicable to long-gate devices, does not apply to microwave devices whose gate lengths are in the micron range. For these devices, when biased in the current saturation

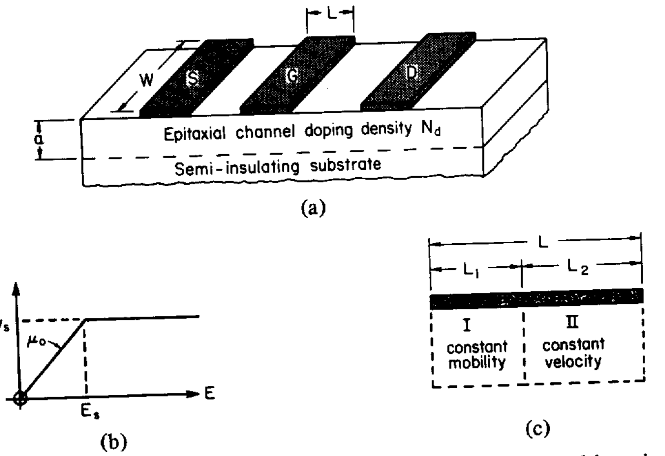


Fig. 2. Perspective sketch and two-section model of FET used in noise analysis. (a) FET model. (b) Assumed velocity-field characteristic. (c) Two-region model of channel.

regime, the average value of the longitudinal dc field in the channel is in the range where the mobility is a decreasing function of field, and indeed, where the carrier velocity is approaching a constant ("saturated") value. Consider, for example, a typical case of a GaAs FET with a 1 μm gate operating with a drain voltage of 3 V. The average longitudinal channel field is 30 kV/cm, approximately ten times the threshold value at which the velocity begins to saturate. Thus, the effects of velocity saturation must be included in any model of a GaAs FET designed for microwave operation.

Velocity saturation within the channel not only modifies the small-signal parameters, but the noise performance as well. Many workers have introduced some aspects of velocity saturation into their FET models, though none of these models include the diffusion noise introduced by electrons experiencing velocity saturation. In the noise and small-signal model developed at the authors' laboratory by Statz *et al.* and Pucel *et al.* [4], [5] this high-field diffusion noise is taken into account. It is the dominant intrinsic noise of microwave GaAs FET's.

A brief description of this model will be given now with the help of Fig. 2. Fig. 2(a) is a perspective sketch of a planar FET consisting of a source electrode (S), gate electrode (G), and drain electrode (D), all of width W. The gate length is denoted by L. The conducting n-type epitaxial channel of thickness a, situated on a semi-insulating substrate, is assumed to be uniformly doped at density N_d cm^{-3} with a low-field mobility μ_0. Typical values for these material parameters are $N_d \sim 10^{17}$ cm^{-3}, $a \sim 0.2 - 0.4$ μm, and $\mu_0 \sim 3000$–4500 cm^2/V $\cdot$ s.

Following Turner and Wilson [10], Statz *et al.* idealized the velocity-field characteristic by a piecewise linear approximation shown in Fig. 2(b). To obtain good agreement with experimental FET data, and reasonable agreement with experimental and theoretical velocity-field data [11], [12], the critical field E_s denoting the onset of velocity saturation was chosen to be 2.9 kV/cm, and the limiting velocity v_s to be 1.3×10^7 cm/s at room temperature.

This piecewise linear approximation to the velocity-field characteristic allows one to divide the conducting channel underneath the gate region into two zones as Grebene and Ghandhi [13] have suggested. In this two-zone model, shown in Fig. 2(c), a portion of the channel near the source end is assumed to be in the constant mobility regime, while the remaining portion near the drain end is postulated to be in velocity saturation. The position of the boundary between these two zones, representing the onset of velocity saturation, is a strong function of the source-drain bias, but a weaker function of the gate-source bias. The length of the velocity-saturated zone increases monotonically with source-drain bias.

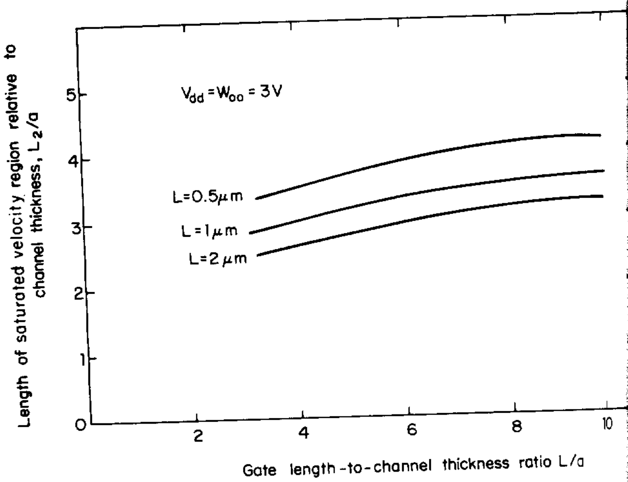


Fig. 3. Length of velocity-saturated zone relative to epi-layer thickness as a function of the gate length and the ratio of the gate length to epi-layer thickness.

By a correct application of this model, it can be shown that when the FET is biased in current saturation, that is, above the knee of the drain-voltage-current characteristic, the length of the velocity-saturated zone L_2 is of the order of two to four times the epitaxial layer thickness a [5]. Fig. 3 shows how the length of the velocity-saturated zone, relative to the channel thickness, varies as a function of the geometric ratio L/a for various gate lengths. The drain voltage V_{dd} is assumed to

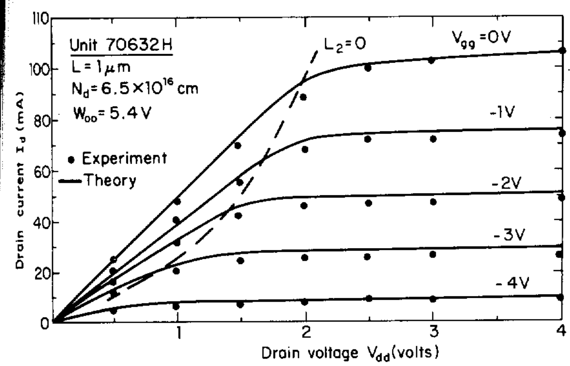


Fig. 4. Comparison between the theoretical and measured drain current-voltage characteristic for an X-band GaAs FET.

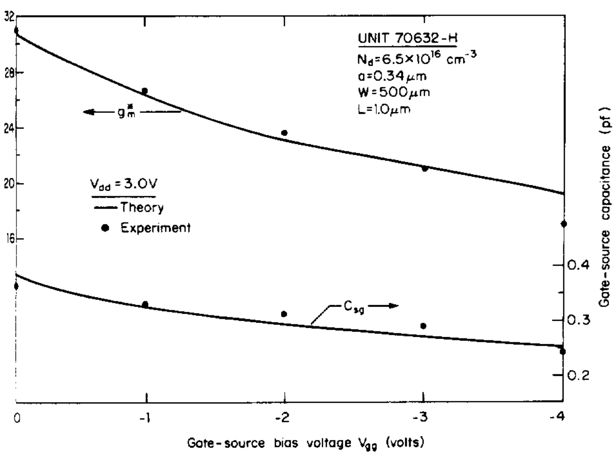


Fig. 5. Comparison between the theoretical and measured values of gate-source capacitance C_{sg} and terminal transconductance g_m^* for an X-band device.

equal to the intrinsic (internal) pinch-off voltage $W_{00} = 3$ V. With contemporary device designs using channel thicknesses of the order of 0.2–0.4 μm, the velocity-saturated zone comprises most of the channel length for gate lengths one micrometer or less. Thus, velocity saturation plays an important role in microwave GaAs FET's.

The piecewise linear approximation, chosen for analytic convenience, is an extreme idealization of the actual $v(E)$ characteristic in that it eliminates any negative resistance regime. In short-channel devices, the assumption of velocity saturation itself may be difficult to justify since the transit time of the electrons in the channel is comparable to the relaxation time of electrons, as Ruch [14] and later Maloney and Frey [15] have pointed out. Despite these recognized limitations, there *does* appear to be an appreciable degree of velocity saturation since this assumption works extremely well for the dc and small-signal characteristics. Fig. 4 demonstrates the agreement between the theoretical model and the measured I-V characteristic. Fig. 5 demonstrates this agreement for the small-signal terminal transconductance g_m^* and source-gate capacitance. The locus $L_2 = 0$ in Fig. 4 denotes the bias conditions for which velocity saturation first begins to manifest itself at the drain end of the gate. To the left of this line, that is, below the "knee" of the I-V characteristic, the channel

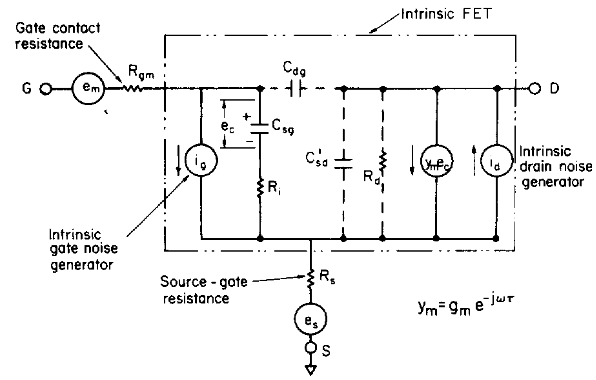


Fig. 6. Noise equivalent circuit of FET showing intrinsic and extrinsic noise sources.

is entirely in the constant mobility mode of operation. Thus, in the current "saturation" regime, i.e., to the right of the locus, the channel is always in velocity saturation over a portion of its extent. The FET is normally operated in this current-saturated mode.

We shall show later that using the two-zone model for the noise analysis, the agreement between the predicted and measured noise performance of GaAs FET's is equally as good as it is for the dc and small-signal properties, as demonstrated by Figs. 4 and 5.

Statz *et al.* [4] assume that the noise in zone I is thermal, as in the van der Ziel treatment, but enhanced by hot electron effects as postulated by Baechtold [16], [17]. Zone II, however, cannot be treated as an ohmic conductor. Its noise contribution (which is new in FET theory) is dominant in microwave devices and must be represented as a high-field diffusion noise as Shockley *et al.* [18] and van der Ziel [19] have shown.[1] This diffusion noise is proportional to the high-field diffusion coefficient and is linearly dependent on drain current [4], [5]. On the other hand, the thermal noise of region I decreases with increasing drain current. Although the high-field diffusion noise is high, a strong correlation (approaching unity) exists between the drain noise and the induced gate noise. This correlation leads to a high degree of cancellation in the noise output of the GaAs FET.

Fig. 6 is a noise equivalent circuit of the FET, valid for high frequencies. The noise generator i_g represents the induced gate noise of the intrinsic device (shown in dotted lines). Its mean-square value varies as the square of the frequency, i.e., ω^2. The intrinsic drain noise generator i_d has a flat spectrum. The coupling between these noise generators, represented by the correlation coefficient C

$$jC = \frac{\overline{i_g^* i_d}}{\sqrt{|\overline{i_g^2}|\,|\overline{i_d^2}|}} \tag{1}$$

[1] Actually, as van der Ziel [19] has shown, the noise of the constant mobility zone also can be represented as diffusion noise. Since the Einstein relation $D_0 = kT\mu_0/q$ holds in this zone, the diffusion noise expression can be transformed into the more familiar thermal or Johnson noise form. This transformation, of course, is invalid when velocity saturation occurs.

where (*) denotes the complex conjugate, and the overbar ($\overline{}$) represents a statistical average, approaches unity in magnitude for short-gate devices. (By comparison, in a constant mobility model, $|C| \sim 0.3$-0.4 [9].) In addition to the intrinsic noise sources, the parasitic source-gate resistance R_s and gate metallization resistance R_{gm} introduce thermal noise. This thermal noise is represented, respectively, by the generators labeled e_s and e_m. The resistance R_i represents the resistive charging path for the gate capacitance in the intrinsic FET. The noise associated with R_i is imbedded in the gate noise generator i_g [7].

It is not necessary to include all of the equivalent circuit parameters of the FET since some have a small effect on the noise figure. For example, for simplicity we shall neglect the (small) feedback drain-gate capacitance C_{dg} as well as the source-drain capacitance C_{sd}. The small perturbation of the noise figure produced by these capacitances can be added later if necessary. We may also neglect the small effect of the output drain resistance R_d, and any source lead inductance. We shall show later that inclusion of these parameters, for a well designed device, alters the minimum noise figure by at most a few tenths of a decibel. Thus, as a first approximation C_{dg}, C_{sd}, and R_d^{-1} will be assumed equal to zero. With these approximations, the equivalent circuit used in the noise figure derivation reduces to that shown in Fig. 7. This circuit also includes the signal source impedance Z_g and its associated thermal noise source e_g.

III. Noise Figure

The configuration shown in Fig. 7 with the source terminal common to input and output is often called the grounded-source or common source connection. Although we shall present the expression for the noise figure for this circuit, our results should apply with negligible error to the common-gate and common-drain configurations [20], [21].

The noise figure F can be expressed as the ratio of the sum of the mean-square noise components in the short-circuited drain-source path produced by all of the noise sources in Fig. 7 to the mean-square thermal noise current component produced by the signal source e_g alone.

By a straightforward (but lengthy) circuit analysis the noise figure can be written in the form

$$F = 1 + \frac{1}{R_g}\left(r_n + g_n |Z_g + Z_c|^2\right) \tag{2}$$

where R_g is the real part of the source impedance (assumed to be at the reference temperature $T_0 = 290$ K). The parameters r_n and g_n are the so-called noise resistance and noise conductance, respectively, and Z_c the correlation impedance [22].

In terms of r_n, g_n, and Z_c all the noise properties of the FET with parasitic resistances are embodied in a very simple noisy network shown in Fig. 8, which precedes the FET (now considered noise-free). Thus, r_n represents a thermal noise voltage generator at the reference temperature; g_n, a shunt thermal noise current generator at the same temperature; and Z_c, an impedance at absolute zero (noiseless). The noise figure of

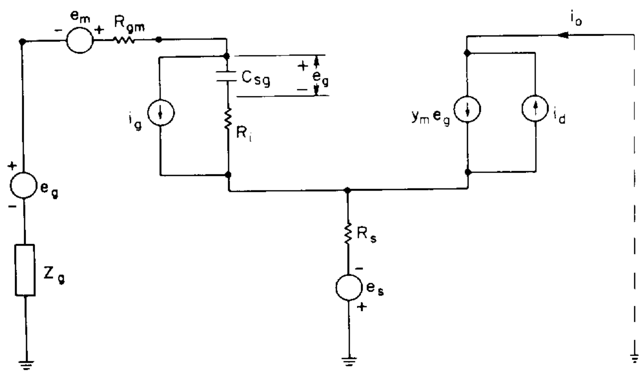


Fig. 7. Simplified equivalent circuit used in noise analysis of FET.

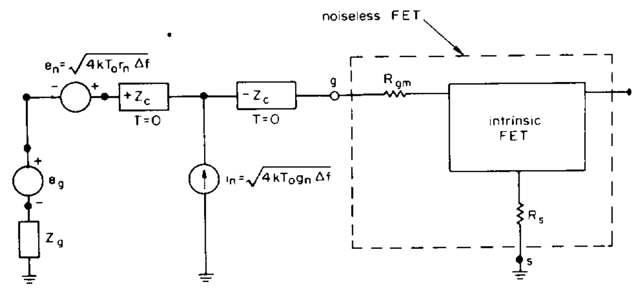


Fig. 8. Representation of noisy FET by a noiseless FET preceded by a noise network.

this combined network is the same as that of the original noisy FET, Fig. 7.

The noise functions are given by the simple expressions [5]

$$r_n = (R_s + R_{gm})\frac{T_d}{T_0} + K_r\left(\frac{1 + \omega^2 C_{sg}^2 R_i^2}{g_m}\right) \tag{3a}$$

$$g_n = K_g \frac{\omega^2 C_{sg}^2}{g_m} \tag{3b}$$

$$Z_c = R_s + R_{gm} + \frac{K_c}{Y_{11}} \tag{3c}$$

where T_d is the temperature of the FET. The parameters K_g, K_r, and K_c are numerical noise coefficients which represent the properties of the intrinsic noise generators i_g, i_d and their correlation (1). For an FET not at room temperature, these noise coefficients, as well as the small-signal parameters g_m, R_i, C_{sg}, the parasitic resistances R_s and R_{gm}, and the input impedance Y_{11}^{-1} of the intrinsic device, Fig. 7, given by

$$Y_{11}^{-1} = R_i + \frac{1}{j\omega C_{sg}} \tag{4}$$

are assumed to be evaluated at the device temperature T_d.

IV. Minimum Noise Figure

The first stage of a low-noise amplifier chain is often designed to have a minimum noise figure. The noise figure is optimized by the proper choice of the source impedance $Z_g = R_g + jX_g$. This optimization can be achieved by a suitable lossless matching network between the signal source and the input (gate-source) terminals of the FET. It is easy to show that the minimum noise figure is achieved when the real and imaginary parts of the source impedance are equal to

$$R_g = R_{g0} = \sqrt{R_c^2 + \frac{r_n}{g_n}} \tag{5a}$$

$$X_g = X_{g0} = -X_c \tag{5b}$$

where R_c and X_c are the real and imaginary parts of the correlation impedance. The minimum value of F corresponding to this "noise match" can be expressed as

$$F_{\min} = 1 + 2g_n(R_c + R_{g0}). \tag{6}$$

In decibels, $F_{\min}$ (dB) = $10 \log_{10} F_{\min}$.

When the source is not optimized for best noise performance, the noise figure is given by

$$F = F_{\min} + \frac{g_n}{R_g}\{(R_g - R_{g0})^2 + (X_g - X_{g0})^2\}. \tag{7}$$

We shall refer to this equation later when we discuss the experimental procedure for determining $F_{\min}$.

The expression for $F_{\min}$ given by (6) can be written to a very good approximation by the simple three-term power series expansion in frequency

$$F_{\min} = 1 + 2\left(\frac{\omega C_{sg}}{g_m}\right)\sqrt{K_g[K_r + g_m(R_s + R_{gm})]} + 2\left(\frac{\omega C_{sg}}{g_m}\right)^2 [K_g g_m(R_{gm} + R_s + K_c R_i)] + \cdots \tag{8}$$

valid at room temperature. This simplified form delineates the roles played by the noise sources intrinsic to the device, embodied in the noise coefficients K_g, K_c, and K_r and the noise sources corresponding to the parasitic resistances R_s and R_{gm}. The frequency dependence of $F_{\min}$ is a consequence of the ω^2 dependence of the induced gate noise. Note that $F_{\min}$ decreases with increasing gain-bandwidth factor g_m/C_{sg} of the FET. The gain-bandwidth factor is a function of gate bias, eventually decreasing as the gate bias approaches the pinch-off condition. In terms of g_m and C_{sg} individually, note that $F_{\min}$ increases with gate capacitance but decreases approximately in proportion to the inverse of the transconductance.

The noise coefficients are frequency-independent numerical factors which are gate-bias dependent, and to a lesser extent, drain-bias dependent. A typical bias dependence of these coefficients is shown in Fig. 9. Note that K_r is an order of magnitude lower than K_g and K_c. The bias dependence is expressed in terms of the drain current I_d normalized to its value I_{dss} at zero gate bias. All three noise coefficients depend in a complicated manner on gate length, channel thickness, and other parameters [5]. Observe that K_g is a strong function of the drain current, increasing at a rate faster than linear with I_d at high currents.

It is evident from (8) that $F_{\min}$ can be lowered by minimizing the parasitic resistances R_s and R_{gm}. As we shall see later, it also can be lowered by a proper choice of gate bias, or equivalently, drain current since the noise coefficients as well as the small signal parameters (mainly g_m) are bias-dependent.

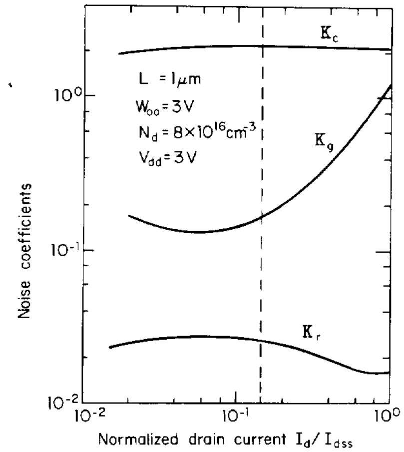


Fig. 9. Drain current dependence of noise coefficients of a GaAs FET for a specific set of design parameters and drain voltage.

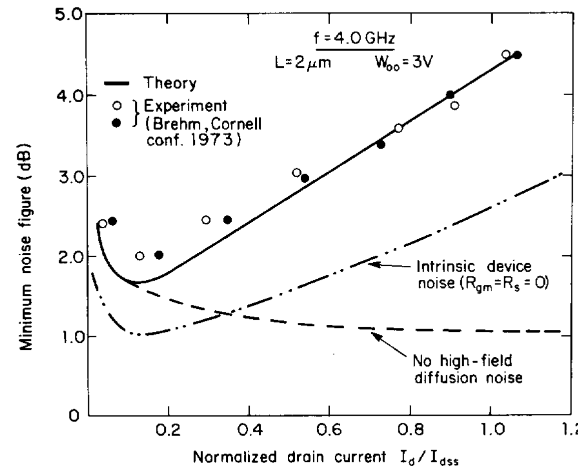


Fig. 10. Theoretical and measured noise figure for a GaAs FET with a 2 μm gate.

V. Comparison of Theory and Experiment

The applications of the two-zone noise model to practical GaAs FET's will be exemplified now.

The solid line in Fig. 10 illustrates the validity of the noise model applied to a device with a 2 μm gate [23]. The nearly linear current dependence of $F_{\min}$ in the high current range demonstrates clearly the contribution of the high-field diffusion noise produced in the velocity-saturated zone. This fact is emphasized further by the lowest dashed line which represents $F_{\min}$ if this diffusion noise were set equal to zero. The increase in $F_{\min}$ at low currents is attributable to the decrease in g_m and the increase in the noise contribution of zone I as pinch-off is approached. The important role played by the parasitic resistances is illustrated by the middle dashed line representing the intrinsic noise obtained by setting R_{gm} and R_s equal to zero. Note that at the minimum the parasitic resistances contribute nearly half of the noise. Fig. 11 illustrates the agreement obtained with the noise data reported for a 1 μm gate device [24]. Again the general features of the bias dependence of $F_{\min}$ are reproduced. If we allow for the

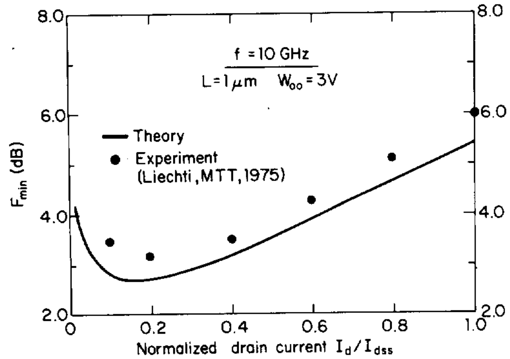


Fig. 11. Theoretical and measured noise figure for a GaAs FET with a 1 μm gate.

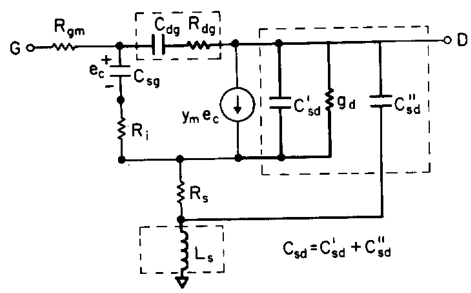


Fig. 12. Inclusion of neglected elements in equivalent circuit for noise figure analysis.

possible measurement uncertainty in the value of the noise figure, which may amount to as much as ±0.4–0.5 dB, the difficulty in accounting for the circuit losses accurately, and the errors introduced by use of the simplified equivalent circuit, the agreement between theory and experiment can be considered satisfactory.

VI. Effects of Neglected Parasitics

We shall assess now the effects of including the equivalent circuit elements neglected in the derivation of the noise figure in Section III. Fig. 12 illustrates these parasitics (delineated by dashed lines). They are, principally, the source-drain capacitance C_{sd}, drain conductance $g_d = R_d^{-1}$, source lead inductance L_s, and the drain-gate feedback admittance Y_{12} represented by a resistance R_{dg} in series with the drain-gate capacitance C_{dg}. This resistance (which is assumed to generate thermal noise) represents the resistive charging path for C_{dg} between the drain and gate terminals as suggested by Vendelin [25] and others. It is possible to include the effects of these parasitics in an exact manner; however, the resultant expression for the noise figure is unwieldy. Fortunately, for the small values of these neglected elements, typical of well-designed FET's, the perturbations to the minimum noise figure are linear functions of the element values, and can be added algebraically to the expression for $F_{\min}$, (6).

Furthermore, since these perturbations are small in comparison to $F_{\min}$, as we shall show, the corrections to $F_{\min}$, expressed in decibel form, are also linear. If we denote the perturbation to $F_{\min}$ by ΔF, where the latter represents the inclusion of one of the neglected elements, or any combination of them, then the correction ΔF, expressed in decibels, is given by

$$\Delta F\,(\mathrm{dB}) = 10 \log_{10} \frac{F_{\min} + \Delta F}{F_{\min}} \tag{9a}$$

$$= 4.34 \ln\left(1 + \frac{\Delta F}{F_{\min}}\right) \tag{9b}$$

$$\approx 4.34 \frac{\Delta F}{F_{\min}} \tag{9c}$$

where the last equation arises from the assumption $|\Delta F| \ll F_{\min}$. If this is not true (9a) must be used.

We shall now demonstrate the magnitude and sign of these corrections to $F_{\min}$ for the 1 μm gate device discussed earlier. The corrections as evaluated here apply for the bias conditions corresponding to the lowest value of $F_{\min}$, namely 2.75 dB. See Fig. 11.

Unfortunately, we do not have the values of the neglected parasitic elements for the specific 1 μm device discussed earlier. However, since we are discussing small perturbations, we may use the element values obtained by Vendelin [25] for a similar device [26] by a computer optimized fit to the S-parameters. These are $C_{sd} = 0.16$ pF, $R_d = g_d^{-1} \approx 200\ \Omega$, $C_{dg} \approx 0.014$ pF, $R_{dg} \approx 660\ \Omega$, and $L_s \approx 26$ pH.

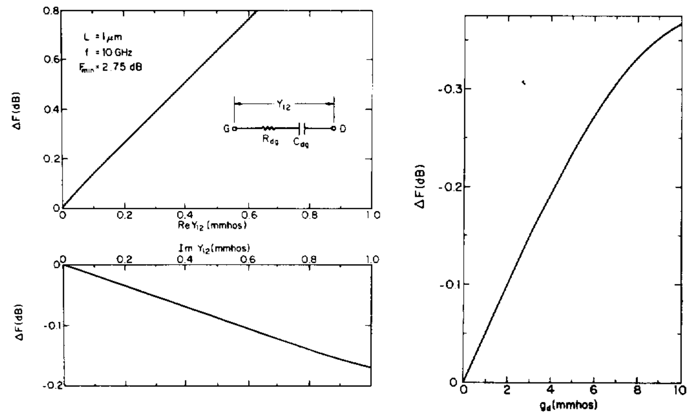
Consider first the inclusion of the drain-gate feedback, illustrated in Fig. 13(a) for a range of feedback admittances Y_{12}. As one might expect, the resistive feedback increases the noise figure. On the other hand, the capacitive component decreases it, in accordance with the findings of others [27]. For the specific values of the feedback elements, Re Y_{12} = 0.38 m℧, Im Y_{12} = 0.66 m℧, the corresponding corrections to the noise figure are $\Delta F = 0.45$ dB and $\Delta F = -0.12$ dB, or a net change of +0.33 dB.

We turn next to the inclusion of the output admittance consisting of g_d and C_{sd} in shunt, shown in dotted lines in Fig. 12. Since there is still some uncertainty amongst workers in the field as to the fraction of the source-drain capacitance which should be terminated at the upper end of R_s, as shown in Fig. 12, and the fraction that should tie to the lower end, we shall only consider the perturbation caused by inclusion of the drain output conductance. This is illustrated in Fig. 13(b). As is evident, the correction is negative. For the stated output resistance g_d = 5 m℧, $\Delta F = -0.24$ dB.

The effect of source lead inductance is of second-order importance. For values of this inductance in the range below 200 pH, the noise figure decreases slightly. This range exceeds by almost an order of magnitude the values of parasitic source lead inductance in a well designed device. For the specific value of inductance of the device under consideration, $\Delta F \approx -0.01$ dB.

Thus taken together, all of the neglected parasitics considered increase the noise figure by about 0.1 dB. This is a negligible error. Therefore, for a well designed device, use of the simplified model for noise analysis shown in Fig. 7 is justified.

It must be cautioned that the corrections implied by Fig. 13(a) and (b) apply only to the device considered in the text.



(a) (b)

Fig. 13. Corrections to minimum noise figure attributable to neglected equivalent circuit elements. (a) Corrections to F_{min} at 10 GHz attributable to drain-gate feedback. (b) Corrections to F_{min} attributable to drain resistance.

Although corrections for other devices of similar design will be comparable, the quantitative values necessarily will be different.

It should be mentioned in passing that since the noise figure decreases with capacitive feedback, one might use this as a means for improving the noise performance of an FET amplifier by external feedback [27]. We do not believe this to be a satisfactory approach for several reasons. First, increasing feedback in this manner reduces the stability factor of the FET [28]. Second, the available gain decreases. Third, since it is the noise measure, rather than the noise figure that one should minimize, as we shall argue later, no improvement is achieved since noise measure does not change under capacitive feedback, or for that matter, for any lossless feedback scheme, as Haus has shown [29].

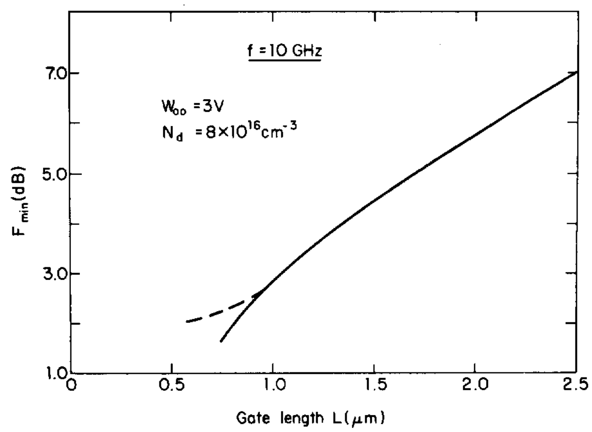


Fig. 14. Theoretical minimum noise figure as a function of gate length.

VII. Theoretical Dependence of Noise Figure on Device Geometry and Parasitic Resistances

We shall use the results of the noise theory described earlier to show how the noise sources intrinsic and extrinsic to the FET depend on the various material and geometrical parameters at the disposal of the device designer. With this as a background, we estimate the improvements likely to be made in the future with advances in materials and device technology. Specifically, we shall discuss the dependence of the noise performance on gate length, frequency, and extrinsic parasitic resistances.

We will limit ourselves, for convenience, to a specific design based on a channel doping density $N_d = 8 \times 10^{16}$ cm^{-3} and intrinsic pinch-off voltage $W_{00} = qN_d a^2/2\kappa\epsilon_0 = 3$ V typical of contemporary microwave devices where $\kappa = 12.5$ is the dielectric constant of GaAs. However, the general conclusions to be drawn will also apply to other microwave devices with similar, though not identical, design parameters.

Dependence of Minimum Noise Figure on Gate Length

The dependence of F_{min} on gate length is embodied in the source-gate capacitance and transconductance, and in a more complicated manner in the noise coefficients. The theoretical value of F_{min} at $f = 10$ GHz, as a function of gate length, is illustrated in Fig. 14. Notice the rapid rate of decrease of F_{min} as the gate length approaches 1 μm. Gate length reduction is the single most productive means of improving the noise performance of an FET—up to a point! Although our theoretical curve extends down to $L = 0.5$ μm, we show an additional, arbitrarily drawn dashed line, since we believe the validity of our theory becomes questionable below $L = 1$ μm, for the channel thickness ($a \approx 0.225$ μm) corresponding to the assumed value of N_d and W_{00}.

Below $L = 0.5$ μm, there are other, more fundamental reasons why we believe that the rate of decrease in F_{min} will "flatten out" as implied by the dashed line.

First, as the gate length continues to decrease below a micron, the fringing capacitance of the gate (which does not decrease with gate length) [5] puts a lower asymptote on the gate capacitance; and hence on F_{min} [see (8)]. For example, for $L = 0.5$ μm, this fringing capacitance is over 30 percent of the gate capacitance.

Second, unless the channel thickness is reduced correspondingly, in accordance with the gate length, the electric field in the channel will begin to deviate markedly from a longitudinal field configuration, to one conforming more to a cylindrical

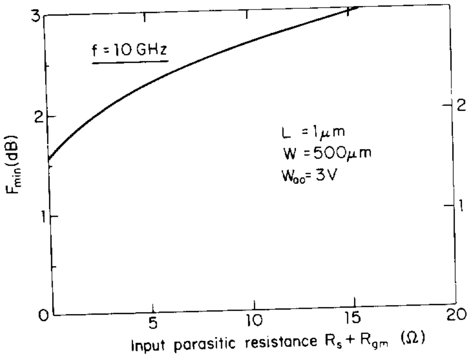


Fig. 15. Theoretical dependence of minimum noise figure on parasitic resistances for a GaAs FET with a 1 μm gate.

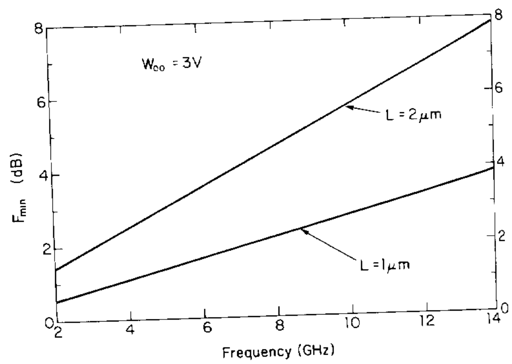


Fig. 16. Predicted frequency dependence of minimum noise figure of GaAs FET for two values of gate length.

pattern about the gate electrode. The reduced longitudinal component of the electric field leads to a diminished control of the electron flow by the gate potential and to a "softer" drain current-voltage saturation characteristic [30], [32]. Although the noise performance and gain will still improve with decreasing gate length, the rate of improvement should decrease.

If the channel thickness is reduced in proportion to the gate length to reestablish a longitudinal field pattern, this requires use of epitaxial layers 0.1 μm thick, or less. Most of the channel doping profile, in this case, will not be constant, but will be decreasing rapidly toward the substrate. This means that the rate of decrease of transconductance with gate bias will be faster than it would be for an ideal (step) profile. Thus the upturn in $F_{\min}$ with decreasing drain current will occur at a higher value of drain current. Hence, the advantages of reducing both gate length and channel thickness, simultaneously, will be partially nullified. Although there appears to be some promise of growing epitaxial layers with a steeper transition zone, eventually one is limited to a lower value of the transition zone fixed by the Debye length [32].

There is another limitation imposed by thinner channel layers, namely, the increase in source gate resistance which must accompany a reduced epitaxial layer.

All of the above considerations must be taken into account in matching the possible advantages of reducing gate lengths much below a micrometer against the additional cost and complexity of producing submicron gate devices with acceptable yield.

Dependence of Minimum Noise Figure on Parasitic Gate and Source Resistance

The theoretical dependence of $F_{\min}$ on the parasitic resistances is shown in Fig. 15. Values of $R_s + R_{gm}$ typical of contemporary devices fall in the range from 8-11 Ω for a 500 μm wide gate device. A reduction of the order of perhaps 0.5 dB might be possible with improvements in the design and technology of contacts.

Dependence of Minimum Noise Figure on Frequency

The predicted frequency dependence of $F_{\min}$ is illustrated in Fig. 16 for two gate lengths. Note that the curves are nearly linear with frequency. This frequency dependence is exhibited by experimental data also, as we shall demonstrate. The noise degradation with increasing frequency is attributable to the frequency dependence of the induced gate noise.

The theoretical noise figures displayed in the previous graphs were all computed for channel doping profiles exhibiting a slope near the epi-substrate interface—that is, for a nonrectangular profile, representative of present epitaxial layers. Some further reductions in the noise figure can be expected as "steeper" transition zones are achieved by improvements in the technology of epitaxial growth.

VIII. Measurement of Noise Figure

Introduction

In this section we shall discuss some of the practical problems in determining the minimum noise figure peculiar to the FET, and the means for overcoming these difficulties.

Earlier we had demonstrated the strong bias dependence of the minimum noise figure and had mentioned that the gain is also bias-dependent. We also pointed out that not only are the lowest noise figure and the maximum available gain achieved at different gate bias values, but that at a given bias condition, the matching conditions for the best noise figure and highest available gain also differ. This is one problem.

Next, the gain associated with the lowest value of the noise figure of present GaAs FET's is not high enough, at least at the upper end of the microwave band, to permit one to neglect in a noise measurement the correction for postamplifier or mixer noise. Thus it is a very tedious procedure to determine the minimum noise figure of an FET by simply varying the tuning adjustments of the input matching circuit because the correction also varies, nor is it a very precise method.

Equation (7) suggests a more direct approach. Note that this equation contains four unknowns, $F_{\min}$, g_n, R_{go}, and X_{go}. Thus, at each bias one may, in principle, ascertain $F_{\min}$ and the remaining noise parameters by measuring the noise figure and gain for four selected source impedances.[2] However, unless these impedances are chosen judiciously, so that the resultant noise figures do not all cluster near $F_{\min}$, or conversely, be all far removed from $F_{\min}$, large errors can be

[2] It is necessary to measure the gain in order to correct for the postamplifier and/or mixer noise.

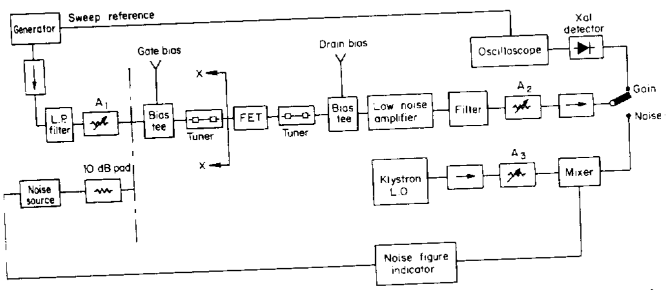


Fig. 17. Experimental set-up for measurement of the microwave gain and noise figure of an FET.

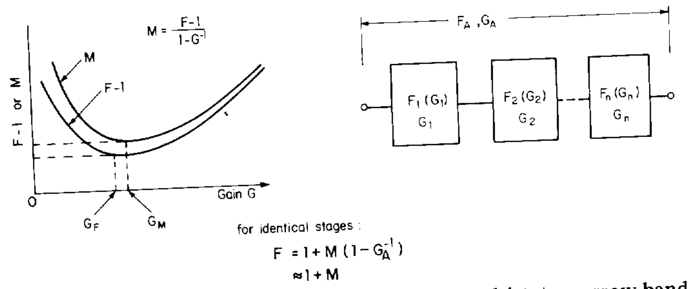


Fig. 18. Relevant to the design of a low-noise multistate, narrow-band FET amplifier.

introduced in the computation of $F_{\min}$. To avoid this pitfall, it is advisable to use more than four measurements.

One such method, widely used [33] is based on seven chosen source impedances and seven noise figure and gain measurements. These seven values, and the corresponding noise figures, are used to obtain the best fit to the four unknown noise parameters (actually four others derived from these) in the minimum mean-square error sense. Naturally, more than seven source impedances may be used, but this lengthens the measurement procedure, and the point of diminishing returns is soon reached.

Noise Measurement Setup

A typical microwave setup to measure the gain and noise figure of FET's is shown in Fig. 17.

The FET is tuned with two coaxial double slug tuners which present very low loss (<0.2 dB) thus reducing the error correction in the noise figure measurement. The low-pass filter at the input eliminates errors in gain measurements due to harmonics; the narrow-band tunable filter (a high-Q cavity) at the output eliminates the image frequencies which would affect the noise measurement.

The gain is measured by a substitution method with a constant level maintained at the output of the crystal detector shown on the oscilloscope. The input level to the FET is adjusted with the attenuator A_1. With the FET and tuners removed, the attenuator A_2 is set at zero and a convenient level set on the oscilloscope. Then the FET is introduced in the circuit and A_2 adjusted to reestablish the original level. The gain is read directly on A_2. With this procedure one must be careful to adjust A_1 such that the saturation level of the low noise amplifier is never approached.

The low-noise amplifier is an essential part of the setup. It facilitates the tuning of the FET for minimum noise and reduces the postamplifier correction. If the noise figure of the postamplifier is F_2 and the noise figure and gain of the FET stage are F_1 and G, respectively, the measured noise figure at the input is given by

$$F = F_1 + \frac{F_2 - 1}{G}. \tag{10}$$

At high microwave frequencies, 10 GHz and higher, the gain G is generally low, less than 6 dB. If F_2 is large, the second term on the right of (10) can be comparable to F_1. In that case, by tuning the FET, one would more likely minimize F by maximizing G rather than minimizing F_1.

The noise figure is measured either with an automatic noise figure indicator such as AILTECH Model 75 or with a receiver and calibrated attenuator, by the so-called Y-factor method. The pad in front of the noise source is necessary only if the source impedance varies with its state (on or off). The attenuation must be taken into account in the noise calculations.

First, the noise figure F_2 of the postamplifier–mixer stages must be determined carefully. Then for a given bias condition of the FET, the output tuner is adjusted for maximum gain and the input tuner for minimum noise. The value of the noise figure measured is recorded together with its associated gain, and F_1 is calculated from (10). It can then be corrected if necessary for input circuit losses. The impedance seen by the FET input is measured (at the plane X–X on Fig. 17) with a network analyzer. This series of measurements is repeated seven times with the input tuner adjusted for slightly different positions each time.

The data are then processed by a computer to obtain $F_{\min}$, g_n, and the optimum source impedance $Z_{g0} = R_{g0} + jX_{g0}$, as described earlier.

This procedure is long and tedious. It can be simplified if many measurements have to be made in the same frequency range. In that case, one can use a set of seven preadjusted tuners which are interchanged for each measurement.

IX. Design Considerations for Cascaded Amplifier

It was mentioned earlier that the lowest noise figure and the highest power gain do not occur at the same bias and tuning conditions. Since the gain at the minimum noise figure condition is not usually high enough to allow one to neglect the noise of the second and succeeding stages, one should not design the first stage of an FET amplifier to have its minimum noise figure if a minimum noise figure for the overall amplifier is to be achieved.

We shall illustrate why this is true with the help of Fig. 18. Shown is a block diagram of a cascaded stage amplifier, assumed to be narrow-band.[3] Since to each value of gain, G, there corresponds a noise figure, F, we have denoted this correspondence as $F(G)$. From the formula for the noise

[3] For wide-band amplifiers, other considerations enter besides noise figure.

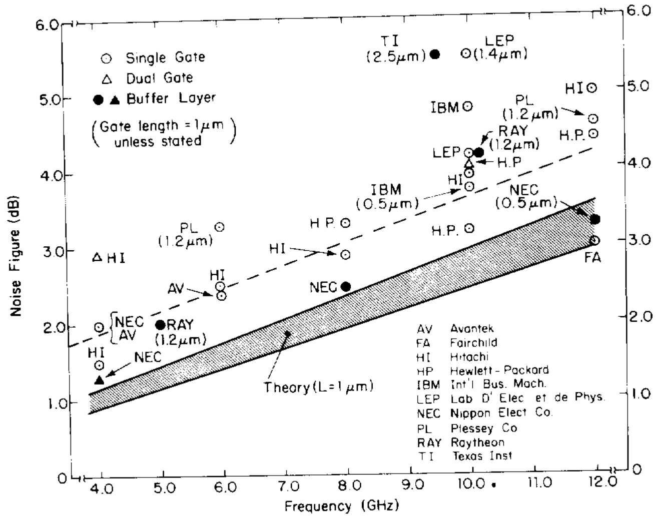


Fig. 19. Noise performance of GaAs FET's obtained at various laboratories (July 1975).

figure of cascaded stages, we find for the overall noise figure of the amplifier

$$F_A = F_1(G_1) + \frac{F_2(G_2) - 1}{G_1} + \frac{F_3(G_3) - 1}{G_1 G_2} + \cdots + \frac{F_n(G_n) - 1}{G_1 G_2 G_3 \cdots G_{n-1}} \tag{11}$$

where the subscript denotes the amplifier stage number. For convenience of our discussion we shall assume identical stages $G_1, G_2, G_3, \cdots, G_n = G; F_1, F_2, F_3, \cdots, F_n = F$. Then (11) becomes

$$F_A = 1 + (F - 1)\left(1 + \frac{1}{G} + \frac{1}{G^2} + \cdots \frac{1}{G^{n-1}}\right) \tag{12a}$$

$$= 1 + M\left(1 - \frac{1}{G_A}\right) \tag{12b}$$

where $G_A = G^n$ is the power gain of the amplifier, and $M = M(G)$ is the noise measure of each stage,

$$M(G) = \frac{F(G) - 1}{1 - \dfrac{1}{G}}. \tag{13}$$

Equation (12b) is equivalent to the statement that the noise measure of n identical cascaded stages is equal to the noise measure of an individual stage [29].

It is evident that in cascade design, where the overall gain G_A is prescribed, one should minimize the noise measure rather than the noise figure of each stage to minimize the overall amplifier noise figure. When the overall gain is high, $F_A = 1 + M(G_A^{1/n})$. The sketches in Fig. 18 show qualitatively how the noise measure and noise figure vary as a function of stage gain. The minimum noise measure usually occurs at a slightly higher current and gain than the minimum noise figure. Also the value of the minimum noise measure exceeds the minimum value of the excess noise figure of a stage, i.e., $M_{\min} > F_{\min} - 1$. It follows that the lowest possible value of the amplifier noise figure is greater than the minimum noise figure of any individual stage, that is $F_{A,\min} > F_{\min}$. This, of course, is what one would expect. However, when the gain per stage is of the order of 6 dB or more at the bias condition corresponding to minimum stage noise figure, then the difference between $F_{A,\min}$ and $F_{\min}$ is small. For example, for the 1 μm gate device described by Fig. 11, the lowest measured value of $F_{\min}$ = 3.2 dB [24]. The computed value of $M_{\min}$ = 3.6 dB. Hence for a three-stage amplifier, with $\approx$7.5 dB gain per stage, the amplifier noise figure F_A = 3.63 dB, only 0.43 dB greater than the single-stage minimum noise figure.

X. Summary of Noise Performance Obtained at Various Laboratories

We shall present now a compilation of the best noise performance reported by laboratories around the world as of the time of this writing (July 1975). First, the results for single-stage amplifiers (devices) will be given, then cascaded narrow-band amplifiers, and finally, wide-band amplifiers.

Fig. 19 is a graphical presentation of the device performance reported. All devices have 1 μm gates, except where noted. The circles refer to single-gate FET's, the triangles to dual-gate devices. Also shown (by the shaded strip) is the theoretical noise figure for a 1 μm gate for a spread of parasitic resistance values typical of present devices. Note that the buffered-layer device performance is within 0.5 dB of the theoretical.[4] Inclusion of circuit losses and corrections for neglected parasitics will reduce this gap.

Use of buffered layers not only improves the performance of single-gate devices, but also of dual-gate devices as the low noise figure for the NEC device at 4 GHz testifies.

The advantages of buffering are emphasized even more dramatically by the noise performance reported for cascaded narrow-band amplifiers (bandwidth $<$20 percent) shown in

[4] A buffered-layer device is one that has an epitaxial growth of a high resistivity layer, of the order of 5–10 μm thick, over the substrate prior to channel epitaxial growth.

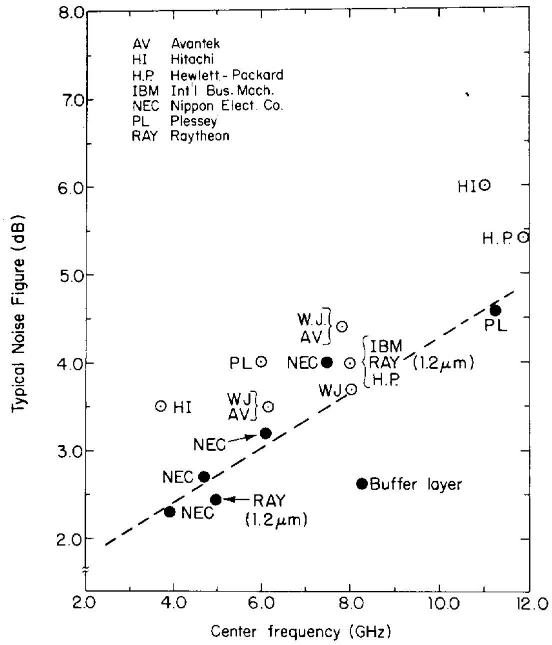


Fig. 20. Noise performance of narrow-band GaAs FET amplifiers as reported by various laboratories (July 1975).

Fig. 20. Notice in particular that the improvement is most pronounced in *C*-band and in the lower end of *X*-band.

Buffering appears to improve the noise performance in several ways. First, it covers or "shields" interface traps from the channel. (Present conjecture is that these traps, their nature unknown, may be ionized by the high channel fields and generate a noise spectra extending up to at least the low microwave band.) Second, with a buffer layer, the channel mobility near the substrate side increases substantially above the values with no buffer layer [34]. This not only increases the transconductance of the FET, but also decreases the source-gate parasitic resistance R_s. Reductions in R_s by nearly a factor of two are observed. These latter two improvements also lead to a higher power gain.

It seems reasonable to assume that the noise improvement in *C*-band and below can be attributed mainly to the reduction in trap noise. On the other hand, in the upper end of *C*-band and higher, where the trap noise would be expected to have diminished significantly, it is the increase in g_m and the reduction in R_s that is primarily responsible for the improvement in the noise performance. (Note the greater sensitivity of the noise figure to variation in parasitic resistance at the higher end of the frequency band exhibited by the theoretical shaded region in Fig. 19.)

It is interesting to note that the dashed lines through the experimental data in Figs. 19 and 20 both have approximately the same slope, namely 0.3-0.35 dB/GHz, as the theoretical lines in Fig. 19. However, the amplifier noise figures, on the average, exceed the single device values by approximately 0.5-0.6 dB.

Fig. 21 is a sampling of the noise performance reported for wide-band amplifiers. The upper and lower values of F_{min} in each case are not to be construed as the value of F_{min} at the band edges but merely the upper and lower values within the

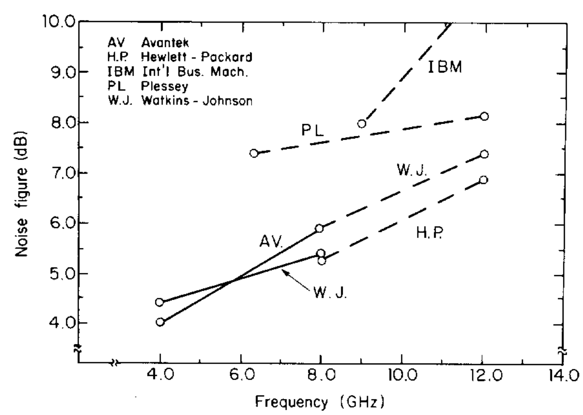


Fig. 21. Noise performance of some wide-band GaAs FET amplifiers (early 1975).

band. Since it is impossible to obtain a good noise match over a wide frequency range, the average noise figures are substantially higher than the narrow-band results.

XI. Conclusions

The measured noise figures of GaAs FET's with buffer layers are approaching the theoretically predicted values based on presently realizable channel doping profiles. With some advances in the design and technology of contacts and the achievement of steeper slopes in the doping profile at the substrate-channel interface, still further improvements in the noise performance should be possible.

It is believed that with the present planar device configuration, gate length reductions substantially below a micron will reach a point of diminishing returns. The reasons are 1) fringing gate capacitance, 2) slower rate of increase in transconductance, 3) increased series resistance of the channel layer, and

4) the need for an extremely narrow doping transition zone at the channel-substrate interface.

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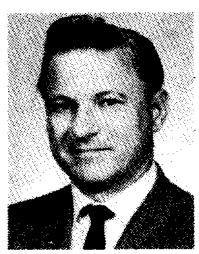

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