Performance of an Electrically Small Antenna Amplifier Circuit

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Abstract

A technique is presented to calculate the noise figure and available power gain for electricially small antenna amplifier circuits over a wide bandwidth. The method permits reasonable predictions of circuit performance solely from the manufacturer's transistor data, i.e., without resorting to extensive measurements. Results for a system designed for 10 kHz to 500 MHz coverage are presented. The agreement between the calculated and measured noise figures and available power gain is within 3 dB over most of the frequency range.

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Introduction

There often exist situations in which electrically small antennas must be used because of mechanical or other constraints. The disadvantages of employing them are well known and become greater when wide bandwidths (e.g., a decade or more) are required. System sensitivity can be adversely affected by the high antenna impedance in receiving applications. Also, narrowband tuning to improve performance is difficult or undesirable for a remotely located antenna or one that feeds several receivers. One approach is to design a wideband amplifier that becomes an integral part of the antenna to provide an interface between the antenna and receiver and to establish a reasonable system noise figure. Meinke has done considerable experimental work in this area although the bandwidth used in that paper is not as wide as the one used here [1,2]. One of the most significant analytical efforts in the area of active antennas is that of Wong [2]. What is still needed is a simple analytical procedure to predict antenna-amplifier performance without resorting to time-consuming measurements of transistor characteristics before the design is actually started. This paper describes the technique used to predict and design an amplifier for an electrically small monopole antenna over the extremely wide 10 kHz to 500 MHz range.

Because the noise figure and available power gain of an amplifier are a function of source impedance, it is necessary to develop an equivalent circuit for antennas used in laboratory bench measurements. The antenna in this case was a vertical monopole that was electrically small and could be represented by a voltage generator, a resistance, and a capacitance in series [Fig. 1(A)]. The measured antenna capacitance of the particular structure used was 6 pF. The resistance is difficult to simulate over a wide bandwidth because it is a function of frequency; therefore, a value of 25 Ω was chosen. This permitted the use of a 50 Ω signal generator to simulate signals received on the antenna for sensitivity and available power gain measurements. The actual dummy antenna circuit is shown in Fig 1(B).

II. Circuit Description

The designed and analyzed amplifier circuit is shown in Fig. 2. It consists of a common source junction field effect transistor (JFET) as the first stage followed by a wideband bipolar (AVANTEK GPD-462) amplifier. Comparison of the noise performance of various active devices indicates that, for a predominately capacitive source, a common source JFET provides the best combination of noise figure and available power gain compared to other FET and bipolar transistor amplifier configurations. Later it is shown that the first stage has an available power gain of less than one; therefore the second stage must be as low noise as possible and must provide appreciable available power gain. Further analysis indicates that additional common source stages would satisfy the requirements; however, this would be at the expense of bandwidth. An approach that preserves the bandwidth is to use a commercial GPD-462 wideband bipolar amplifier, which provides the available power gain. As is shown here, a large value for the gate return resistance (≈ 140 MΩ) is required to reduce the noise figure at very low frequencies (VLFs).

III. Theory and Measurements

The noise figure of a noisy two-port is [3]

$$f = 1 + [\langle e_n^2\rangle + |Z_a|^2 \langle i_n^2\rangle + 2\,\mathrm{Re}(\langle e_n i_n^*\rangle Z_a)] / \langle e_a^2\rangle \tag{1}$$

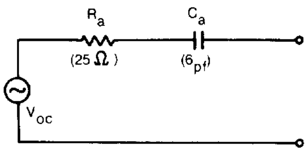
where e_n, i_n are equivalent noise sources at the input to the two-port, $Z_a = R_a - jX_a$ is the antenna impedance, and e_a is the thermal noise voltage of the source resistance.

The noise model of an FET in a common source configuration is shown in Fig. 3 [4,5]. The expressions given in Fig. 3 are derived from noise sources and circuit models presented in [4,5]. The expressions also include the noise generated in the gate return resistance (G_B) and the load resistance (G_L). The noise figure of the first stage can be found using the expressions in (1). After much manipulation and assuming that $G_B^2 \ll (\omega C_{in})^2$, $g_m^2 \gg (\omega C_{gd})^2$, and $g_m C_{in} \gg G_B C_{gd}$, which is the usual case, (1) becomes

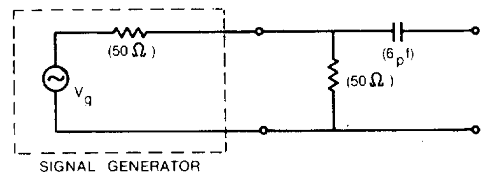
$$f_1 = 1 + (1/g_m R_a)[\alpha_d + (R_a^2 + X_a^2)(\omega C_{in})(\alpha_i - 2\alpha_c + \alpha_d) + (g_m/(\omega C)^2)(G_B + qI_g/2kt) + (2C_{in}/C)(\alpha_d - \alpha_c)] \tag{2a}$$

where

g_m transconductance
α_i dimensionless factor (≈ 0.12 at pinchoff) [4]
α_d dimensionless factor (≈ 0.67 at pinchoff) [4]
α_c dimensionless factor (≈ 0.11 at pinchoff) [4]
k Boltzmann's constant (1.38×10^{-23} J/K)
q electronic charge (1.6×10^{-19} C)
t temperature (288 K)
I_g gate leakage current
C_{gd} gate to drain capacitance
C_{gs} gate to source capacitance
C_{in} $C_{gd} + C_{gs}$ is the input capacitance
G_B $1/R_B$
R_B gate return resistance (140 MΩ)
R_a dummy antenna resistance (25 Ω)



(A) Antenna equivalent circuit.



(B) Antenna dummy circuit.

Fig. 1.

X_a $1/\omega C$ is the dummy antenna capacitive reactance
C $C_a/(1 - \omega^2 LC_a)$ is the effective dummy antenna capacitance
C_a dummy antenna capacitance (6 pF)
L 0.0116 μH is the capacitor lead inductance (calculated from the measured capacitance of the dummy antenna).

At frequencies below 100 MHz, approximations $X_a \gg R_a$ and $C \approx C_a$ can be made. The FET noise figure expression (2a) now becomes

$$f_1 = 1 + (1/R_a g_m)[\alpha_d + (C_{in}/C_a)^2(\alpha_i - 2\alpha_c + \alpha_d) + (2C_{in}/C_a)(\alpha_d - \alpha_c) + (g_m/(\omega C_a)^2)(G_B + qI_g/2kt)]. \tag{2b}$$

The U311 (first stage) JFET parameters are [6]

C_{gd} = 2.5 pF
C_{gs} = 5 pF
g_m = 15 mmho
I_g = 150 pA.

Substituting the above into (2b) results in

$$f_1 = 8.896 + 0.286/f^2_{MHz}. \tag{3}$$

Note that at VLFs the second term is dominant and from (2b) may be written as

$$f_{1\,VLF} = (1/R_a(\omega C_a)^2)(G_B + qI_g/2kt). \tag{4}$$

The importance of having a high value gate return resistance is clearly evident. The shot noise term caused by the gate leakage current (I_g) is important in JFETs and, in this case, the noise figure is 1.5 dB higher than when the term is neglected. The simplicity

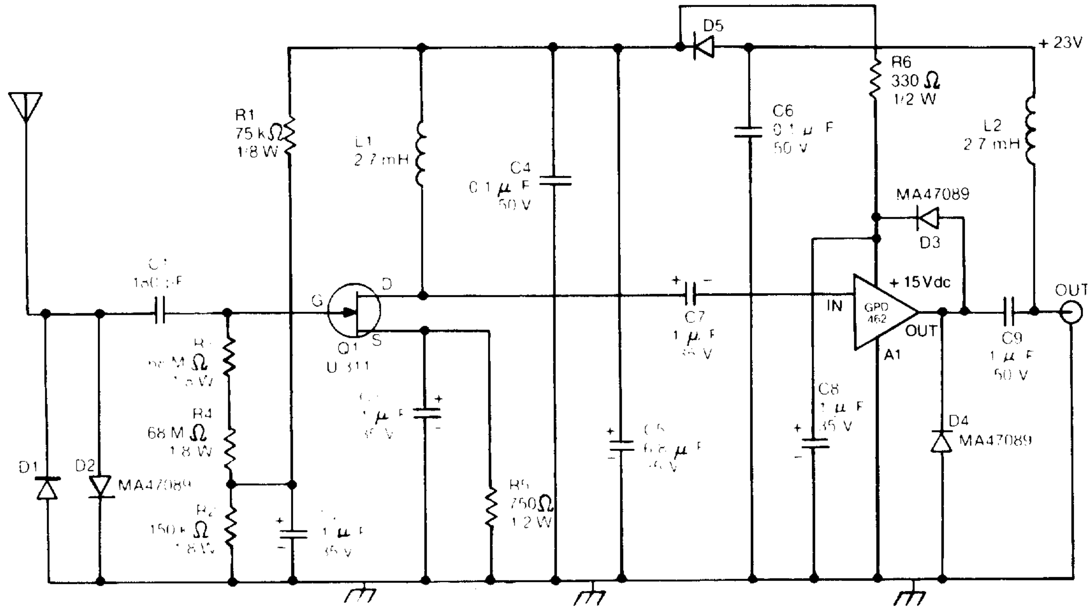
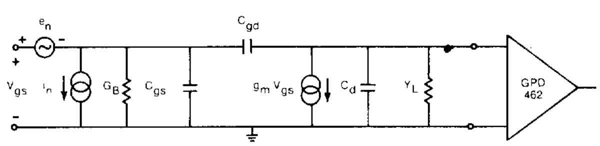


Fig. 2. Antenna amplifier circuit schematic.

Fig. 3. JFET noise model: Common source configuration.



$$\langle e_n^2 \rangle = \frac{4kT\Delta f \alpha_d}{g_m}\left[1 + \frac{G_L}{g_m \alpha_d}\right]$$

$$\langle i_n^2 \rangle = \frac{4kT\Delta f \alpha_d}{g_m}(\omega C_{in})^2 \left\{1 + \frac{\alpha_L}{\alpha_d} - 2\frac{\alpha_i}{\alpha_d} + \frac{G_L}{g_m \alpha_d} + \frac{G_B g_m}{\alpha_d(\omega C_{in})^2}\right\} + q\Delta f I_g$$

$$\langle e_n i_n^* \rangle = -j\frac{4kT\Delta f \alpha_d}{g_m}(\omega C_{in})\left[1 - \frac{\alpha_c}{\alpha_d} + \frac{G_L}{g_m \alpha_d}\right]$$

Y_L = ADMITTANCE OF 2.7 mH COIL

$= G_L + jB_L$

of (2b) allows for a quick but reasonably accurate determination of first stage noise figure. It also provides a means for determining the effect of any parameter change.

To determine the overall noise figure of the antenna amplifier circuit, the formula for amplifiers in cascade is used, i.e.,

$$f = f_1 + (f_2 - 1)/g_1 \tag{5}$$

where f_1 is the noise figure of the first stage (U311), f_2 is the noise figure of the second stage (GPD-462), and g_1 is the maximum available power gain of the first stage.

The maximum available power gain is given by [7]

$$g_1 = (\mathrm{Re}(Y_a)/\mathrm{Re}(Y_o))\,|Y_{21}/(Y_{11} + Y_a)|^2 \tag{6}$$

where $Y_a = 1/Z_a$, Y_o is the first stage output admittance [Re $(Y_o) \approx$ Re$(Y_L) + (g_m C_{gd}/(C_{gd} + C_{gs} + C)$)], and Y_{11}, Y_{21} are the first stage short circuit admittance parameters ($Y_{11} \approx j\omega\,(C_{gs} + C_{gd})$ and $Y_{21} \approx g_m$).

Before g_1 can be calculated, it is necessary to determine the load admittance (Y_L) on the JFET stage because it appears in Y_o. The 2.7 mH load inductance has a measured direct current resistance of 25 Ω and is resonant at 2 MHz. Therefore, it can be shown that the calculated value of Re Y_L is negligible compared with the other terms in Re Y_o. Also, after much manipulation,

$$g_1 = G_a[g_m^2 + (\omega C_{gd})^2]/\{\omega C_{gd}\,[\omega C_{gd}\,G_a + g_m \cdot (\omega C_{in} + B_a)]\} \tag{7a}$$

where

$$G_a = R_a/(R_a^2 + X_a^2)$$

$$B_a = X_a/(R_a^2 + X_a^2).$$

Below 100 MHz, the gain becomes

$$g_1 = g_m R_a C_a^2/[C_{gd}(C_{in} + C_a)] = 0.4\,(-4\text{ dB}). \tag{7b}$$

It is interesting to note that g_1 is now independent of frequency. Again the simplicity of (7b) results in a rapid determination of g_1 and of various parameter tradeoffs.

The noise figure of the GPD-462 amplifier is listed as 6 dB for a 50 Ω source impedance. It is necessary to determine the new noise figure when the source impedance is the output impedance of the JFET. This may be done quite easily if it is assumed that the output noise power available from the GPD-462 is constant, i.e., that it is independent of the "slight" change in source impedance. It can be shown that the change in noise figure is the change in mismatch loss (ML). The calculated output impedance of the JFET is a function of frequency and has a constant standing wave ratio (SWR) of about 12:1 based upon the published input impedance of 30 Ω for the GPD-462; therefore, ML = 5.4 dB. The ML from a 50 Ω source into the amplifier is 0.3 dB. This results in a noise figure, using a JFET impedance source, of 11.1 dB (f_2 = 12.9). Then the overall noise figure becomes

$$f = 8.9 + 0.286/f^2_{\mathrm{MHz}} + 29.7 \tag{8a}$$

$$= 38.6 + 0.286/f^2_{\mathrm{MHz}} \tag{8b}$$

where in (8a) the terms $8.9 + 0.286/f^2_{MHz}$ represent the first stage, and the term 29.7 represents the second stage.

It is difficult to measure the noise figure directly when the source impedance is not 50 Ω. For this reason, sensitivity measurements were made and converted to the noise figure. A comparison between the calculated noise figure and that developed from the sensitivity measurements using the dummy antenna shows reasonable agreement (Fig. 4). The procedure used here is shown to be valid by better than 3 dB agreement over most of the broad frequency range. A comparison of the first and second stage contributions above 1 MHz (8a) to the overall noise figure indicates that the second stage is the main contributor; this is caused by the poor power gain of the first stage. Because the JFET parameters are as good as can be obtained for wideband applications, the most practical way to increase available power gain is by making the antenna longer. This would increase the antenna capacitance and resistance. However, increased antenna size is not always possible for many applications.

If the output impedance of the first stage of the amplifier could somehow be converted to 50 Ω, then f_2 = 4 (i.e., 6 dB) and the overall noise figure below 100 MHz would become

$$f = 16.4 + 0.286/f^2_{\mathrm{MHz}}. \tag{9}$$

The improvement in noise figure is shown in Fig. 4 as the "matched" case for the amplifier circuit. At VLF, the improvement is slight or nonexistent because the bias resistance term is the predominant noise source. At HF and above, the improvement would be a maximum of 4 dB.

By way of comparison, the noise figure which would result from using only the GPD-462 is shown in Fig. 4. As expected, except at the high end of the frequency range where the antenna impedance is low, the GPD-462 has a much higher noise figure.

The available power gain of the antenna amplifier circuit is the product of the available power gains of the first [see (7)] and second stages. The GPD-462 insertion gain is 13 dB in a 50 Ω system and its published output impedance is 80 Ω. The available power gain may be calculated using the insertion gain by incorporating the three MLs. It can be shown that second stage gain g_2 is

$$g_2 = g_I(\mathrm{ML}) \tag{10}$$

where g_I = insertion gain and ML = $\mathrm{ML}_{80/50}$ $(\mathrm{ML}_{50/30})/\mathrm{ML}_{360/30}$.

The notation $\mathrm{ML}_{80/50}$, and so on, denotes the mismatch loss between an 80 Ω and 50 Ω impedance, etc. Below 100 MHz the output impedance of the JFET stage is approximately real and the calculated value is 360 Ω . The result of (10) is a calculated 8 dB available power gain for the second stage. Therefore, below 100 MHz the calculated antenna amplifier circuit gain becomes 4 dB. The available power gain of the entire circuit was developed from insertion gain measurements and is shown in Fig. 5 along with the calculated value. Again the agreement is within 3 dB over most of the frequency range which is satisfactory considering the ease of evaluating (7) and (10). The low frequency rolloff of the measured data below 100 kHz is caused by the fact that the Re (Y_L) is no longer negligible. Also shown is the available power gain when just the GPD-462 is used.

The available power gain of the entire circuit should be high enough to ensure that the antenna amplifier is setting the overall noise figure. In the example provided, this could be ensured by using an additional GPD-462 amplifier, or comparable 50 Ω low noise amplifier (depending upon the length of transmission line to the receiver).

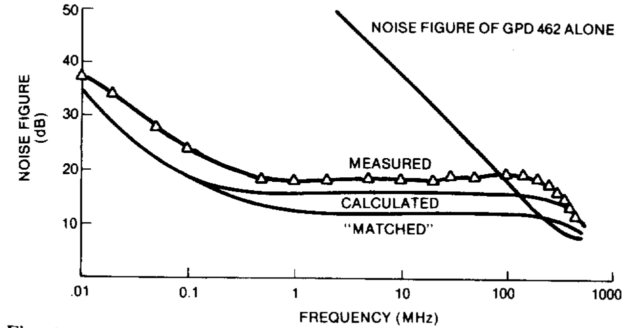
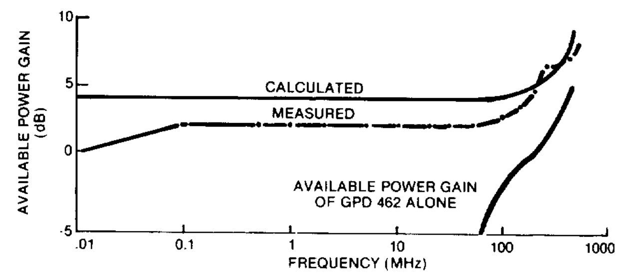


Fig. 4. Comparison of calculated and measured noise figures.

Fig. 5. Calculated and measured available power gain for antenna amplifier circuit.



IV. Conclusion

It has been shown that by using the manufacturer's transistor parameters it is possible to predict wideband antenna circuit performance with relatively simple calculations and without extensive measurements. Calculations of the noise figure and available power gain for a circuit designed to cover a 10 kHz to 500 MHz range agree with measured values to within 3 dB over most of the frequency range. The criterion for performance is, of course, the field strength sensitivity measured with the actual antenna installed in an operational situation. Below 30 MHz, it is desirable that the antenna and preamplifier be atmospherically noise limited. This determination could be made by a knowledge of the actual antenna impedance and comparing the antenna amplifier noise figure with the atmosphere noise figure [8].

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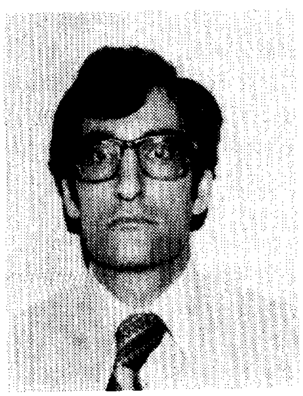

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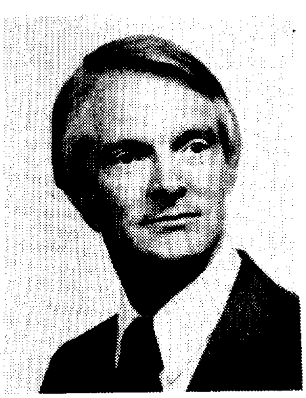

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