Multicore Resource Management for Embedded Real-Time Systems

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High-Performance **Multicores** for Embedded **Real-Time** Systems

• **Why?**
  – Intelligence $\rightarrow$ more performance
  – Space, weight, power (SWaP), cost
Time Predictability Challenge

• Hardware resources are shared among the cores
• Tasks can suffer significant **interference delays**
  – unpredictable, non-deterministic ➔ non-certifiable, unsafe
Example: Real-Time Obstacle Detection and Avoidance

- Co-runners were launched on idle CPU cores
- 5X slowdown in detection speed (~10fps → 2fps)
  - can fail to avoid obstacle
    - e.g., 10m/s aircraft (MAV) can move 1m in 100ms
Research Mission

• Our research goal is to build **predictable**, **efficient**, and **safe** computing infrastructure for the next generation of intelligent embedded real-time systems, a.k.a., Cyber Physical Systems (CPS).

• Approach
  – Develop software/hardware mechanisms
  – Develop analysis framework
Research Results

**Certifiable Multicore Architecture**

- **Core1**
- **Core2**
- **Core3**
- **Core4**

**Shared DRAM**

**High Performance Real-Time Memory Controller**

**Operating System**

- **B/W Regulator**
- **B/W Regulator**
- **B/W Regulator**
- **B/W Regulator**

**System Library**

**Memory Controller**

**BWLOCK**
*In submission*

**MemGuard**
*TC’15, RTAS’13, ECRTS’12*

**PALLOC**
*RTAS’14*

**Shared cache, MSHR**
*OSPERT’15, RTAS’16*

**UAV simplex**
*In preparation*

**BWLOCK**
*In submission*

**Medusa**
*CPSNA’15*

**Memory delay analysis**
*ECRTS’15, RTAS’16*

**In submission**

**In preparation**
PALLOC

- DRAM bank-aware kernel memory allocator
- Can void bank conflict

**SMP OS**

- Core1
- Core2
- Core3
- Core4

**CPC**

Memory Controller (MC)

- Bank 1
- Bank 2
- Bank 3
- Bank 4

**Improved Isolation**

OS Controlled MSHR Partitioning

- Experimentally showed cache partitioning doesn’t provide cache performance isolation in non-blocking caches
- Proposed a OS/hardware collaborative solution that guarantees cache perf. isolation

[RTAS16] Prathap Kumar Valsan (*), Heechul Yun, Farzad Farshchi (*). Taming Non-blocking Caches to Improve Isolation in Multicore Real-Time Systems. In IEEE Intl. Conference on Real-Time and Embedded Technology and Applications Symposium (RTAS), 2016 (Best paper award. *: KU students)
References

- [RTAS16-1] Prathap Kumar Valsan (*), Heechul Yun, Farzad Farshchi (*). Taming Non-blocking Caches to Improve Isolation in Multicore Real-Time Systems. In IEEE Intl. Conference on Real-Time and Embedded Technology and Applications Symposium (RTAS), 2016 (Best paper award. *: KU students)
On-going Projects

• Multicore Resource Management
  – OS, architecture research for time predictability
  – Funding Agencies: NSF, ETRI

• UAV Software Platform
  – ROS (Robot Operating System) based autopilot and real-time sensor (radar and vision) processing
  – Funding Agencies: NASA
Autonomous Racing

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http://www.f1tenth.org/
Prospective Students

• Solid background in operating systems and computer architecture
• Good system programming skills
• **Interests and experiences in building Intelligent cyber-physical systems**
  – ROS, python, Linux, OpenCV, CUDA
  – PID control, real-time sensor fusion

• Send me your CV and schedule a meeting