EECS 312 Exam II (Spring 2018)

Name _____SOLUTION_____

KUID#_____

Instructions:

Please put your last name at the top of each page of the exam in addition to your full name and KUID in the cover page.

The exam is close-book, close-notes. One page of equation sheet is allowed.

For answers in numerical or equation forms, please draw a box around your answer.

Calculators may be used.

Complete all calculations called for and express answers with appropriate precision and in proper engineering notation, e.g. 1mA not 0.001A.

No credit will be given for unsupported answers when reason is asked for.

Additional blank sheets will be provided if needed.

1. _____ (15 pts)

2. _____ (30 pts)

3. _____ (15 pts)

4. _____ (30 pts)

5. _____ (10 pts)

1. (15 pts) Circle the best answer for each question below:

(1) For an ideal MOSFET operating in saturation, the drain-to-source current I_D is independent of the drain-to-source voltage V_{DS}. This is primarily caused by

(a) channel length modulation
(b) channel width modulation
(c) channel pinch-off
(d) zero gate voltage

(2) In a MOSFET, the ***body-effect*** has to be taken into account only when

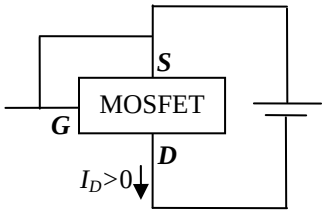
(a) the body is made of *n*-type semiconductor
(b) the body is made of *p*-type semiconductor
(c) the body is connected to the source
(d) the body is not connected to the source

(3) For a MOSFET operating in saturation with a certain V_{GS}, the drain current I_D is ***lower*** for the device with a

(a) longer channel length
(b) wider channel width
(c) larger gate capacitance
(d) higher carrier mobility

(4) For a MOSFET in a circuit with its gate *G* connected to its source *S*, and there is a positive current flowing from the source to the drain through the MOSFET. This MOSFET must be

(a) an enhancement type NMOS
(b) an enhancement type PMOS
(c) a depletion type NMOS
(d) a depletion type PMOS

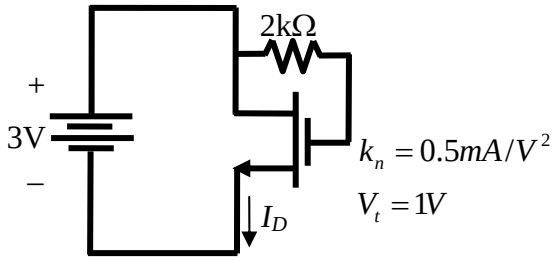


(5) A MOSFET can be used as a voltage-controlled resistor, in which the resistance between the drain and the source is linearly proportional to the voltage between the gate and the source, that is $V_{DS} / I_D \approx k(V_{DS} - V_t)$. To have this voltage/current relation, the MOSFET has to operate in

(a) cutoff mode
(b) triode mode
(c) saturation mode
(d) any one of the above

2, (30 pts.) For each of the following circuits, find the operation mode of MOSFET, and parameter shown in the table (I_D or V_{DS}). Fill results into the table near the circuit.
(***Please show your work, and verify that your assumption of option mode is correct***)

(1)

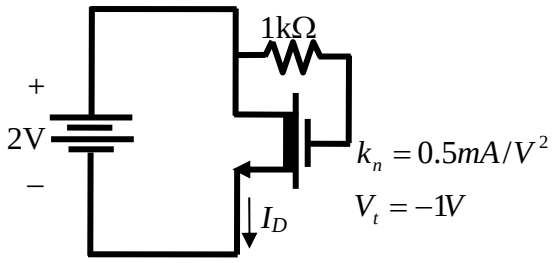


FET operation mode	I_D(mA)
Saturation	1

Solution: $V_{DS} = V_{GS}$, so that $V_{DS} > V_{GS} - V_t$, NMOS operates in saturation

$$I_D = \frac{k_n}{2}(V_{GS} - V_t)^2 = 0.25(3-1)^2 = 1mA$$

(2)

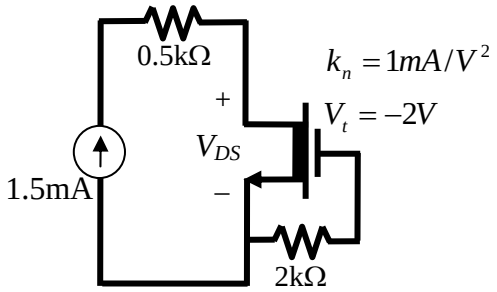


FET operation mode	I_D(mA)
triode	2

Solution: $V_{DS} = V_{GS} = 2V$, but $V_t < 0$, so that $V_{DS} < V_{GS} - V_t$, the depletion-NMOS must operate in triode mode:

$$I_D = k_n\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right] = 0.5\left[2(2+1) - \frac{4}{2}\right] = 2mA$$

(3)



FET operation mode	V_{DS}(V)
Triode	1

Solution: $V_{GS} = 0$, $V_{GS} - V_t = 2V$, assume triode, $I_D = k_n\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right] = 1.5mA$

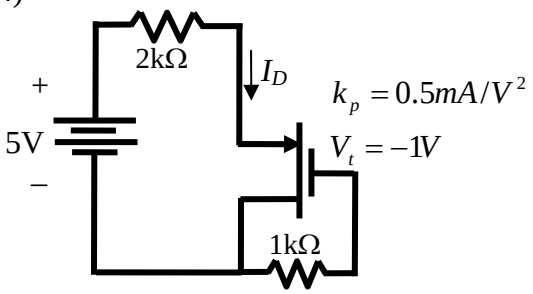
$1.5 = 1\times\left[2V_{DS} - \frac{1}{2}V_{DS}^2\right]$, $V_{DS}^2 - 4V_{DS} + 3 = 0$, thus, $V_{DS} = 1V$ or $V_{DS} = 3V$

Choose $V_{DS} = 1V$ so that $V_{DS} < V_{GS} - V_t = 2V$ for triode

If assume saturation, we must have $I_D = 0.5k_n(V_{GS} - V_t)^2 = 1.5mA$, since

$0.5(0-2)^2 = 2mA$, it cannot be in saturation

(4)



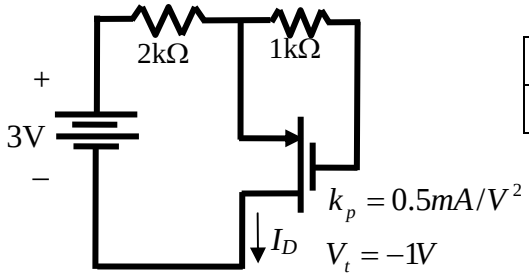
FET operation mode	I_D(mA)
Saturation	1

Solution: since $V_{SD} = V_{SG}$, $V_{SD} > V_{SG} - |V_t|$, PMOS is in saturation,

$I_D = \frac{k_p}{2}(V_{SG} - |V_t|)^2 = 0.25(5 - 2I_D - 1)^2 = (2 - I_D)^2$, solution: $I_D = 1mA$ or $I_D = 4mA$

Choose $I_D = 1mA$, so that $V_{SD} = V_{SG} = 5 - 2I_D = 3V > |V_t|$

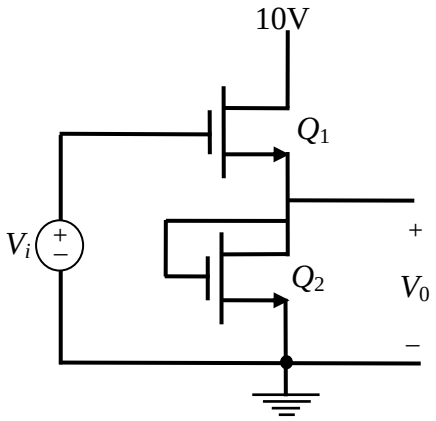
(5)



FET operation mode	I_D(mA)
Cutoff	0

Solution: since $V_{SG} = 0$, $V_{SG} < |V_t|$, PMOS is in cutoff mode, $I_D = 0$

3. (15 pts.) In the following circuit, two identical NMOS are used with k_n = 1mA/V^2 and V_t = 2V.



(1) Assume both Q_1 and Q_2 operate in *saturation*, please write the output voltage V_0 as the function of the input voltage V_i [that is, $V_0 = f(V_i)$].

Solution: $I_{D1} = \frac{k_n}{2}(V_{GS1} - V_t)^2 = \frac{k_n}{2}(V_i - V_0 - V_t)^2$; $I_{D2} = \frac{k_n}{2}(V_0 - V_t)^2$

Since $I_{D1} = I_{D2}$

$\frac{k_n}{2}(V_i - V_0 - V_t)^2 = \frac{k_n}{2}(V_0 - V_t)^2$,

as $(V_i - V_0 - V_t) > 0$ and $(V_0 - V_t) > 0$ we have $V_i - V_0 - V_t = V_0 - V_t$,

that is, $V_0 = V_i / 2$

(2) Find the range of V_i in which both Q_1 and Q_2 operate in saturation.

For Q_2 not to be in cutoff

$V_0 > V_t = 2V$ is requited, that is $V_i / 2 > 2V$, $V_i > 4V$

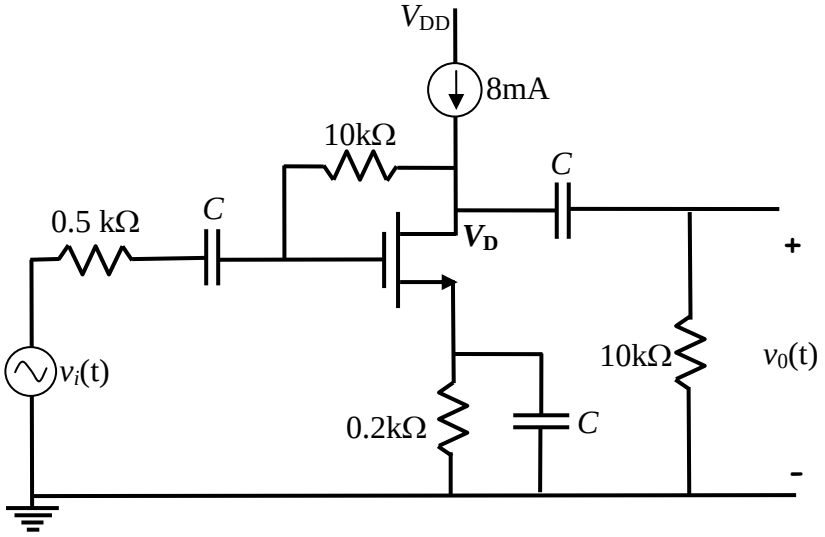
For Q_1 in saturation, it requires $10 - V_0 > V_i - V_0 - V_t$, or, $V_i > 12V$

Therefore, overall $4V < V_i < 12V$

4. (30 pts.) The following circuit uses an NMOS with k_n = 1mA/V^2 and V_t = 2V. All the capacitors have very large capacitances so that they can be treated as short circuits in AC and open circuits in DC. The input v_i(t) is a small AC signal and the small-signal output voltage is v_0(t).

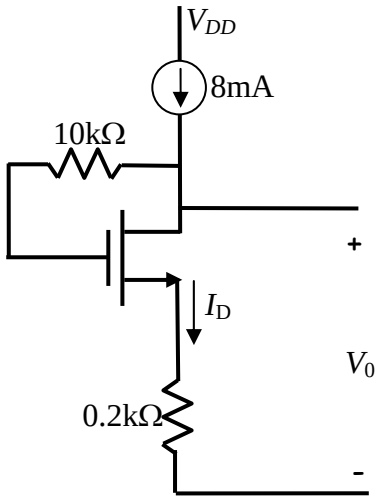
(1) Draw the DC equivalent circuit and find the DC voltage $\boldsymbol{V_D}$ at the drain of the NMOS

(2) Draw the AC equivalent circuit and find the small-signal voltage gain
($A_V = v_0(t)/v_i(t) = ?$)



Solution:

(1) The DC equivalent circuit is:



$I_D = 10mA$, and $V_{DG} = 0$, so that $V_{DS} = V_{GS}$

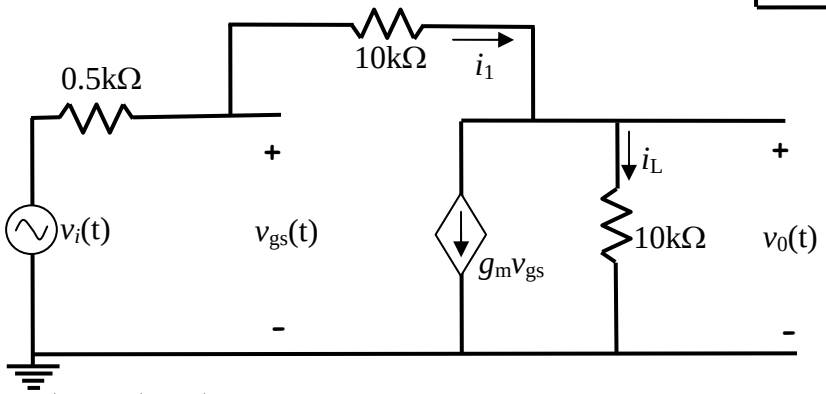
NMOS must be operating in saturation

$$I_D = \frac{k_n}{2}(V_{GS} - V_t)^2 = 0.5(V_{GS} - 2)^2 = 8$$

$$V_{GS} = 6V$$

$$V_0 = V_{GS} + 8 \times 0.2 = 6 + 1.6 = 7.6V$$

(2) The AC equivalent circuit is



$$g_m = k_n(V_{GS} - V_t) = 1 \times (6 - 2) = 4mA/V$$

$$i_1 = \frac{v_{gs} - v_0}{10} \qquad (1)$$

$$v_0 = 10(i_1 - g_m v_{gs}) \qquad (2)$$

$$v_i - 0.5i_1 = v_{gs} \qquad (3)$$

Based on these three equations, eliminate i_1 and v_{gs},

Bring (1) into (2) and (3)

$v_0 = 10\left(\frac{v_{gs} - v_0}{10} - g_m v_{gs}\right) = v_{gs} - v_0 - 10 g_m v_{gs}$, that is $2v_0 = (1 - 10g_m)v_{gs}$

or $v_0 = \frac{(1-40)}{2} v_{gs} = -19.5 v_{gs}$

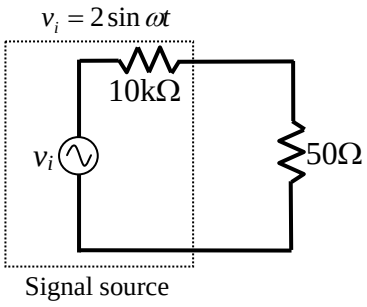
$v_i - 0.5\frac{v_{gs} - v_0}{10} = v_{gs}$, $20v_i - v_{gs} + v_0 = 20v_{gs}$, that is $v_{gs} = \frac{v_0 + 20v_i}{21}$

$v_0 = -19.5\frac{v_0 + 20v_i}{21}$, $\left(\frac{21}{19.5} + 1\right)v_0 = -20v_i$, that is $A_v = \frac{v_0}{v_i} = -\frac{20}{\frac{21}{19.5} + 1} = -9.6$

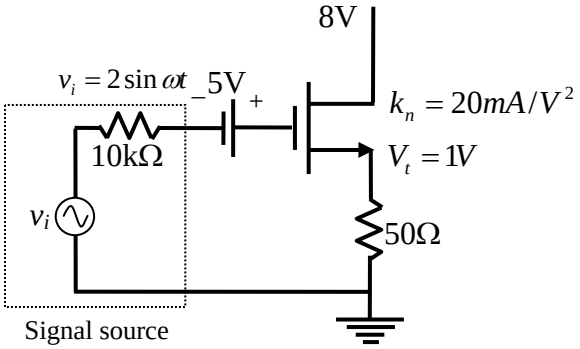
5. (10 pts.) Consider a sine-wave voltage source $v_i = V_p \sin \omega t$ with V_p = 1V, and the source has a 10kΩ output resistance as shown in the following figure.

(1) In circuit (a) of the following figure, this signal source is driving a 50Ω load (which can be a speaker). What is the average AC signal power that is delivered to the load resistor? [Note: for an AC current $i = I_p \sin \omega t$ flowing through a load resistor *R*, the average power delivered to the load is $P = I_p^2 R / 2$]

(2) In circuit (b) of the following figure, a MOSFET is used and the 50Ω load resistor is connected to the source of the NMOS. The MOSFET operates in ***saturation*** region. What is the average AC signal power that is delivered to the load resistor? So, what is the signal power amplification introduced by this MOSFET (compared to circuit (1))?



(a)



(b)

Solution:

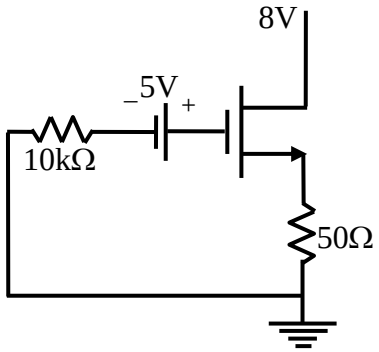
(1) Current flowing through the load resistor is

$$i_L = \frac{v_s}{100050} = \frac{V_p}{10050}\sin\omega t = \frac{1}{10050}\sin\omega t \approx 10^{-4}\sin\omega t[A]$$

Average power is, $P_L = 10^{-8} R_L / 2 = 25\times 10^{-8} W = 0.25\mu W$

(2) For DC analysis,

$$I_D = \frac{k_n}{2}(V_G - V_S - V_t)^2 \text{ and } V_S = 0.05 I_D \text{ or } I_D = 20 V_S$$



$20V_S = 10(4 - V_S)^2$, $2V_S = 16 - 8V_S + V_S^2$,

$V_S^2 - 10V_S + 16 = 0$

$V_S = \frac{10 \pm \sqrt{100-64}}{2} = \frac{10 \pm 6}{2}$. Solutions are $V_S = 8V$ and $V_S = 2V$

Choose $V_S = 2V$, so that $V_{GS} = 5 - 2 = 3V$

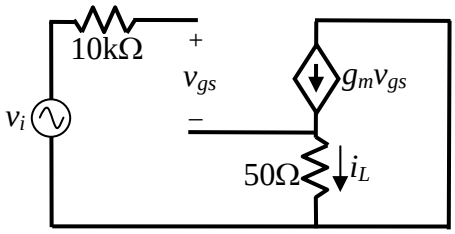
$g_m = k_n(V_{GS} - V_t) = 20(3-1) = 40mA/V = 0.04A/V$

For AC analysis:

$v_i = v_{gs} + 50 g_m v_{gs}$, $i_L = g_m v_{gs}$

$v_i = \frac{i_L}{g_m} + 50 i_L$, so that

$$i_L = \frac{v_i}{\frac{1}{g_m} + 50} = \frac{v_i}{\frac{1}{0.04} + 50} = \frac{1}{75}\sin\omega t[A]$$



Average power to the load is,

$$P_L = \frac{1}{75^2}\frac{R_L}{2} = \frac{1}{75^2}\frac{50}{2} = 0.004W = 4mW$$

Thus, the power gain of this amplifier is $\frac{0.004}{25\times 10^{-8}} = 16000$