EECS 312 Exam III (Spring 2017)

Name _____SOLUTION_____

KUID#_____

Instructions:

Please put your last name at the top of each page of the exam in addition to your full name and KUID in the cover page.

The exam is close-book, close-notes. Two pages of equation sheets may be used.

For answers in numerical or equation forms, please draw a box around your answer.

Calculators may be used.

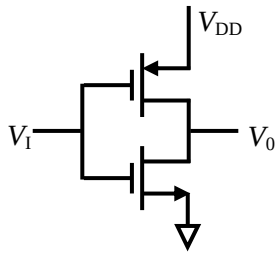
Complete all calculations called for and express answers with appropriate precision and in proper engineering notation, e.g. 1mA not 0.001A.

No credit will be given for unsupported answers when reason is asked for.

Additional blank sheets will be provided if needed.

1. (15 pts) Circle the best answer for each question below:

(1) For a CMOS inverter without output load, if the input voltage is either $V_I = 0$ or $V_I = V_{DD}$, the ***static*** power dissipation of the CMOS is

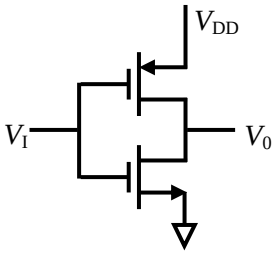


(a) V_{DD}^2
(b) $V_{DD}^2 / 2$
(c) $V_{DD}^2 / 4$
(d) 0

(2) A desired property of a high quality CMOS inverter is to have

(a) Large noise margin
(b) Small noise margin
(c) Zero noise margin
(d) Uncertain noise margin

(3) For a CMOS inverter (no load) made by two MOSFETs with matched parameters ($k_n = k_p$, $V_{tn} = |V_{tp}|$), the highest **static** power dissipation happens at

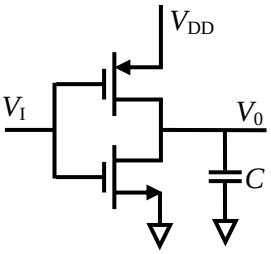


(a) $V_I = 0$
(b) $V_I = V_t$
(c) $V_I = V_{DD} / 2$
(d) $V_I = V_{DD}$

(4) In MOSFET-based digital logic circuits, "pseudo-NMOS" is

(a) a *NMOS* transistor
(b) often used to replace the entire pull-up network (PUN)
(c) often used to reduce the static power dissipation
(d) all of the above

(5) If f represents switching repetition frequency, V_{DD} is the bias voltage, and C is the load resistance, average ***dynamic power dissipation*** of the CMOS inverter is

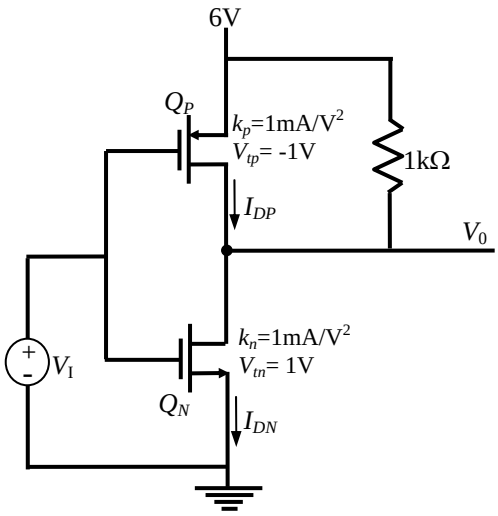


(a) $fCV_{DD}^2 / 2$
(b) $2\,fCV_{DD}^2$
(c) fCV_{DD}^2
(d) $fC^2V_{DD}^2$

2. (30 pts.) Consider the following CMOS inverter with a bias voltage V_{DD} = 6V, the parameters of MOSFETS are: for the PMOS (Q_P), $k_p = C_{ox}\mu_p(W/L) = 1mA/V^2$, V_{tp} = -1V, and for the NMOS (Q_N): $k_n = C_{ox}\mu_n(W/L) = 1mA/V^2$, V_{tn} = 1V.

(a) For V_I = 6V, and V_I = 0V, respectively, use *equivalent resistance approximation*, please find:
Operation modes of Q_N, and Q_P
Drain currents I_{DP}, and I_{DN}
Output voltage V_0

(b) For V_I = 3V (equivalent resistance approximation is no longer valid), please find:
Operation modes of Q_N, and Q_P
Drain currents I_{DP}, and I_{DN}
Output voltage V_0
[*Note*: in this case Q_N and Q_P CANNOT be both in saturation mode)



(***Fill all results into the table on top of the next page***)

Solution:

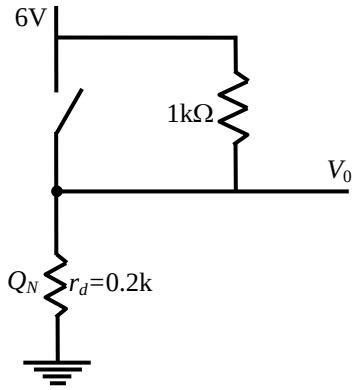
For V_I = 6V, Q_P is cutoff and Q_N is triode.

$$r_d = \frac{1}{k_n(V_{GS} - V_{tn})} = \frac{1}{1\times(6-1)} = 0.2k\Omega$$

Since Q_P is cutoff, I_{DP} = 0.

V_0 can be obtained with a voltage divider

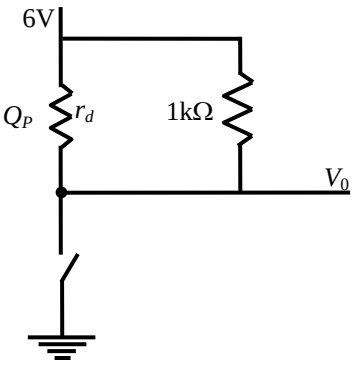
$$V_0 = 6\times\frac{0.2}{1+0.2} = 1V \text{ and } I_{DN} = \frac{1V}{0.2k\Omega} = 5mA$$



For V_I = 0V, Q_N is cutoff and Q_P is triode.

$$r_d = \frac{1}{k_p(V_{SG} - |V_{tp}|)} = \frac{1}{1\times(6-1)} = 0.2k\Omega$$

Since Q_N is cutoff, I_{DN} = 0, I_{DP} = 0, and V_0 = 6V



For V_I = 3V, equivalent resistance approximation cannot be used. Assume Q_N is saturation and Q_P is triode.

$$I_{DN} = \frac{1}{2}k_n(V_{GS} - V_{tn})^2 = 0.5\times(3-1)^2 = 2mA$$

$$I_{DP} = k_p\left[(V_{SG} - |V_{tp}|)(6-V_0) - \frac{1}{2}(6-V_0)^2\right]$$

$$I_{DP} + I_L = 2mA, \text{ or, } I_{DP} + \frac{6-V_0}{1} = 2mA$$

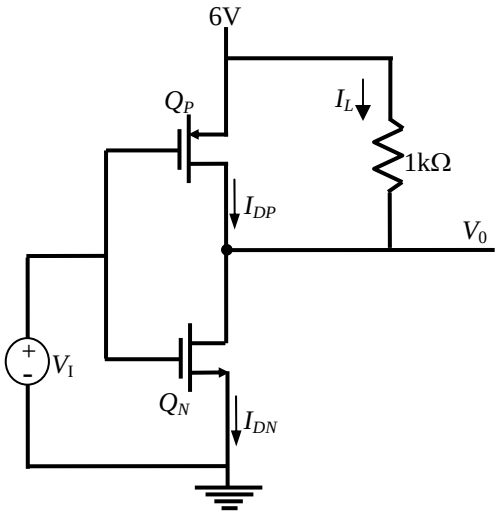
That is,

$$k_p\left[(V_{SG} - |V_{tp}|)(6-V_0) - \frac{1}{2}(6-V_0)^2\right] = V_0 - 4$$

$$1\times\left[(3-1)(6-V_0) - \frac{1}{2}(6-V_0)^2\right] = V_0 - 4$$

$$\left[4(6-V_0) - (6-V_0)^2\right] = 2V_0 - 8$$

$V_0^2 - 6V_0 + 4 = 0$, solutions are $V_0 = 5.23V$ and $V_0 = 0.764V$.

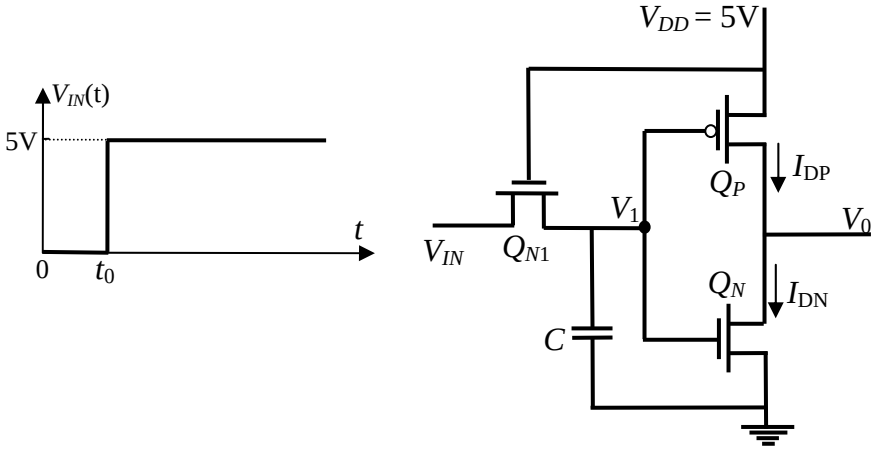


Choose $V_0 = 5.23V$ as Q_N is saturation was assumed.

Then $I_{DP} + \frac{6-V_0}{1} = 2 + 5.23 - 6 = 1.23mA$, and $I_L = 6 - 5.23 = 0.77$

Input voltage V_I	Operation mode of Q_N	Operation mode of Q_P	I_{DP}	I_{DN}	Output voltage V_0
6V	Triode	cutoff	0	5mA	1V
0V	cutoff	triode	0	0	6V
3V	Saturation	triode	1.23mA	2mA	5.23V

3, (20 pts) The following circuit uses an NMOS transmission gate to drive a CMOS inverter.



(1) Assume the NMOS transmission gate, Q_{N1}, has $k_n = 1mA/V^2$ and V_t=1V, and the body effect can be neglected for simplicity (that is γ = 0). At time t = t_0, the input voltage V_{IN} is switched from 0 to 5V. Please find:

(a) For $t \geq t_0$, what is the maximum current that flows through Q_{N1}?

(b) At $t = \infty$, what is the voltage value of V_1 ?

(2) If V_1 = 3.5V at the CMOS input (output of the transmission gate), and CMOS parameters are $k_p = k_n = 1mA/V^2$ and $V_{tn} = |V_{tp}| = 0.5V$, please find V_0 = ?

Solution: (1)

(a) As $V_D = V_G = 5V$ NMOS is in saturation, and the current is constant

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 = \frac{1}{2}k_n(V_{DD} - V_1 - V_t)^2 = 0.5 \times (4 - V_1)^2$$

Thus, $I_{D,\max} = 0.5 \times 16 = 8mA$, which happens at t = t_0 and V_0 = 0.

(b) At $t = \infty$, V_1 reaches to its maximum value which is $V_1 = V_{DD}$ - V_t = 4V
and at this point NMOS is cutoff.

(2) For the CMOS with V_1 =3.5V at the input, Q_p is saturation and Q_n is in triode.

$$I_{DP} = \frac{1}{2}k_p(V_{DD} - V_1 - |V_{tp}|)^2 = 0.5 \times (5 - 3.5 - 0.5)^2 = 0.5mA$$

To calculate the value of V_0,

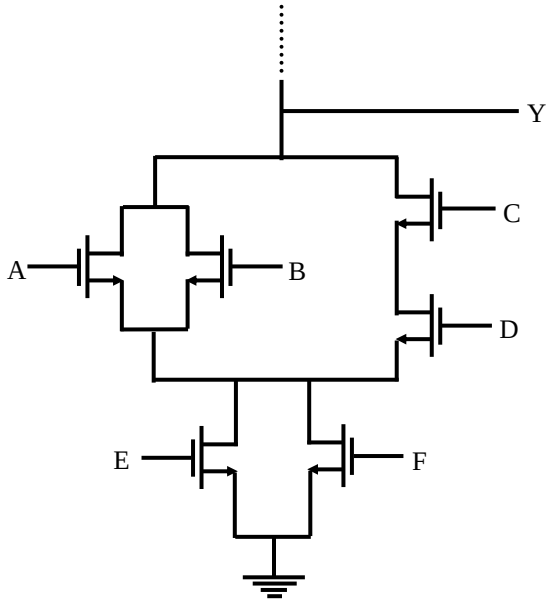
$$I_{DN} = k_n\left[(V_1 - V_{tn})V_0 - \frac{1}{2}V_0^2\right] = k_n\left[(3.5 - 0.5)V_0 - \frac{1}{2}V_0^2\right] = 1 \times \left[3V_0 - \frac{1}{2}V_0^2\right]$$

Since $I_{DP} = I_{DN}$, $\left[3V_0 - \frac{1}{2}V_0^2\right] = 0.5$, $V_0^2 - 6V_0 + 1 = 0$,

The solutions are $V_0 = 3 \pm \sqrt{8}$. Choose $V_0 = 3 - \sqrt{8} = 0.172V$

4. (25 pts)

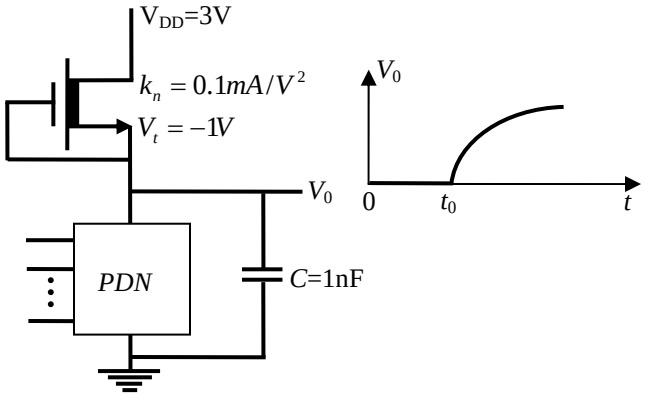
(1) (10 pts) The pull-down network (PDN) of a CMOS logical circuit is shown in the following figure. Please draw the corresponding pull-up network (PUN), and find the logical function of this circuit.



(2) (15 pts) Assume the *PUN* is a "depletion- load" based on a depletion-NMOS shown in the following circuit with parameters: $k_n = 0.1mA/V^2$ and V_t = -1V. The bias voltage is V_{DD} = 3V.

(a) Please find the static power dissipation when the output is at low level V_0 = 0 (for $t < t_0$)

(b) The input is suddenly switched at $t = t_0$ so that PDN suddenly becomes an open circuit and the voltage V_0 starts to increase. If the load capacitor is C = 1nF (which is $10^{-9}F$), how long it takes for V_0 to rise from 0 to 1.5V? [Note: voltage increase across a capacitor is $\Delta V = I_c \Delta t / C$ if the charge current I_c is constant]



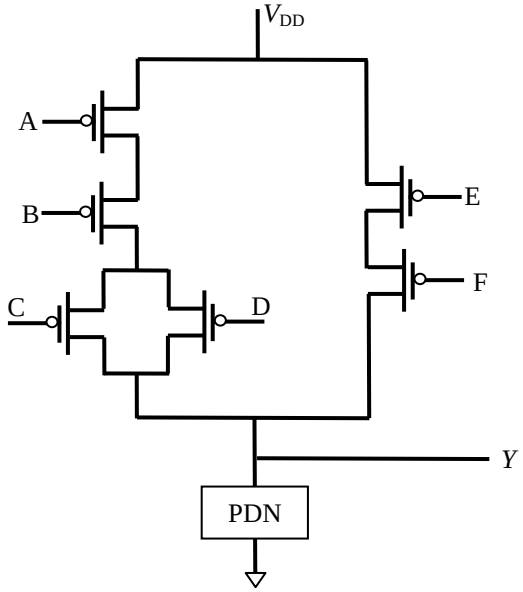
Solution:

(1) The PDN circuit performs the logical function of

$$\overline{Y} = (A + B + CD)(E + F)$$

Then the PUN has to perform

$$Y = f(\overline{A}, \overline{B}, \overline{C}, ...) = \overline{(A + B + CD)(E + F)}$$
$$= \overline{(A + B + CD)} + \overline{(E + F)}$$
$$= \overline{(A + B)}\,\overline{CD} + \overline{E}\,\overline{F} = \overline{A}\,\overline{B}(\overline{C} + \overline{D}) + \overline{E}\,\overline{F}$$



(2) Now the *PUN* is a depletion-load. When the output is at $V_0 = 0$, the depletion-type NMOS operates in saturation mode (because $V_{DS} = V_{DD} = 3V$, $V_{GS} - V_t = 1V > 0$ (not in cutoff), so that $V_{DS} > V_{GS} - V_t$).

(a) $I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 = 0.05 \times (0 + 1)^2 = 0.05mA$

Static power dissipation of this logic gate is $P_D = V_{DD} I_D = 3 \times 0.05 = 0.15mW$

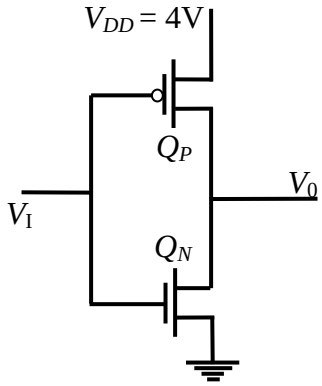
(b) When PDN suddenly switches off, current flowing through the depletion load does not change, which is a constant value: $I_D = 0.05mA$

Voltage change across the load capacitor is $\Delta V_0 = \frac{I_D \Delta t}{C}$ or, $\Delta t = \frac{C \Delta V_0}{I_D}$

For $\Delta V_0 = 1.5V$, $I_D = 0.05mA$ and $C = 10^{-9}F$,

$$\Delta t = \frac{10^{-9} \times 1.5}{0.05 \times 10^{-3}} = 3 \times 10^{-5} s = 30 \mu s$$

5, (10 pts) For a non-ideal CMOS inverter with $V_t = V_{tn} = |V_{tp}| = 1V$ but $k_n = 4k_p$. The bias voltage is V_{DD} = 4V. What is the input voltage V_I which makes the output V_0 = 2V? (Note, at this point, both Q_P and Q_n are in saturation mode)



Solution: Since both Q_P and Q_N are in saturation,

$I_{DP} = I_{DN} = \frac{k_n}{2}(V_I - V_t)^2 = \frac{k_p}{2}(V_{DD} - V_I - V_t)^2$,

because $k_n = 4k_p$, we have $4(V_I - 1)^2 = (3 - V_I)^2$

That is, $2(V_I - 1) = \pm(3 - V_I)$

The only positive solution is, $V_I = 5/3 = 1.667V$

For an ideal CMOS with $k_n = k_p$, $V_I = V_{DD}/2 = 2V$ is required to have $V_0 = 2V$.

Thus, with $k_n = 4k_p$, NM_H will be increased but NM_L will likely be decreased.