14.18 $NM_H = V_{OH} - V_{IH}$

$= 0.8V_{DD} - 0.6V_{DD} = 0.2V_{DD}$

$NM_L = V_{IL} - V_{OL}$

$= 0.4V_{DD} - 0.1V_{DD} = 0.3V_{DD}$

Width of transition region $= V_{IH} - V_{IL}$

$= 0.6V_{DD} - 0.4V_{DD} = 0.2V_{DD}$

For a minimum noise margin of 0.4 V, we have

$NM_H = 0.4$

$\Rightarrow 0.2V_{DD} = 0.4$

$\Rightarrow V_{DD} = 2$ V

14.34 For $v_I = +1.5$ V, Q_N will be conducting and operating in the triode region while Q_P will be off. Thus, the incremental resistance to the left of node A will be r_{DSN},

$$r_{DSN} = \frac{1}{k_n(V_I - V_{tn})}$$

$$= \frac{1}{0.2(1.5 - 0.5)} = 5\text{ k}\Omega$$

Thus,

$$v_a = 100\left(\frac{5}{5 + 100}\right)$$

$= 4.8$ mV

For $v_I = -1.5$ V, Q_N will be off but Q_P will be operating in the triode region with a resistance r_{DSP},

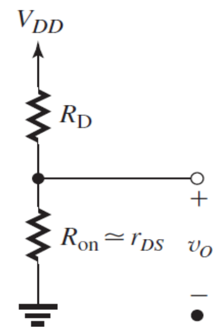
$$r_{DSP} = \frac{1}{k_p(V_{SGP} - |V_{tp}|)}$$

$$= \frac{1}{0.04(1.5 - 0.5)} = 25\text{ k}\Omega$$

Thus,

$$v_a = 100\left(\frac{25}{25 + 100}\right) = 20\text{ mV}$$

14.24



Equivalent circuit for output-low state

The output-high level for the simple inverter circuit shown in Fig. 14.12 of the text is

$V_{OH} = V_{DD} \Rightarrow V_{DD} = 1.2$ V.

When the output is low, the current drawn from the supply can be calculated as

$$I = \frac{V_{DD}}{R_D + R_{on}} = 30\ \mu\text{A}$$

Therefore: $R_D + r_{DS} = \dfrac{1.2}{30 \times 10^{-6}} = 40\text{ k}\Omega$

Also:

$$V_{OL} = 0.05\text{ V} = \frac{r_{DS}}{R_D + r_{DS}} \times V_{DD}$$

$$\Rightarrow r_{DS} = 40\text{ k}\Omega \times \frac{0.05}{1.2} = 1.67\text{ k}\Omega$$

Hence: $R_D = 40\text{ K} - 1.67\text{ K} = 38.3\text{ k}\Omega$

$$r_{DS} = \frac{1}{\mu_n C_{ox}\dfrac{W}{L}(V_{GS} - V_t)}$$

$$= \frac{1}{500 \times 10^{-6} \times \dfrac{W}{L}(1.2 - 0.4)}$$

$= 1.67\text{ k}\Omega$

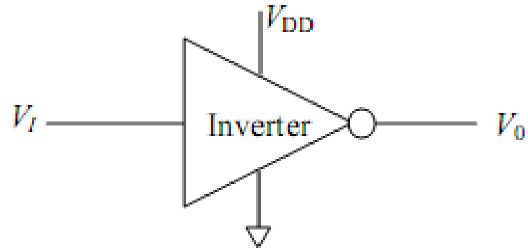
$$\Rightarrow \frac{W}{L} = 1.5$$

When the output is low:

$P_D = V_{DD}I_{DD} = 1.2 \times 30\ \mu\text{A} = 36\ \mu\text{W}$

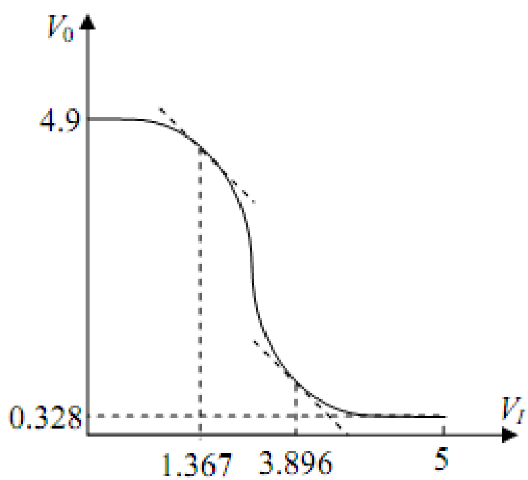
When the output is high, the transistor is off: $P_D = 0$ W

Handout problem 1:
An inverter has the transfer function described by
$V_0 = 2.6 + 2.3\cos(0.19\pi V_I)$



If the DC bias voltage is V_{DD} = 5V, find V_{IH}, V_{IL}, V_{0H}, V_{0L}, NM_L, and NM_H. (Use $dV_0 / dV_I = -1$ to determine the boundary of regions).

Solution:
Based on the transfer function $V_0 = 2.6 + 2.3\cos(0.19\pi V_I)$, for V_I = 0, V_0 = 4.9V, and for V_I = 5V, V_0 = 0.328V.
To find V_{IH} and V_{IL}, we need to find solutions for $dV_0 / dV_I = -1$.
Since $\frac{dV_0}{dV_I} = -2.3 \times 0.19\pi \sin(0.19\pi V_I) = -1.373 \sin(0.19\pi V_I) = -1$, the solutions are,
$V_I = 1.367$ and $V_I = 3.896$



Therefore, $V_{IL} = 1.367$, $V_{IH} = 3.896$, $V_{0L} = 0.328$ and $V_{0H} = 4.9$
$NM_L = V_{IL} - V_{0L} = 1.367 - 0.328 = 1.039V$
$NM_H = V_{0H} - V_{IH} = 4.9 - 3.896 = 1.004V$

Handout problem 2:

A CMOS inverter has $k = 10mA/V^2$, $V_t = 2V$, $V_{DD} = 6V$ and an output capacitance of $C = 2nF$.

(1) Plot the transfer function of $V_0(V_I)$

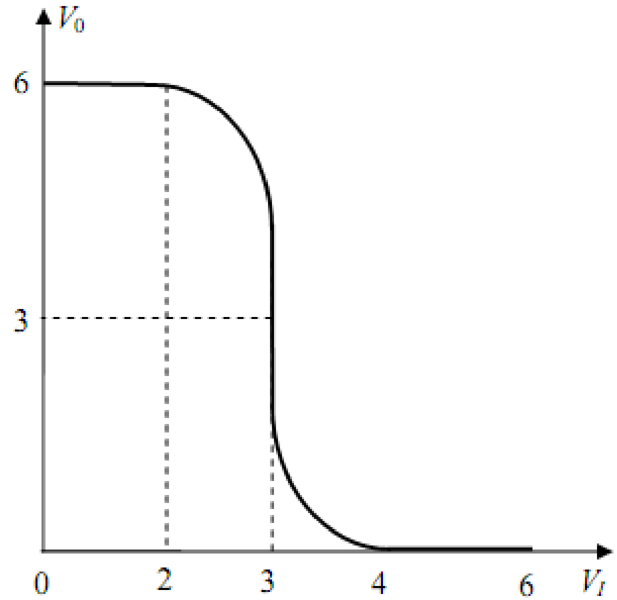
(2) Find t_{PHL}

(3) How do t_{PHL} change if the channel length L of the MOSFET is doubled?

(4) Find the dynamic power dissipation if the CMOS is switched by a signal with 10MHz repetition rate.

Solution:

(1)



(2) Based on equations 14.51 and 14.52:

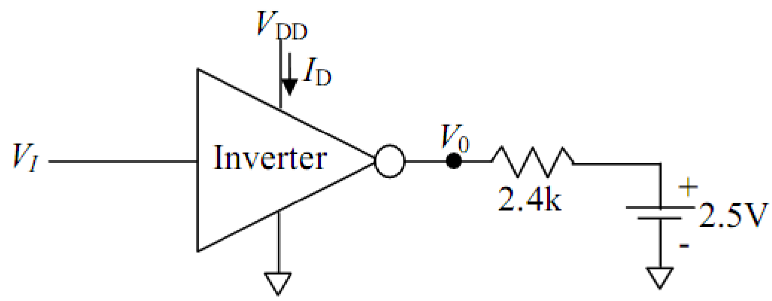
$$t_{PHL} = \frac{2C}{k_n\left[\frac{7}{4} - \frac{3V_t}{V_{DD}} + \left(\frac{V_t}{V_{DD}}\right)^2\right]V_{DD}} = \frac{2\times 2\times 10^{-9}}{10\left[\frac{7}{4} - \frac{3\times 2}{6} + \left(\frac{2}{6}\right)^2\right]\times 6} = \frac{4\times 10^{-9}}{60\left[\frac{7}{4} - 1 + \frac{1}{9}\right]} = 77.5ns$$

(3) Since $t_{PHL} \propto \frac{1}{k_n} = \frac{1}{C_{ox}\mu_n(W/L)} = \frac{L}{C_{ox}\mu_n W}$, if the channel length is doubled, t_{PHL} will be doubled.

(4) Dynamic power dissipation is: $P_D = fCV_{DD}^2 = 10^7 \times 2 \times 10^{-9} \times 6^2 = 0.72W$

Handout problem 3:

In the following CMOS inverter $k = 2.5mA/V^2$, $V_t = 1V$, $V_{DD} = 5V$.



(a) Find V_0 if $V_I = 0$V

(b) Find V_0 if $V_I = 5$V

(c) Find the drain current I_D when $V_I = 2.5$V

Solution:

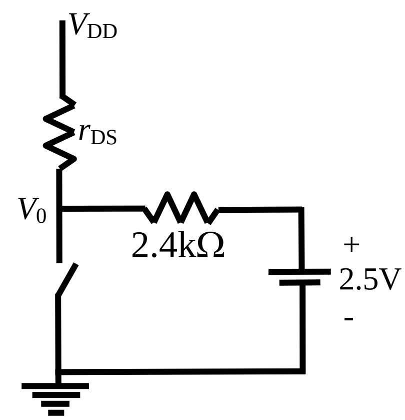
(a) When $V_I = 0$, NMOS (Q_n) is cutoff and PMOS (Q_p) is triode, and the equivalent resistance of Q_p is,

$$r_{DS} = \frac{1}{k_p(V_{DD} - |V_{tp}|)} = \frac{1}{2.5\times(5-1)} = 0.1k\Omega$$

The current flowing through Q_p is,

$$I_D = \frac{V_{DD} - 2.5}{r_{DS} + 2.4} = \frac{5-2.5}{0.1+2.4} = 1mA$$

Then, $V_0 = V_{DD} - I_D r_{DS} = 5 - 1\times 0.1 = 4.9V$



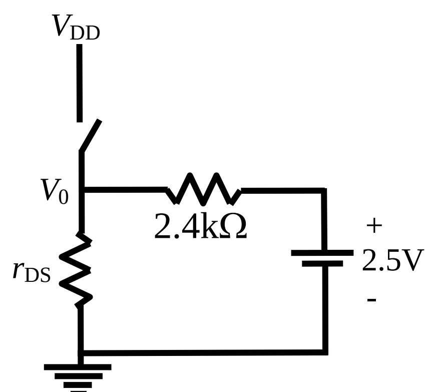
(b) When $V_I = 5$V, PMOS (Q_p) is cutoff and NMOS (Q_n) is triode, and the equivalent resistance of Q_n is,

$$r_{DS} = \frac{1}{k_n(V_{DD} - V_{tn})} = \frac{1}{2.5\times(5-1)} = 0.1k\Omega$$

The current flowing through Q_n is,

$$I_D = \frac{2.5}{r_{DS} + 2.4} = \frac{2.5}{0.1+2.4} = 1mA$$

Then, $V_0 = I_D r_{DS} = 1\times 0.1 = 0.1V$



(c) When $V_I = 2.5$V, the output is $V_0 = 2.5$V due to the symmetry of the circuit. Both of the two MOSFETs are in saturation mode, and

$$I_D = \frac{k}{2}(V_{GS} - V_t)^2 = 1.25\times(2.5-1)^2 = 2.81mA$$