EECS 312 - Electronics Circuits I, Exam III (Spring 2018)

Material:

Chapter 14: 14.1, 14.2, 14.3, 14.4 (14.4.1, 14.4.2), 14.6

Chapter 15: 15.1 (15.1.1, 15.1.2, 15.1.3), 15.3, 15.4

Chapter 16: 16.1

Chapter 14 –CMOS digital logic circuits

What is CMOS? CMOS inverter basic configuration

Why a CMOS inverter is better than an inverter using a single NMOS and a resistor?

CMOS transfer function (5 different regions of the transfer function): operation mode of Q_N and Q_P in each region.

CMOS equivalent circuit model (equivalent resistance model) when the output load is considered

Condition at which equivalent resistance model is valid (usually at $V_I = 0$ or V_{DD})

How to calculate equivalent resistances of NMOS and PMOS in a CMOS configuration?

Definition and derivation of V_{IL}, V_{IH}, V_{OL} and V_{OH}

Definition and significance of noise margin (NM, NM_H, NM_L)

Switch-on and switch-off processes when the load is a resistor, or capacitor.

Propagation delay (load capacitor charge or discharge), static and dynamic power dissipation

Design of CMOS logic-gate circuits
Why CMOS?
Logic AND: MOSFETs in series
Logic OR: MOSFETs in parallel
Pull-up network: $Y = f(\overline{A}, \overline{B}, \overline{C}, ...)$
Pull-down network: $\overline{Y} = f(A, B, C, ...)$
Put pull-up and pull-down networks together to get a complete logic-gate
Requires Boolean algebra

Chapter 15 –Advanced topics in digital integrated circuit design

Moore's Law
Number of CMOS per unit area increases, size of each CMOS decreases, channel length decreases. Consequence: carrier velocity saturation (change of I_D vs. V_{DS} and I_D vs. V_{GS} characteristics), and sub-threshold conduction (current leakage)

***Pseudo-NMOS logical circuits and depletion load*:**
Major purpose of pseudo-NMOS in digital inverters
Pseudo-NMOS is made by a PMOS FET with the gate connected to the ground
Depletion load is a depletion NMOS with Gate connected to the source
They are basically two-terminal devices. They can be used as active loads (to simulate resistors).
Current-voltage relations of these circuits, their applications in digital logic circuits,

Pass-transistor logic circuits:
Use a single MOSFET as a switch (NMOS or PMOS)
Impact of body effect
Use CMOS transmission gate as a switch, what is the major advantage?
Equivalent resistance of CMOS transmission gate

Chapter 16 –Memory Circuits

Latches and flip-flops
CMOS implementation of flip-flops (circuit configurations)
SR flip-flops, and triggering of flip-flops