EECS 140 and 141:
Brown and Vranesic problems
7.1, 7.3, 7.5, 7.8, 7.13, 7.17

EECS 141 only:
Brown and Vranesic problems
7.33, 7.34

Puzzler #10 (mandatory for EECS 141; extra credit for EECS 140):

You have just taken a new engineering job at a clock company, and your first design assignment is a digital alarm clock with stopwatch and countdown timer capabilities. Draw a block diagram for a circuit to implement this. You should display hours, minutes, seconds (to the tenth of a second) on seven-segment displays, have controls for changing modes (clock, stopwatch, countdown timer), setting time for the clock and countdown timer, and starting/stopping the stopwatch. Assume that you have in input clock with at frequency of 0.1 Hz. You do not need to draw the gate-level circuits for any counters or registers you need, but do need to show how they are connected and draw any “glue logic” gates or flip flops that are needed to control or interconnect the timer.

Staple this sheet to the front of your work, fold vertically, and write your name and homework # on the outside.

©2010 James P.G. Sterbenz – for use only by students enrolled in KU EECS 140 or 141
Reproduction and redistribution is prohibited. Upload to, and hosting by course sites including Course Hero, Cramster, and Notehall is expressly prohibited.