Chapter 7. Flip-Flops, Registers, and a Simple Processor

7.1 Basic latch
- construction of level-sensitive memory element from cross-coupled inverters
- SR latch symbol and design from cross-coupled NOR or NAND gates
- characteristic tables and timing diagrams for latches and flip-flops

7.2 Gated latches
- gated SR latch design from NOR and NAND gates; advantage of NAND

7.3 Gated D latch
- D latch symbol, characteristic table, and design from SR latch or gates
- propagation delays: setup and hold time

7.4 Master-slave and edge triggered D flip-flops
- design of master-slave edge-triggered D flip-flops from latches or gates
- positive and negative edge-triggering and “wedge” symbol and bubble
- comparison of level-sensitive, positive-edge, and negative-edge elements
- clear and preset inputs to flip flops symbol and design using gates

7.5 T flip-flops
- T flip-flop symbol, characteristic, and design from D flip-flop
- use as frequency halver in counter

7.6 JK flip-flops
- JK flip-flop symbol, characteristic, and design from D flip-flop

7.7 Summary of terminology
- latches, gated latches, and flip-flops
- edge-triggered and master-slave

7.8 Registers
- functionality: store multiple bits using flip-flops
- shift register functionality and design from D flop-flops
- parallel-access shift register functionality and design from D flop-flops

7.9 Counters
- functionality and timing diagrams
- asynchronous up- and down-counter design from T flip-flops
- synchronous counter advantages and design from T flip-flops
- enable and clear inputs to counters
- synchronous counter design from D flip-flops
- parallel load using preset and clear or multiplexors

7.10 Reset synchronization
- modulo-$n$ counters using reset

7.11 Other types of counters
- BCD counter functionality and design
- ring and Johnson counters
Chapter 8. Synchronous Sequential Circuits

8.1 Basic design steps
- FSM (finite state machines): states and transitions
- problem specification, state diagrams and state tables
- Moore machines: output values assigned to states
  - outputs labeled within state circles
- state assignment: binary representation of each state
- general sequential circuit design from combinational circuits and flip-flops
- design of sequential circuits using D flip-flops
- sequential-circuit timing diagrams

8.2 State assignment
- alternative state assignments affect circuit complexity
- one-hot encoding

8.3 Mealy state model
- Mealy machine: output values are combination of state and inputs
  - outputs labeled on state transition arcs

8.5 Serial adder example
- Mealy and Moore implementations

Chapter 9. Asynchronous Sequential Circuits

9.1 Asynchronous behavior
- advantages and disadvantages with respect to synchronous sequential circuits
- SR latch analysis with delay element model
- Moore flow (state) table and state diagram

9.1 Asynchronous behavior
- SR latch analysis with delay element model
- Moore flow (state) table and state diagram

9.3 p.599 Race Conditions
- definition and concept of race condition

9.6 Hazards
- definitions and concepts of static and dynamic hazards

Chapter 10. Digital System Design

10.1 Building block circuits
- registers with enable inputs
- SRAM