10.4 NMOS Logic Design

Reading Assignment: 974-980

An alternative to CMOS logic is NMOS logic.

Q:

A: HO: NMOS Logic Circuits

HO: The Depletion Load

HO: The Pseudo-NMOS Load
The Pseudo-NMOS Load

There is another type of active load that is used for NMOS logic, but this load is made from a PMOS transistor!

Hence, NMOS logic that uses this load is referred to as Pseudo NMOS Logic, since not all of the devices in the circuit will be NMOS (the load will be PMOS!).

We therefore call this load the "Pseudo NMOS Load", since it is the load used in Pseudo NMOS logic. But, keep in mind that the pseudo NMOS load is made from a PMOS device (this can cause great confusion!)

\[ V_{DS} = -V \]
\[ v_{GS} - V_t = -(V_{DD} + V_t) \]

\[ V_{DD} \]
\[ i \]

\[ i_D = i \]
\[ v_{GS} = 0 - V_{DD} = -V_{DD} \]
\[ v_{DS} = -V \]
Note that \( v_{GS} = -V_{DD} < V_t \), so that the load is not in cutoff—it can either be in **saturation** or **triode**.

The PMOS will be in **triode** if:

\[
\begin{align*}
  v_{DS} &> v_{GS} - V_t \\
  -v &> -(V_{DD} + V_t) \\
  v &< (V_{DD} + V_t)
\end{align*}
\]

In which case the **current** is:

\[
\begin{align*}
  i_D &= K \left[ 2(v_{GS} - V_t)v_{DS} - v_{DS}^2 \right] \\
  i &= K \left[ -2(V_{DD} + V_t)(-v) - (-v)^2 \right] \\
  i &= K \left[ 2(V_{DD} + V_t)v - v^2 \right]
\end{align*}
\]

Likewise, the PMOS will be in saturation if:

\[
\begin{align*}
  v_{DS} &< v_{GS} - V_t \\
  -v &< -(V_{DD} + V_t) \\
  v &> (V_{DD} + V_t)
\end{align*}
\]

In which case the **current** is:

\[
\begin{align*}
  i_D &= K \left( v_{GS} - V_t \right)^2 - \frac{v_{DS}}{r_o} \\
  i &= K \left( V_{DD} + V_t \right)^2 + \frac{v}{r_o}
\end{align*}
\]
where in this case:

\[ r_o = \frac{1}{\lambda K(\nu_{GS} - \nu_t)^2} = \frac{1}{\lambda K(\nu_{DD} + \nu_t)^2} \]

Combining these two results, we find that the pseudo NMOS load behaves very much like the depletion load:

\[
\begin{align*}
    i &= \begin{cases} 
        K \left[ 2(\nu_{DD} + \nu_t) \nu - \nu^2 \right] & \text{if } 0 < \nu < (\nu_{DD} + \nu_t) \\
        K (\nu_{DD} + \nu_t)^2 + \frac{\nu}{r_o} & \text{if } \nu > (\nu_{DD} + \nu_t)
    \end{cases}
\end{align*}
\]
A Pseudo-NMOS Logic Example
The Depletion Load

Say we connect the gate of a depletion NMOS to its source—we now have a two-terminal device!

This device is called a depletion load.

Since the depletion load is a two-terminal device, its behavior is defined by the relationship between the voltage $v$ across the device and the current $i$ through it.

For example, a resistor is a two terminal device whose behavior (i.e., its relationship between $i$ and $v$) is defined by Ohm's Law ($i = v/R$).

Although the depletion load is decidedly not a resistor, its $i$-$v$ relationship does have some similarities with Ohm's Law.

Q: So what is "Ohm's Law" for a depletion load (i.e., what is $i = f(v)$)?
**A:** A result easily found by implementing our knowledge of depletion MOSFETs!

For a depletion load, we find that:

\[ i_D = i \]
\[ v_{GS} = 0 \]
\[ v_{DS} = v \]
\[ v_{GS} - V_t = -V_t \]

**Q:** But since \( v_{GS} = 0 \), isn’t the NMOS device in cutoff?

**A:** Nope! Notice that this is a depletion MOSFET, and a depletion MOSFET will conduct when \( v_{GS} = 0 \! \)!

Thus the MOSFET in a depletion load will always be either in: a) triode or b) saturation.

**a)** Depletion load MOSFET is in triode if:

\[ v_{DS} < v_{GS} - V_t \]
\[ v < 0 - V_t \]
\[ v < -V_t \]
Therefore, the current will be:

\[
i_D = K \left[ 2(v_{GS} - V_t)v_{DS} - v_{DS}^2 \right]
\]

\[
i = K \left[ 2(0 - V_t)v - v^2 \right]
\]

\[
i = K \left[ -2V_t v - v^2 \right]
\]

b) Depletion load MOSFET is in saturation if:

\[
v_{DS} > v_{GS} - V_t
\]

\[
v > 0 - V_t
\]

\[
v > -V_t
\]

Therefore, the current will be:

\[
i_D = K (v_{GS} - V_t)^2 + \frac{v_{DS}}{r_o}
\]

\[
i = K (0 - V_t)^2 + \frac{v}{r_o}
\]

\[
i = K (-V_t)^2 + \frac{v}{r_o}
\]

\[
i = KV_t^2 + \frac{v}{r_o}
\]

where in this case:

\[
r_o = \frac{1}{\lambda K (v_{GS} - V_t)^2} = \frac{1}{\lambda K (0 - V_t)^2} = \frac{1}{\lambda V_t^2}
\]

**Channel-Length Modulation!**
Combining the two results, we find that “Ohm’s Law” for a depletion load is:

\[ i = \begin{cases} 
K[-2V_t \nu - \nu^2] & \text{if } 0 < \nu < -V_t \\
K'V_t^2 + \frac{\nu}{r_o} & \text{if } \nu > -V_t 
\end{cases} \]

Plotting this function, we find something like this:
Note that the behavior of a Depletion Load and a resistor are very different—however they are precisely the same in two key ways:

1. When the voltage across each device (i.e., resistor and depletion load) is zero, the current through each device is likewise zero (and vice versa!).

2. As the voltage across each device increases, the current through each device increases.

As a result, we can use a depletion load as the “pull-up resistor” in our integrated circuit NMOS logic!
NMOS Logic Circuits

An alternative way to construct a digital logic gate is to simply use a single large resistor as the pull-up network!

If the PDN is open, no current will flow ($i_R = 0$), and thus there will be no voltage drop across the Pull-Up Resistor $R$—the output will be high, just like before!

But, if the PDN is conducting, current will flow ($i_R \neq 0$), and thus there will be a large voltage drop across $R$—the output will be low (sort of)!
This method of constructing digital devices is called **NMOS logic** (for hopefully **obvious** reasons!).

**Q:** Why would we want use NMOS logic?

**A:** Replacing the PUN with a single resistor greatly **simplifies** and **shrinks** the circuit. For complex gates (i.e., gates with **many** inputs), we can reduce the number of required devices (transistors and resistors) by **nearly half**!

**Q:** Yikes! This seems to be a **lot** better. Why wouldn’t we **always** use NMOS logic?

**A:** There are **two** really big problems with NMOS logic (at least, when compared to **CMOS**):

1. Since current flows when the output is low, the static power dissipation is **not zero**.

2. Since current flows when the output is low, \( V_{OL} \) is **not equal** to its ideal value of **zero** (i.e., \( V_{OL} \neq 0 \))!

Additionally, there is **one more** problem when implementing NMOS in **integrated circuits**. **IC** resistors are (relatively) **very large** and difficult to construct.

→ This problem, though, is easily solved—we replace the pull-up **resistor** with an **active load**.