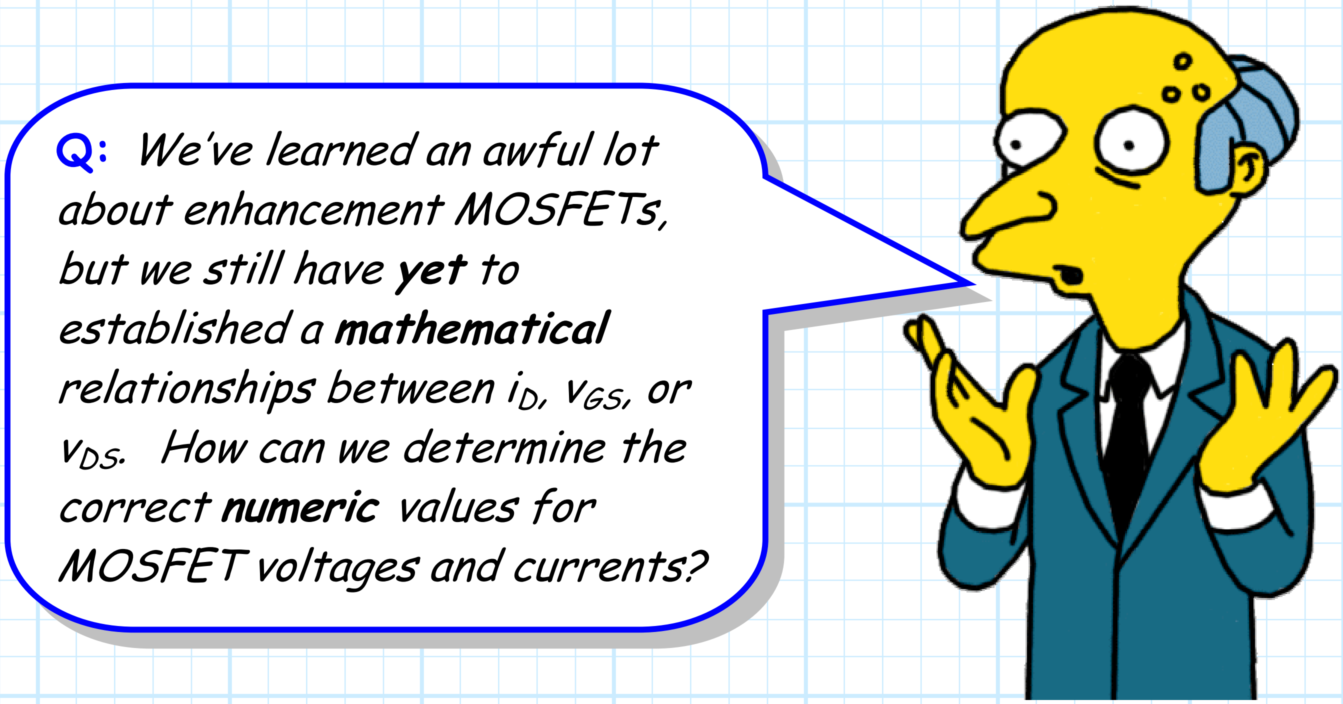
A Mathematical Description of MOSFET Behavior



A: A **mathematical** description of enhancement MOSFET behavior is relatively straightforward ! We actually need to concern ourselves with just **3 equations**.

Specifically, we express the drain current i_D in terms of v_{GS} and v_{DS} for each of the **three MOSFET modes** (i.e., Cutoff, Triode, Saturation).

Additionally, we need to mathematically define the **boundaries** between each of these three modes!

But first, we need to examine some fundamental **physical parameters** that describe a MOSFET device. These parameters include:

$$k' \doteq \text{Process Transconductance Parameter } \left[A/V^2\right]$$

$$\frac{W}{L} = \text{Channel Aspect Ratio}$$

The Process Transconductance Parameter k' is a constant that depends on the process technology used to fabricate an integrated circuit. Therefore, all the transistors on a given substrate will typically have the **same value** of this parameter.

The Channel Aspect Ratio W/L is simply the ratio of channel width W to channel length L. This is the MOSFET device parameter that can be **altered** and **modified** by the circuit designer to satisfy the requirements of the given circuit or transistor.

We can likewise combine these parameter to form a **single** MOSFET device parameter $\boldsymbol{K}$:

$$K = \frac{1}{2} k' \left(\frac{W}{L}\right) \qquad \left[{}^{A}\!/\!{}_{V^2}\right]$$

Now we can mathematically describe the behavior of an enhancement MOSFET! Well do this **one mode at a time**.

CUTOFF

This relationship is very simple—if the MOSFET is in **cutoff**, the drain current is simply **zero** !

$$i_D = 0 \qquad \text{(CUTOFF mode)}$$

TRIODE

When in **triode** mode, the drain current is dependent on **both** v_{GS} and v_{DS}:

$$\begin{aligned} i_D &= k'\left(\frac{W}{L}\right)\left[\left(v_{GS}-V_t\right)v_{DS}-\frac{1}{2}\,v_{DS}^2\right] \qquad \text{(TRIODE mode)} \\ &= K\left[2\left(v_{GS}-V_t\right)v_{DS}-v_{DS}^2\right] \end{aligned}$$

This equation is valid for **both** NMOS and PMOS transistors (**if** in TRIODE mode). Recall that for **PMOS** devices, the values of v_{GS} and v_{DS} are **negative**, but note that this will result (correctly so) in a **positive** value of i_D.

SATURATION

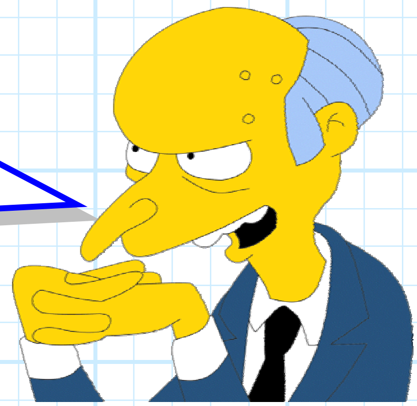
When in **saturation** mode, the drain current is (approximately) dependent on v_{GS} **only**:

$$i_D = \frac{1}{2} k' \left(\frac{W}{L} \right) (v_{GS} - V_t)^2 \qquad \text{(SATURATION mode)}$$
$$= K (v_{GS} - V_t)^2$$

Thus, we see that the drain current in saturation is proportional to **excess gate voltage squared**!

This equation is likewise valid for **both** NMOS and PMOS transistors (**if** in SATURATION mode).

Q: *OK, so know we know the expression for **drain current** i_D in each of the **three** MOSFET modes, but how will we know **what mode** the MOSFET is in?*



A: We must determine the **mathematical boundaries** of each mode. Just as before, we will do this **one mode at a time**!

CUTOFF

A MOSFET is in **cutoff** when **no channel** has been induced. Thus, for an enhancement **NMOS** device:

$$\text{if} \quad v_{GS} - V_t < 0 \quad \text{then NMOS in CUTOFF}$$

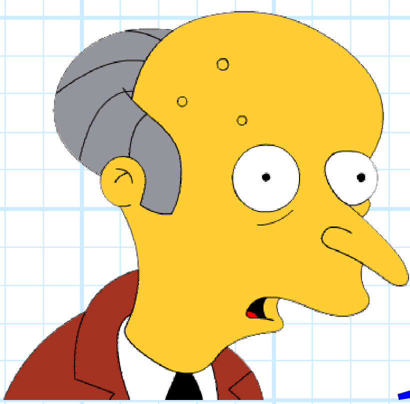
Like wise, for an enhancement **PMOS** device:

$$\text{if} \quad v_{GS} - V_t > 0 \quad \text{then PMOS in CUTOFF}$$

TRIODE

For triode mode, we know that a channel **is** induced (i.e., an inversion layer is present).

Additionally, we know that when in triode mode, the voltage v_{DS} is not sufficiently large for NMOS, or sufficiently small (i.e., sufficiently negative) for PMOS, to pinch off this induced channel.



Q: *But how **large** does v_{DS} need to be to pinch off an NMOS channel? How can we determine **if** pinch off has occurred?*

A: The answer to that question is surprisingly **simple**. The induced channel of an NMOS device is pinched off **if** the voltage v_{DS} is greater than the **excess gate voltage**! I.E.:

$$\text{if} \quad v_{DS} > v_{GS} - V_t \quad \text{then NMOS channel is "pinched off"}$$

Conversely, for PMOS devices, we find that:

$$\text{if} \quad v_{DS} < v_{GS} - V_t \quad \text{then PMOS channel is "pinched off"}$$

These statements of course mean that an NMOS channel is **not** pinched off if $v_{DS} < v_{GS} - V_t$, and a PMOS channel is **not** pinched off if $v_{DS} > v_{GS} - V_t$. Thus, we can say that an **NMOS** device is in the **TRIODE** mode:

$$\text{if} \quad v_{GS} - V_t > 0 \quad \text{and} \quad v_{DS} < v_{GS} - V_t \quad \text{then NMOS in TRIODE}$$

Similarly, for **PMOS**:

$$\text{if} \quad v_{GS} - V_t < 0 \quad \text{and} \quad v_{DS} > v_{GS} - V_t \quad \text{then PMOS in TRIODE}$$

SATURATION

Recall for SATURATION mode that a channel **is** induced, and that channel **is** pinched off.

Thus, we can state that for **NMOS**:

$$\text{if} \quad v_{GS} - V_t > 0 \quad \text{and} \quad v_{DS} > v_{GS} - V_t \quad \text{then NMOS in SAT.}$$

And for **PMOS**:

$$\text{if} \quad v_{GS} - V_t < 0 \quad \text{and} \quad v_{DS} < v_{GS} - V_t \quad \text{then PMOS in SAT.}$$

We now can construct a **complete** (continuous) expression relating drain current i_D to voltages v_{DS} and v_{GS}. For an **NMOS** device, this expression is:

$$i_D = \begin{cases} 0 & \text{if} \quad v_{GS} - V_t < 0 \\ K\left[2\left(v_{GS} - V_t\right)v_{DS} - v_{DS}^2\right] & \text{if} \quad v_{GS} - V_t > 0 \text{ and } v_{DS} < v_{GS} - V_t \\ K\left(v_{GS} - V_t\right)^2 & \text{if} \quad v_{GS} - V_t > 0 \text{ and } v_{DS} > v_{GS} - V_t \end{cases}$$

Likewise, for a **PMOS** device we find:

$$i_D = \begin{cases} 0 & \text{if} \quad v_{GS} - V_t > 0 \\ K\left[2(v_{GS} - V_t)v_{DS} - v_{DS}^2\right] & \text{if} \quad v_{GS} - V_t < 0 \text{ and } v_{DS} > v_{GS} - V_t \\ K(v_{GS} - V_t)^2 & \text{if} \quad v_{GS} - V_t < 0 \text{ and } v_{DS} < v_{GS} - V_t \end{cases}$$

Let's take a look at what these expressions look like when we **plot** them. Specifically, for an NMOS device let's plot i_D versus v_{DS} for different values of v_{GS}: