CMOS Device Structure

For every CMOS device, there are essentially two separate circuits:

1) The Pull-Up Network

2) The Pull-Down Network

The basic CMOS structure is:

A CMOS logic gate must be in one of two states!
**State 1:** PUN is open and PDN is conducting.

In this state, the output is LOW (i.e., $Y=0$).

**State 2:** PUN is conducting and PDN is open.

In this state, the output is HIGH (i.e., $Y=1$).
Thus, the PUN and the PDN essentially act as switches, connecting the output to either $V_{DD}$ or to ground:

* Note that the key to proper operation is that one switch must be closed, while the other must be open.

* Both switches closed or both switches open would cause an ambiguous digital output!

* To prevent this from occurring, the PDN and PUN must be complementary circuits.
For example, consider the CMOS inverter:

For more complex digital CMOS gates (e.g., a 4-input OR gate), we find:

1) The PUN will consist of multiple inputs, therefore requires a circuit with multiple PMOS transistors.

2) The PDN will consist of multiple inputs, therefore requires a circuit with multiple NMOS transistors.