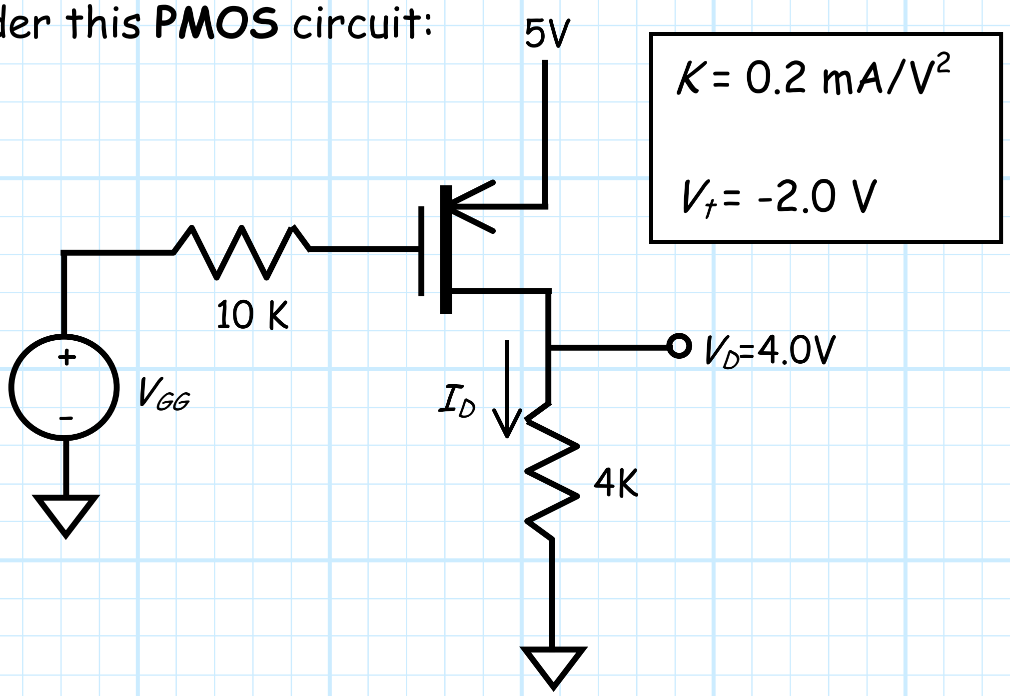
Example: PMOS Circuit Analysis

Consider this PMOS circuit:



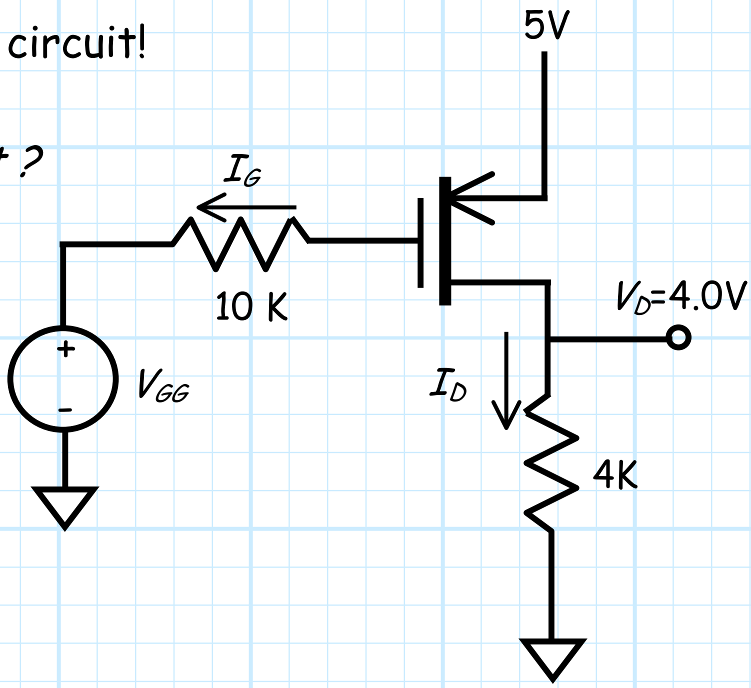
For this problem, we know that the **drain voltage** $V_D = 4.0$ V (with respect to ground), but we do **not** know the value of the voltage source V_{GG}.

Let's attempt to **find** this value V_{GG}!

First, let's ASSUME that the PMOS is in **saturation** mode.

Therefore, we ENFORCE the **saturation** drain current equation $I_D = K\left(V_{GS} - V_t\right)^2$.

Now we must ANALYZE this circuit!



Q: *Yikes! Where do we start ?*

A: The best way to start is by "**picking the low-hanging fruit**". In other words, determine the **obvious** and easy values. **Don't** ask, "What is V_{GG}?", but **instead** ask, "What **do** I know?" !

There are **lots** of things that we can **quickly** determine about this circuit!

$$I_G = 0.0 \quad mA$$

$$V_S = 5.0 \quad V$$

$$I_D = \frac{V_D - 0}{4} = \frac{4.0 - 0}{4} = 1 \ mA$$

$$V_G = V_{GG} - 10\,I_G = V_{GG} - 10(0) = V_{GG}$$

Therefore, we can likewise determine:

$$V_{DS} = V_D - V_S = 4.0 - 5.0 = -1.0 \ V$$

$$V_{GS} = V_G - V_S = V_{GG} - 5.0 \quad V$$

Note what we have **quickly determined**—the **numeric** value of drain current (I_D=1.0 mA) and the voltage drain-to-source (V_{DS}=-1.0) Moreover, we have determined the value V_{GS} in terms of **unknown** voltage V_{GG} ($V_{GS} = V_{GG} - 5.0$).

We've determined all **the important stuff** (i.e., V_{GS}, V_{DS}, I_D) !

We can now relate these values using our PMOS **drain current equation**. Recall that we ASSUMED **saturation**, so **if** this assumption is correct:

$$I_D = K\left(V_{GS} - V_t\right)^2$$

Inserting into this equation our knowledge from above, along with our **PMOS** values K=0.2 mA/V^2 and V_t=-2.0, we get:

$$\begin{aligned} I_D &= K\left(V_{GS} - V_t\right)^2 \\ 1.0 &= 0.2\left(V_{GS} - (-2.0)\right)^2 \\ 5.0 &= \left(V_{GS} + 2.0\right)^2 \end{aligned}$$

Be **careful** here! Note in the above equation that threshold voltage V_t is **negative** (since PMOS) and that I_D and K are both written in terms of **milliamps** (mA).

Now, we solve this equation to find the value of V_{GS}!

$$5.0 = (V_{GS} + 2.0)^2$$
$$\pm\sqrt{5} = V_{GS} + 2.0$$
$$\pm\sqrt{5} - 2.0 = V_{GS}$$

Q: *So V_{GS} is **both** $\sqrt{5} - 2.0 = 0.24\,V$ **and** $-\sqrt{5} - 2.0 = -4.23\,V$? How can this be **possible**?*

A: It's **not** possible! The solution is **either** V_{GS}=0.24 V **or** V_{GS} = -4.23 V.

Q: *But how can we tell **which** solution is correct?*

A: We must choose a solution that is **consistent** with our original ASSUMPTION. Note that **neither** of the solutions **must** be consistent with the saturation ASSUMPTION, an event meaning that our ASSUMPTION was wrong.

However, **one** (but **only one**!) of the two solutions may be consistent with our saturation ASSUMPTION—**this** is the value that we choose for V_{GS}!

For this example, where we have ASSUMED that the PMOS device is in **saturation**, the voltage gate-to-source V_{GS} must be **less** (remember, it's a **PMOS** device!) than the **threshold voltage**:

$$V_{GS} < V_t$$
$$V_{GS} < -2.0\,V$$

Clearly, one of our solutions **does** satisfy this equation ($V_{GS} = -4.23 < -2.0$), and therefore we choose the **solution** $V_{GS} = -4.23\ V$.

Q: *Does this mean our saturation ASSUMPTION is* ***correct?***

A: **NO!** It merely means that our saturation ASSUMPTION **might** be correct! We need to CHECK the other inequalities to know for **sure**.

Now, returning to our circuit **analysis**, we can quickly determine the **unknown** value of V_{GG}. Recall that we **earlier** determined that:

$$V_{GS} = V_{GG} - 5.0$$

And now, since we "know" that the V_{GS}=-4.23 V, we can determine that:

$$\begin{aligned} V_{GG} &= V_{GS} + 5.0 \\ &= -4.23 + 5.0 \\ &= 0.77\ V \end{aligned}$$

This solution (V_{GG}=0.77 V) is of course true **only if** our original ASSUMPTION was correct. Thus, we must CHECK to see if our **inequalities** are valid:

We of course already know that the **first** inequality is true—a p-type channel is induced:

$$V_{GS} = -4.23 < -2.0 = V_t \ \checkmark$$

And, since the **excess gate voltage** is $V_{GS} - V_t = -2.23\ V$, the **second** inequality:

$$V_{DS} = -1.0 > -2.23 = V_{GS} - V_t \quad \times$$

shows us that our ASSUMPTION was **incorrect**!

→ Time to make a **new** ASSUMPTION and **start over**!

So, let's **now** ASSUME the PMOS device is in **triode** region.

Therefore ENFORCE the drain current equation:

$$i_D = K\left[2\left(V_{GS} - V_t\right)V_{DS} - V_{DS}^2\right]$$

Now let's ANALYZE our circuit!

Note that most of our **original** analysis was **independent** of our PMOS mode ASSUMPTION. Thus, we **again** conclude that:

$I_G = 0.0$ mA

$V_S = 5.0$ V

$$I_D = \frac{V_D - 0}{4} = \frac{4.0 - 0}{4} = 1\ mA$$

$$V_G = V_{GG} - 10\,I_G = V_{GG} - 10(0) = V_{GG}$$

Therefore,

$$V_{DS} = V_D - V_S = 4.0 - 5.0 = -1.0 \;\; V$$

$$V_{GS} = V_G - V_S = V_{GG} - 5.0 \quad V$$

Now, inserting these values in the **triode drain current equation**:

$$\begin{aligned} i_D &= K\left[2\left(V_{GS} - V_t\right)V_{DS} - V_{DS}^2\right] \\ 1.0 &= 0.2\left[2\left(V_{GS} - (-2)\right)(-1) - (-1)^2\right] \\ 5.0 &= \left[-2\left(V_{GS} + 2\right) - 1\right] \end{aligned}$$

Look! **One** equation and **one** unknown! Solving for V_{GS} we find:

$$\begin{aligned} 5.0 &= \left[-2\left(V_{GS} + 2\right) - 1\right] \\ 6.0 &= -2\left(V_{GS} + 2\right) \\ -3.0 &= V_{GS} + 2 \\ -5.0 &= V_{GS} \end{aligned}$$

Thus, we find that V_{GS} = -5.0 V, so that we can find the **value** of voltage source V_{GG} :

$$\begin{aligned} V_{GS} &= V_{GG} - 5.0 \\ -5.0 &= V_{GG} - 5.0 \\ 0.0 &= V_{GG} \end{aligned}$$

The voltage source V_{GG} is equal to **zero**—provided that our triode ASSUMPTION was **correct**.

To find out **if** the ASSUMPTION is correct, we must CHECK our **triode inequalities**.

First, we CHECK to see if a channel has indeed been **induced:**

$$V_{GS} = -5.0 < -2.0 = V_t \quad \checkmark$$

Next, we CHECK to make sure that our channel is **not** in pinch-off. Noting that the **excess gate voltage** is $V_{GS} - V_t = -5.0 - (-2.0) = -3.0\, V$, we find that:

$$V_{DS} = -1.0 > -3.0 = V_{GS} - V_t \quad \checkmark$$

Our **triode** ASSUMPTION is **correct**! Thus, the voltage source V_{GG} = 0.0 V.