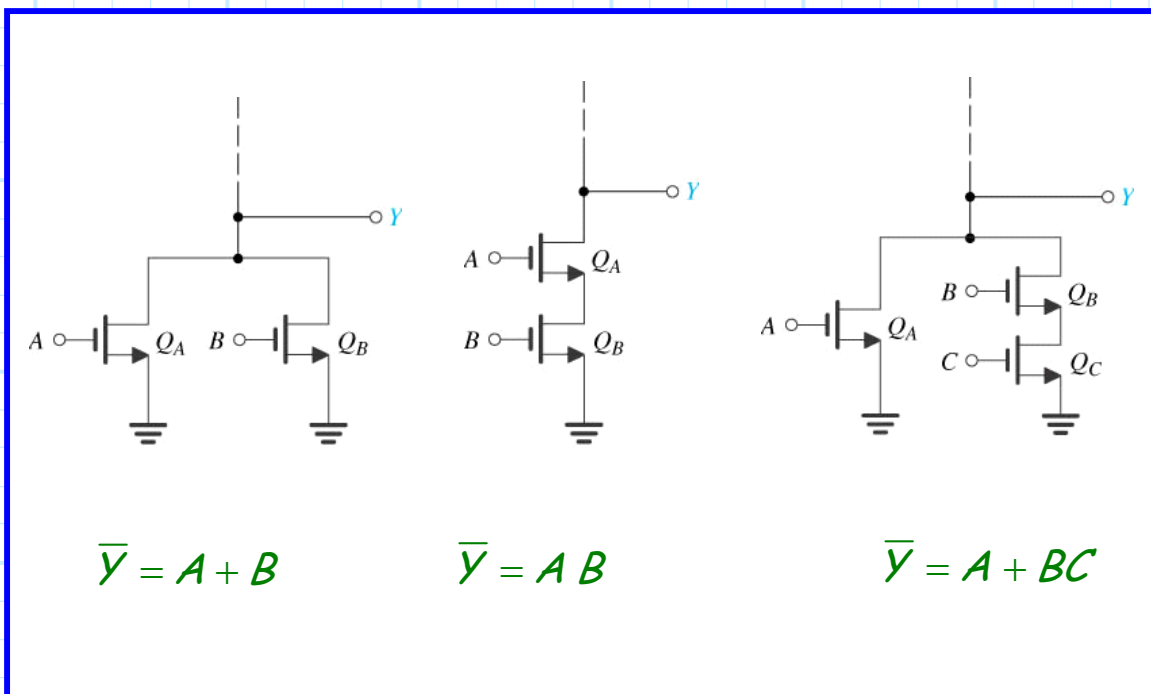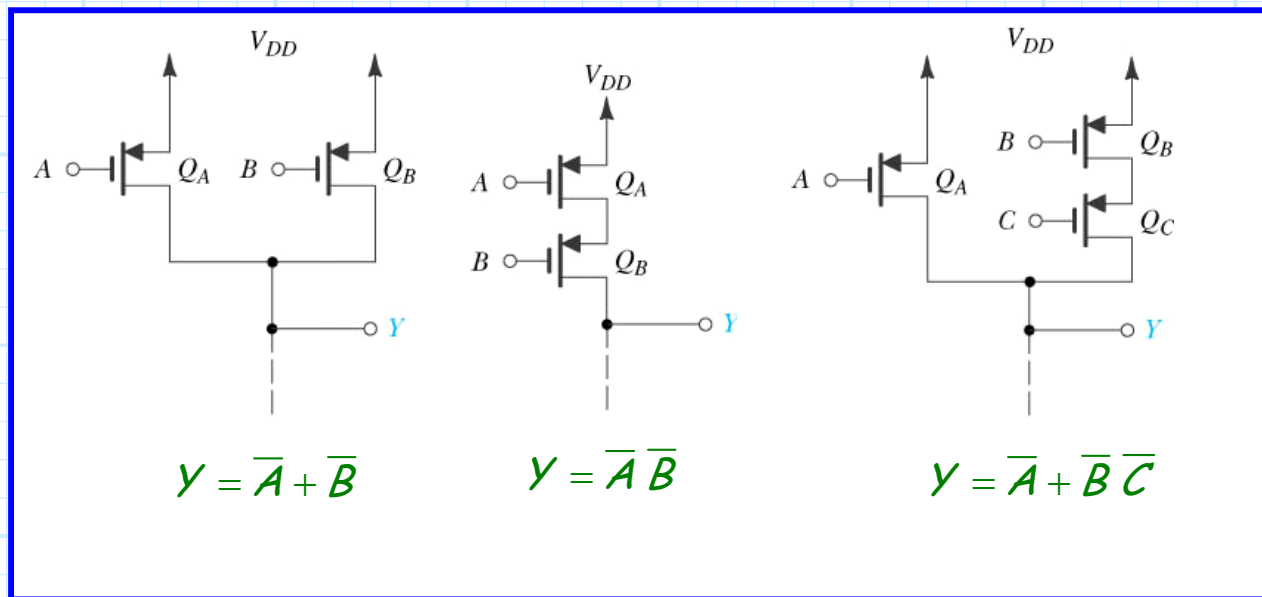# Examples of CMOS Logic Gates
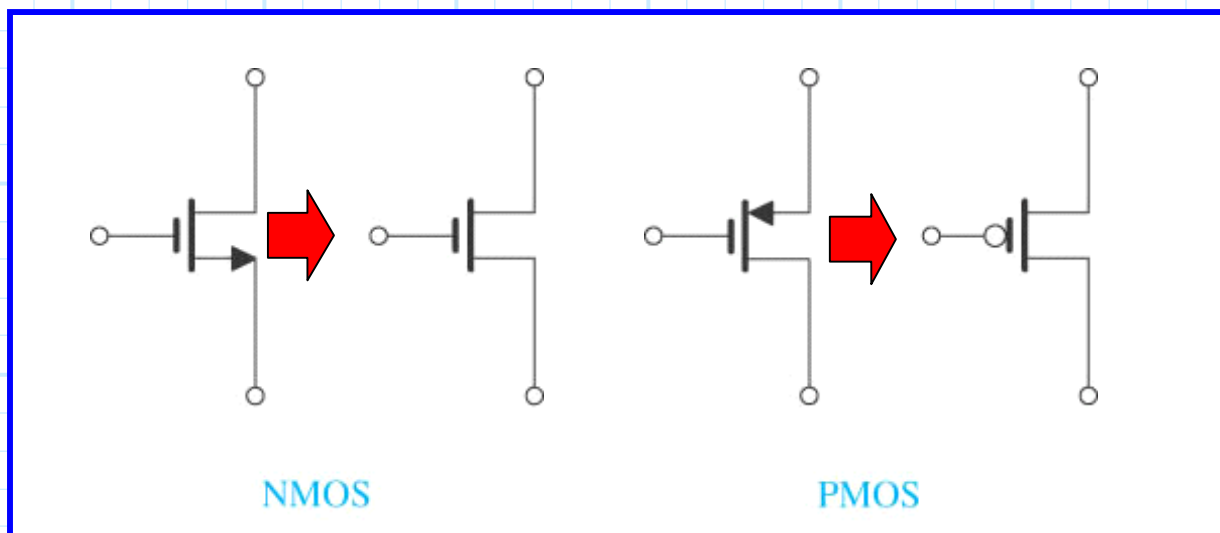
See if you can determine the **Boolean expression** that describes these **pull-down networks**:

$$\overline{Y} = A + B \qquad \overline{Y} = A\,B \qquad \overline{Y} = A + BC$$

See now if you can determine the **Boolean algebraic expression** for these **pull-up networks**:

$$Y = \overline{A} + \overline{B} \qquad\qquad Y = \overline{A}\,\overline{B} \qquad\qquad Y = \overline{A} + \overline{B}\,\overline{C}$$
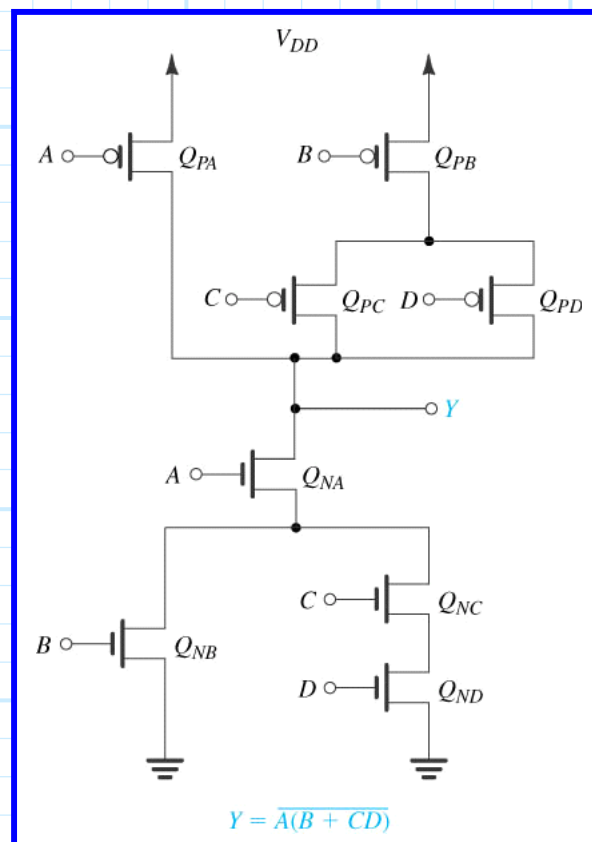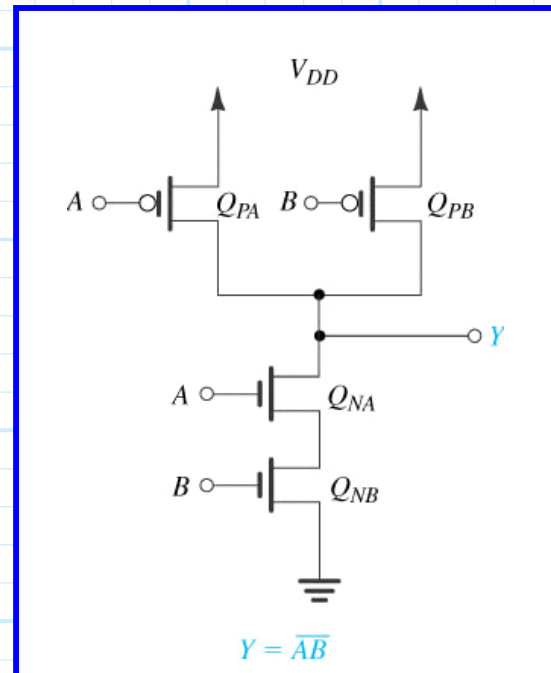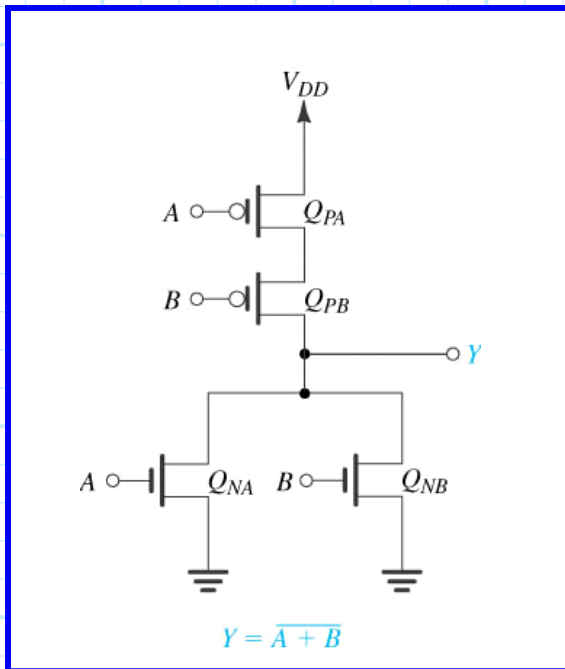
Now, we will make a simplifying **change of symbols**:

NMOS   PMOS

Effectively, these symbols represent the fact that we are now considering MOSFETs as **switches,** which can be placed either in an **open** state or a **conducting** state.

Note there are **two** kinds of "switches"—the ones that conduct when the input is high (i.e., **NMOS**) and ones that conduct when the input is low (i.e., **PMOS**).

And now consider **these** logic gates:

$$Y = \overline{A + B}$$

$$Y = \overline{AB}$$

$$Y = \overline{A(B + CD)}$$

Note the PUN and the PDN for each of these circuits have **equivalent Boolean expressions** (make sure **you** see this!).