

Gate Propagation Delay

Say the **input** to a logic gate changes its state (e.g., 0 to V^+ , or V^+ to 0). The **output** of the gate will likely change state as a result.

However, the output will **not change instantaneously** when the input changes. Instead, the output will change **after a small delay**.

We call this delay the **propagation delay**. Ideally, this delay is as **small** as possible; typically, it is on the order of a few **nanoseconds** or less.

Often, the delay when the output changes from **low to high** is a **different value** than the delay when the output changes from **high to low**. Therefore, we can define:

t_{pHL} = delay for output changing from high to low

t_{pLH} = delay for output changing from low to high

We can therefore define the **propagation delay** t_p as the **average** of these values:

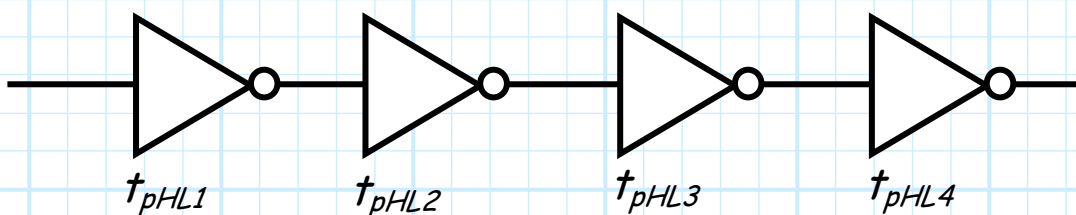
$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

Q: *Why does this delay occur?*

A: Again, the reason is **output capacitance!**

It takes a **non-zero** amount of time to **charge** or **discharge** a capacitor. In other words, the output voltage **cannot** change instantaneously to a change in the input.

Propagation delay is a particularly disturbing **problem** when we construct a **complex** digital circuit consisting of **many** interconnecting stages. For example:



The **total** propagation delay for this complex digital circuit is therefore:

$$t_p = t_{pHL1} + t_{pHL2} + t_{pHL3} + t_{pHL4}$$

Thus, although the propagation delay of **one** individual logic gate may be insignificant, the **total delay** through a complex digital circuit consisting of many stages and gates can be quite **large!**

This can cause **big problems** in the precise timing required of sophisticated and complex digital systems!