**Peak CMOS Current**

**Q:** What do you mean, "peak CMOS current"? I thought that the drain current of a CMOS inverter was \( i_D = 0 \)?

**A:** The drain current \( i_D \) is zero specifically when \( v_I = 0 \) or \( v_I = V_{DD} \). But, consider when \( v_I \) is some value between 0 and \( V_{DD} \).

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**Diagram:**

- The diagram shows the relationship between input voltage \( v_I \) and output voltage \( v_O \) for a CMOS inverter.

- The points labeled A, B, C, and D correspond to different regions of operation:
  - **A:** \( V_{OH} = V_{DD} \) with a slope of -1 indicating the transition between \( Q_N \) off and triode region.
  - **B:** The point \( (\frac{V_{DD}}{2} + V_I) \) showing the transition between different regions.
  - **C:** \( (\frac{V_{DD}}{2} - V_I) \) with a slope of -1 indicating the transition in the input range.
  - **D:** The transition point \( V_{DD} - V_I \) indicating the off region for the output.

- The diagram also highlights points \( V_{OL} = 0 \) and \( V_{IH} \) as critical points for understanding the operation of the CMOS inverter.

- The equation \( V_{th} = \frac{V_{DD}}{2} \) is used to define the threshold voltage for the transition.
Note it is apparent from the transfer function that:

1. If $V_t < V_I < V_{DD}/2$, then $Q_N$ is in saturation and $Q_P$ is in triode.

2. If $V_I = V_{DD}/2$, then $Q_N$ and $Q_P$ are both in saturation.

3. If $V_{DD}/2 < V_I < (V_{DD} - V_t)$, then $Q_N$ is in triode and $Q_P$ is in saturation.

Note that for each of these three cases, a conducting channel is present in both transistors $Q_N$ and $Q_P$.

The drain current $i_D$ is therefore non-zero !!!

Note that the peak current $i_D^{peak}$ occurs when $V_I = V_{DD}/2$. 
A: The answer is rather obvious! The peak current occurs when $\nu_I = V_{DD}/2$. For that situation, we know that both transistor $Q_N$ and $Q_P$ are in saturation—and we know the current through a MOSFET when in saturation is:

"K times the excess gate voltage squared"

For this case, $\nu_{GSN} = \nu_I = V_{DD}/2$, thus:

$$i_D^{peak} = K_n (\nu_{GSN} - \nu_{th})^2$$
$$= K (V_{DD}/2 - \nu_f)^2$$

If we wish to minimize the dynamic power dissipation $P_D$, then we need to minimize this current value (e.g., minimize $K$, or maximize $\nu_f$).

Q: I can’t wait to find out the value of this peak current $i_D^{peak}$!!

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