

## 3.3- Modeling the Diode Forward Characteristic

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$$\text{e.g., } v_D(t) = 0.7V \quad \therefore V_D = 0.7 \text{ and } v_d(t) = 0.0$$

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# Transcendental Solutions of Junction Diode Circuits

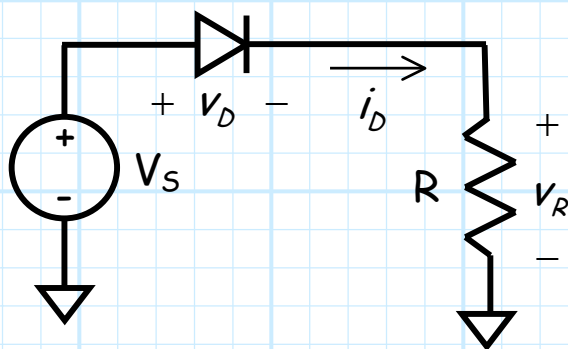
In a previous example, we were able to use the junction diode equation to **algebraically** analyze a circuit and find **numeric** solutions for all circuit currents and voltages.

However, we will find that this type of circuit analysis is, in general, often **impossible** to achieve using the junction diode equation!



*Q: Impossible !?! I must intercede here, and point out that you are clearly wrong. If I have an explicit mathematical description of each device in a circuit (which I do for a junction diode), I can use KVL and KCL to analyze **any** circuit.*

**A:** Although we can always determine a numerical solution, it is often impossible to find this solution **algebraically**. Consider this **simple** junction diode circuit:



From KVL:

Likewise, from the **junction** diode equation:

$$i_D = I_s \left( e^{v_D/nV_T} - 1 \right)$$

Equating these two, we have a **single** equation with a **single** unknown ( $v_D$ ):

$$\frac{V_s - v_D}{R} = I_s \left( e^{v_D/nV_T} - 1 \right)$$

*Q: Precisely! Just as I said! You have 1 equation with 1 unknown. Go solve this equation for  $v_D$ , and then you can determine all other unknown voltages and currents (i.e.,  $i_D$  and  $v_R$ ). Gosh, is there any problem that I cannot solve?*



**A:** But that's the problem! What is the algebraic solution of  $v_D$  for the equation:

$$\frac{V_s - v_D}{R} = I_s \left( e^{v_D/nV_T} - 1 \right)$$



????

The above equation is known as a **transcendental equation**. It is an algebraic expression for which there is **no algebraic solution!**

**Examples** of transcendental equations include:

$$x = \cos[x], \quad y^2 = \ln[y], \quad \text{or} \quad 4 - x = 2^x$$

**Q:** *But, we could build that simple junction diode circuit in the lab. Therefore  $v_D$ ,  $i_D$  and  $v_R$  must have **some** numeric value, right !?!*

**A:** Absolutely! For every value of source voltage  $V_s$ , resistance  $R$ , and junction diode parameters  $n$  and  $I_s$ , there is a specific numerical solution for  $v_D$ ,  $i_D$  and  $v_R$ . However, we **cannot** find this **numerical** solution with **algebraic** methods!

**Q:** *Well then how the heck do we find solution??*

**A:** We use what is know as **numerical methods**, often implementing some **iterative** approach, typically with the help of a **computer** (see example 3.4 on pp. 154-155).

This generally involves **more work** than we wish to do when analyzing junction diode circuits!

**Q:** *So just how **do** we analyze junction diode circuits??*

**A:** We replace the junction diodes with **circuit models** that **approximate** junction diode behavior!



**Q:** *Oh you're tricky, but you are still clearly **wrong** (thus **I** am clearly right). Recall in an **earlier example** we analyzed a junction diode circuit, but we did **not** use "approximate models" nor "numerical methods" to find the answer!*

**A:** This is absolutely correct; we did **not** use approximate models or numerical methods to solve that problem. However, if you look back at that example, you will find that the problem was a bit **contrived**.

\* Recall that effectively, we were **given** the voltage across one diode as part of the problem statement. We were then asked to find the **source voltage**  $V_S$ .

\* This was a bit of an **academic** problem, as in the "real world" it is **unlikely** that we would somehow know the voltage across the diode without knowing the value of the voltage source that produced it!

**Example: A Junction Diode Circuit**

Consider the following circuit with two junction diodes:

The diodes are identical, with  $n = 1$  and  $I_S = 10^{-14}$  A.

**Q:** *If the current through the resistor is 6.5 mA, what is the voltage of source  $V_S$ ??*

**A:** This is a **difficult** problem to solve! Certainly, we cannot just write:

$$V_S =$$

and then the answer. Instead, let's just determine **what we can**, and see what happens!

- \* Thus, problems like this previous example are sometimes used by professors to create junction diode circuit problems that are solvable, **without** encountering a dreaded **transcendental equation!**
- \* In the real world, we typically know **neither** the diode voltage **nor** the diode current directly—transcendental equations are most often the **sad** result!
- \* **Instead** of applying numerical techniques, we will find it much faster (albeit slightly less accurate) to apply **approximate circuit models.**

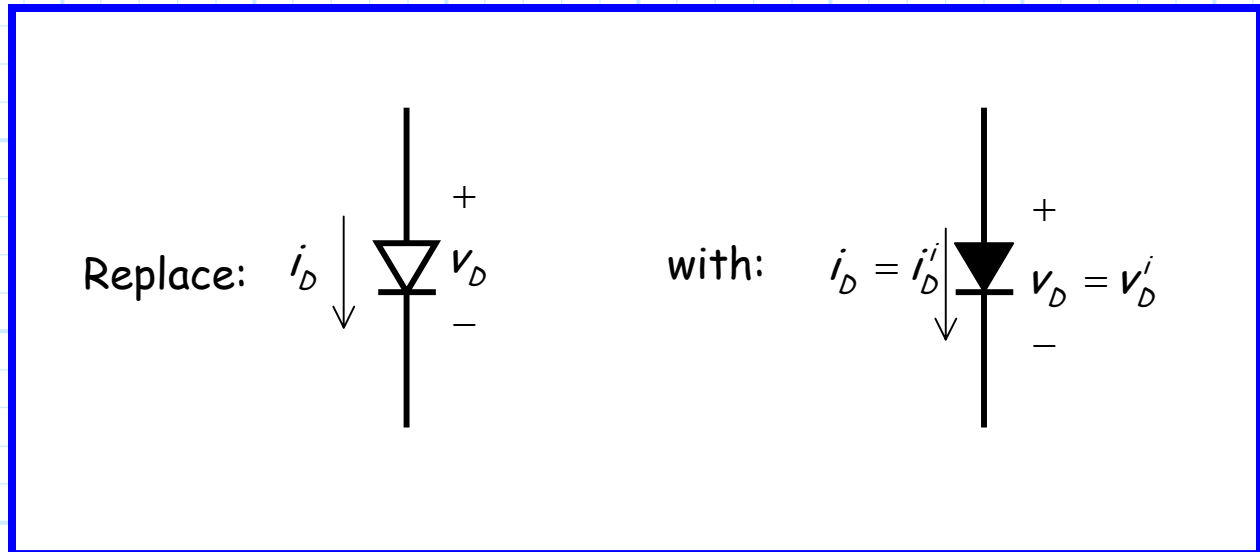


*I wish I had a **nickel**  
for every time my  
software has **crashed**—  
Oh wait, **I do!***



# The Ideal Diode Model

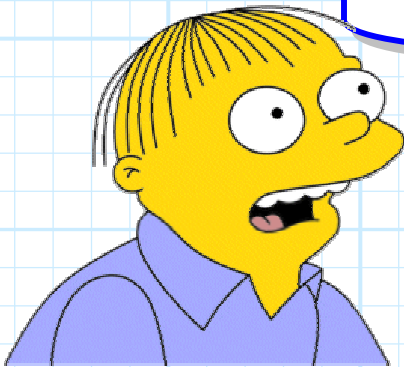
One way to analyze junction diode circuits is simply to **assume** the junction diodes are **ideal**. In other words:



We **know** how to analyze **ideal** diode circuits (recall sect. 3.1)!

**IMPORTANT NOTE !!! PLEASE READ THIS CAREFULLY:**

Make sure you analyze the resulting circuit **precisely** as we did in section 3.1. You **assume** the same **ideal** diode modes, you **enforce** the same **ideal** diode values, and you **check** the same **ideal** diode results, precisely as before. Once we replace the junction diodes with ideal diodes, we have an ideal diode circuit—**no junction diodes** are involved!



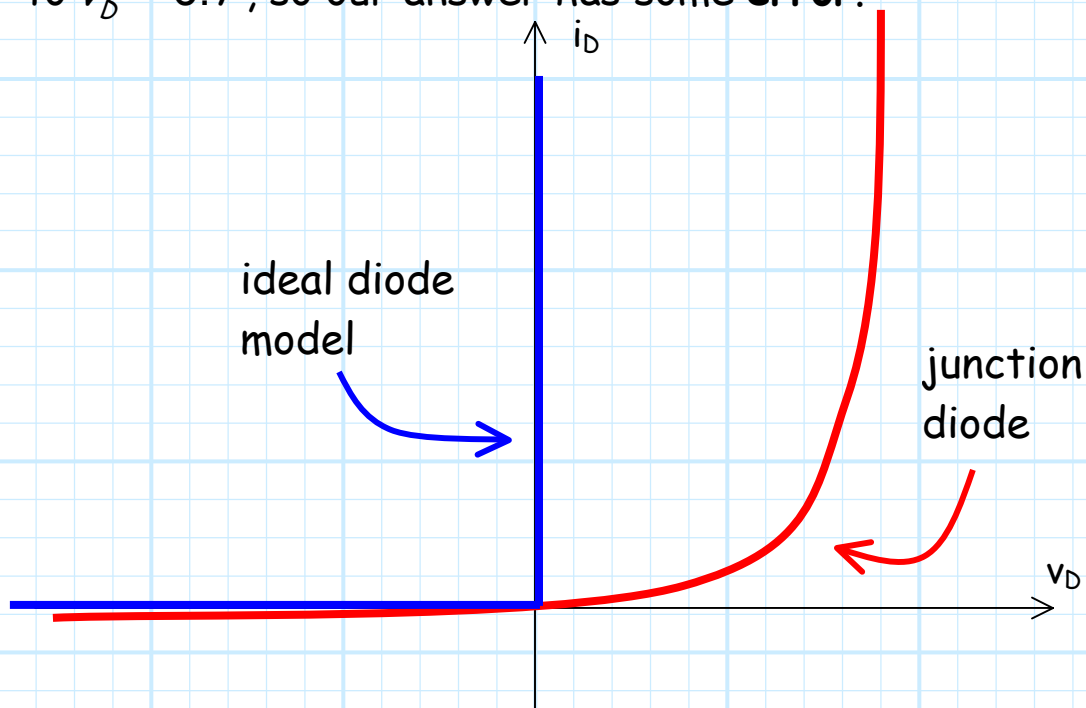
Q: But, ideal diodes are **not** junction diodes; won't we get the **wrong** answer???

A: **YES !!!** Darn right we won't ! However, the answers, albeit incorrect, will be **close** to the actual values. In other words, our answers will be **approximately** correct.

We **approximate** a junction diode as an ideal diode.

**→** Our answers are therefore—**approximations !!**

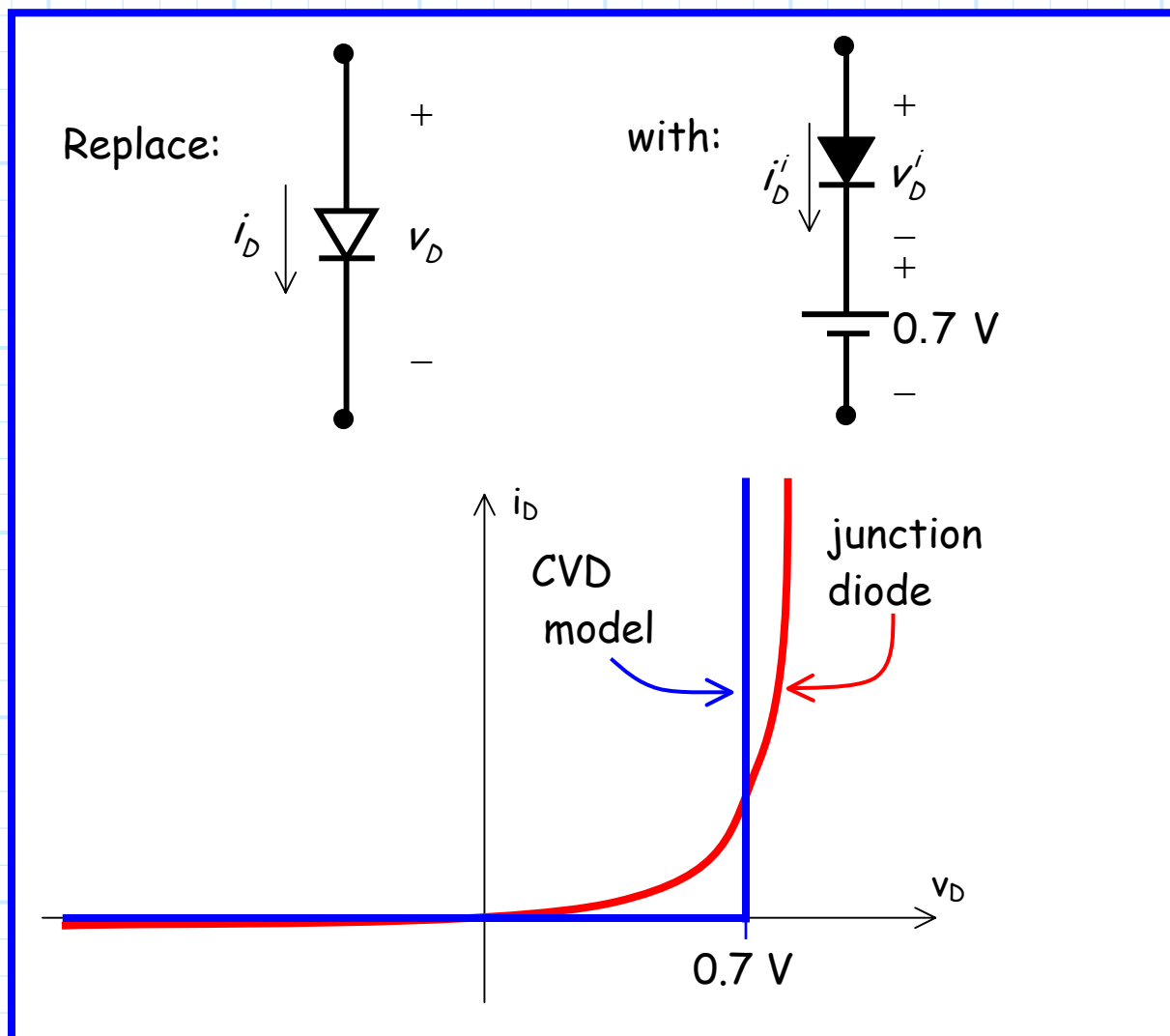
For example, if using the ideal diode model we find that current  $i_D = i_D^i > 0$ , then the diode voltage determined will be  $v_D = v_D^i = 0$ . Of course, the **exact** solution will be some value closer to  $v_D = 0.7$ , so our answer has some **error**.



# The Constant Voltage Drop (CVD) Model

**Q:** We know if *significant positive current flows through a junction diode*, the diode voltage will be some value near 0.7 V. Yet, the ideal diode model provides an approximate answer of  $v_D=0$  V. Isn't there a more *accurate* model?

**A:** Yes! Consider the **Constant Voltage Drop (CVD)** model.



In other words, replace the junction diode with **two** devices—an **ideal diode** in series with a **0.7 V voltage source**.

To find **approximate** current and voltage values of a junction diode circuit, follow these steps:

**Step 1** - Replace each junction diode with the **two** devices of the **CVD model**.

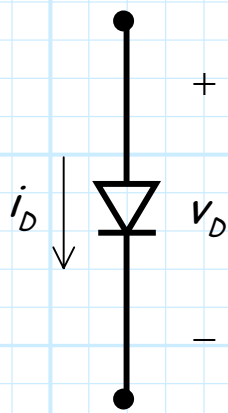
Note you now have an **IDEAL** diode circuit! There are **no junction diodes** in the circuit, and therefore **no junction diode** knowledge need be (or should be) used to analyze it.

**Step 2** - Analyze the **IDEAL** diode circuit. Determine  $i_D^i$  and  $v_D^i$  for each ideal diode.

**IMPORTANT NOTE!!! PLEASE READ THIS CAREFULLY:**

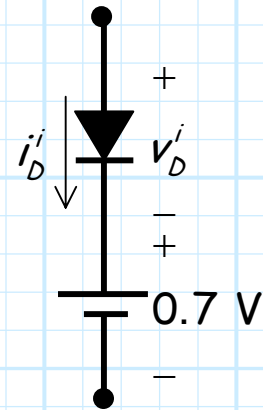
Make sure you analyze the resulting circuit **precisely** as we did in section 3.1. You **assume** the same **IDEAL** diode modes, you **enforce** the same **IDEAL** diode values, and you **check** the same **IDEAL** diode results, **precisely** as before. Once we replace the junction diodes with the CVD model, we have an **IDEAL** diode circuit—**no junction diodes** are involved!

**Step 3** - Determine the **approximate** values  $i_D$  and  $v_D$  of the **junction diode** from the **ideal** diode values  $i_D^i$  and  $v_D^i$ :



$$i_D \approx i_D^i$$

$$v_D \approx v_D^i + 0.7$$



Note therefore, if the **IDEAL** diode (note here I said **IDEAL** diode) is **forward** biased ( $i_D^i > 0$ ), then the **approximation** of the **junction** diode current will likewise be positive ( $i_D > 0$ ), and the **approximation** of the **junction** diode voltage (unlike the **ideal** diode voltage of  $v_D^i = 0$ ) will be:

$$\begin{aligned} v_D &= v_D^i + 0.7 \\ &= 0.0 + 0.7 \\ &= 0.7 \text{ V} \end{aligned}$$

However, if the **IDEAL** diode is **reversed** biased ( $i_D^i = 0$ ), then the **approximation** of the **junction** diode current will likewise be zero ( $i_D = 0$ ), and the **approximation** of the **junction** diode voltage (unlike the **ideal** diode voltage of  $v_D^i < 0$ ) will be:

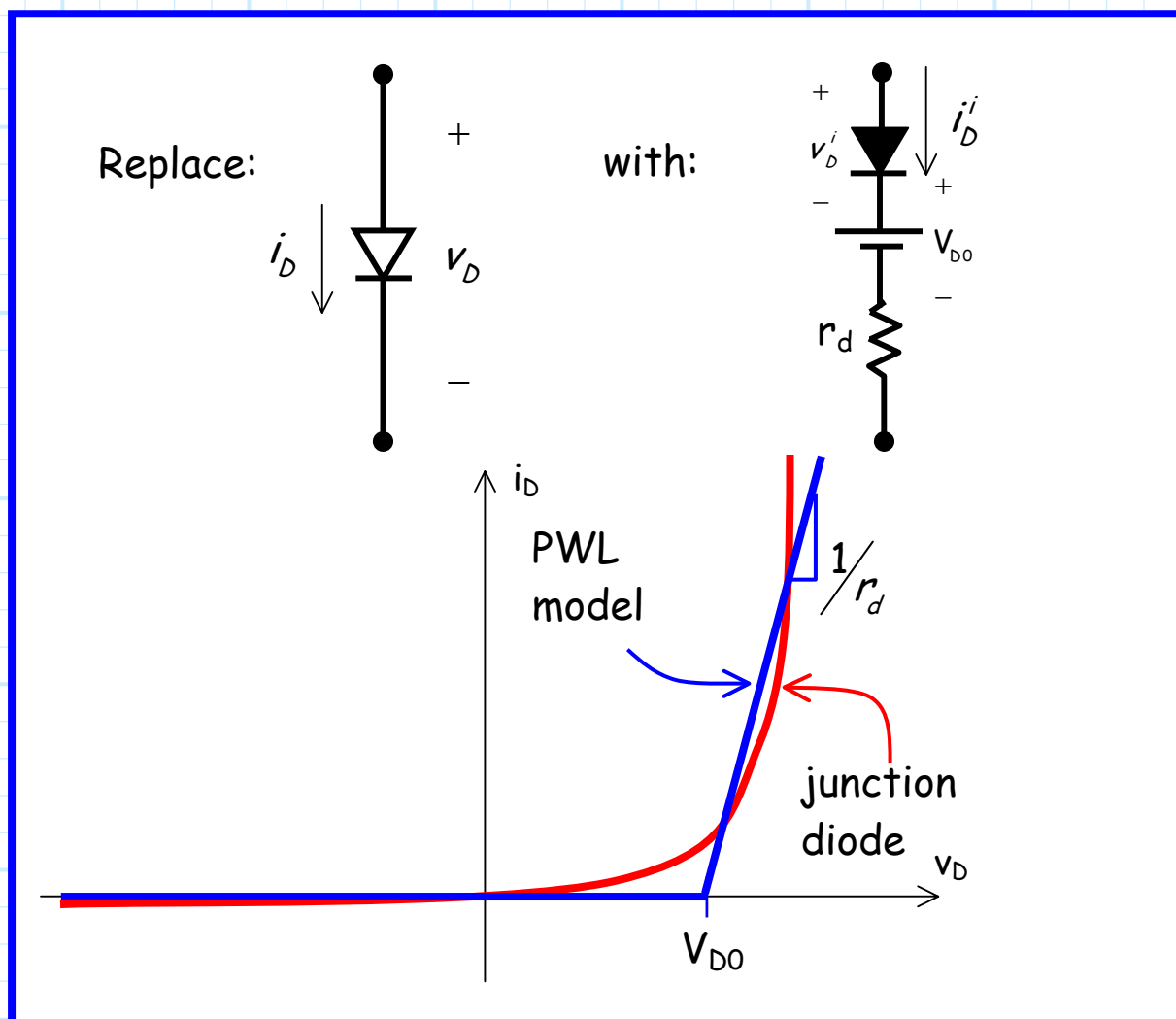
$$\begin{aligned} v_D &= v_D^i + 0.7 \\ &< 0.7 \text{ V} \end{aligned}$$

**NOTE:** Do **not** check the resulting junction diode **approximations**. You do not **assume** anything about the junction diode, so there is **nothing to check** regarding the junction diode answers.

# The Piece-Wise Linear Model

**Q:** *The CVD model approximates the forward biased junction diode voltage as  $v_D = 0.7\text{ V}$  regardless of the junction diode current. This of course is a good approximation, but in reality, the junction diode voltage **increases** (logarithmically) with increasing diode current. Isn't there a more **accurate** model?*

**A:** Yes! Consider the **Piece-Wise Linear (PWL)** model.



In other words, replace the junction diode with **three** devices—an **ideal diode**, in series with some **voltage source** (not 0.7 V!) and a **resistor**.

To find **approximate** current and voltage values of a junction diode circuit, follow these steps:

**Step 1** - Replace each junction diode with the **three** devices of the PWL model.

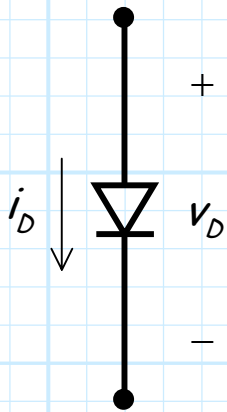
Note you now have an **IDEAL** diode circuit! There are **no junction diodes** in the circuit, and therefore **no junction diode** knowledge need be (or should be) used to analyze it.

**Step 2** - Analyze the **IDEAL** diode circuit. Determine  $i_D^i$  and  $v_D^i$  for each **IDEAL** diode.

**IMPORTANT NOTE !!! PLEASE READ THIS CAREFULLY:**

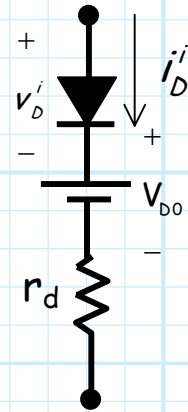
Make sure you analyze the resulting circuit **precisely** as we did in section 3.1. You **assume** the same **IDEAL** diode modes, you **enforce** the same **IDEAL** diode values, and you **check** the same **IDEAL** diode results, **precisely** as before. Once we replace the junction diodes with the CVD model, we have an **IDEAL** diode circuit—**no junction diodes** are involved!

**Step 3** - Determine the **approximate** values  $i_D$  and  $v_D$  of the **junction diode** from the **ideal** diode values  $i_D^i$  and  $v_D^i$ :



$$i_D \approx i_D^i$$

$$v_D \approx v_D^i + V_{D0} + i_D^i r_d$$



Note therefore, if the **IDEAL** diode (note here I said **IDEAL** diode) is **forward** biased ( $i_D^i > 0$ ), then the **approximation** of the **junction** diode current will likewise be positive ( $i_D > 0$ ), and the **approximation** of the **junction** diode voltage (unlike the **ideal** diode voltage of  $v_D^i = 0$ ) will be:

$$\begin{aligned} v_D &= v_D^i + V_{D0} + i_D^i r_d \\ &= 0.0 + V_{D0} + i_D^i r_d \\ &= V_{D0} + i_D^i r_d \end{aligned}$$

However, if the **IDEAL** diode is **reversed** biased ( $i_D^i = 0$ ), then the **approximation** of the **junction** diode current will likewise be zero ( $i_D = 0$ ), and the approximation of the junction diode voltage (unlike the **ideal** diode voltage of  $v_D^i < 0$ ) will be:

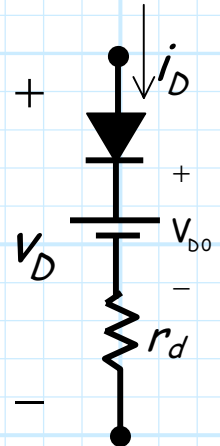
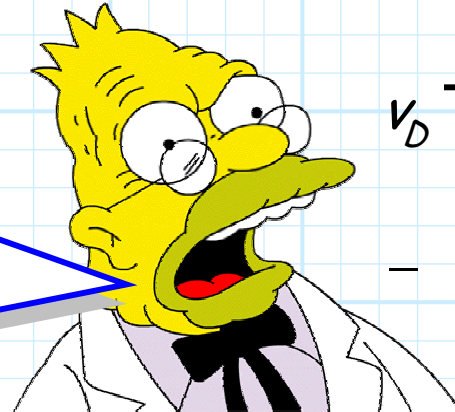
$$\begin{aligned} v_D &= v_D^i + V_{D0} + i_D^i r_d \\ &= v_D^i + V_{D0} + 0 \\ v_D &< V_{D0} \end{aligned}$$

**NOTE:** Do **not** check the resulting junction diode approximations. You do **not** assume anything about the junction diode, so there is **nothing** to check regarding the junction diode answers.



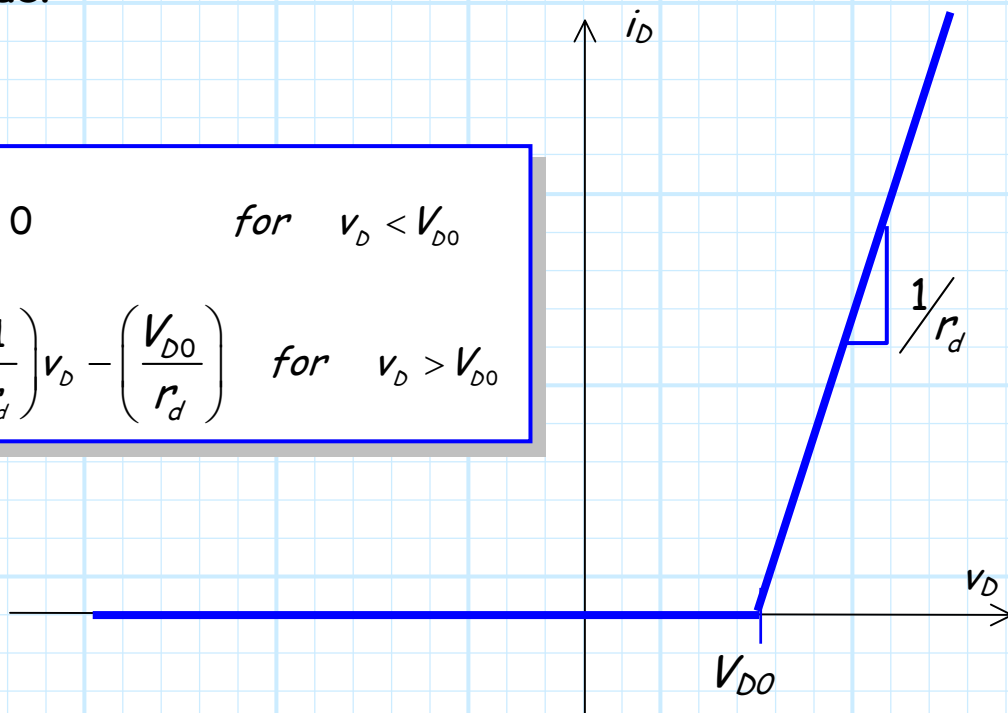
# Constructing the PWL Junction Diode Model

**Q:** Wait a minute! How the heck are we supposed to use the **PWL model** to analyze junction diode circuits? You have yet to tell us the **numeric values** of voltage source  $V_{D0}$  and resistor  $r_d$ !



**A:** That's right! The reason is that the **proper** values of voltage source  $V_{D0}$  and resistor  $r_d$  are up to **you** to determine! To see why, consider the current voltage relationship of the **PWL model**:

$$i_D = \begin{cases} 0 & \text{for } v_D < V_{D0} \\ \left(\frac{1}{r_d}\right)v_D - \left(\frac{V_{D0}}{r_d}\right) & \text{for } v_D > V_{D0} \end{cases}$$



Note that when the **ideal** diode in the PWL model is forward biased, the current-voltage relationship is simply the equation of a **line**!

$$i_D = \left( \frac{1}{r_d} \right) v_D - \left( \frac{V_{D0}}{r_d} \right)$$

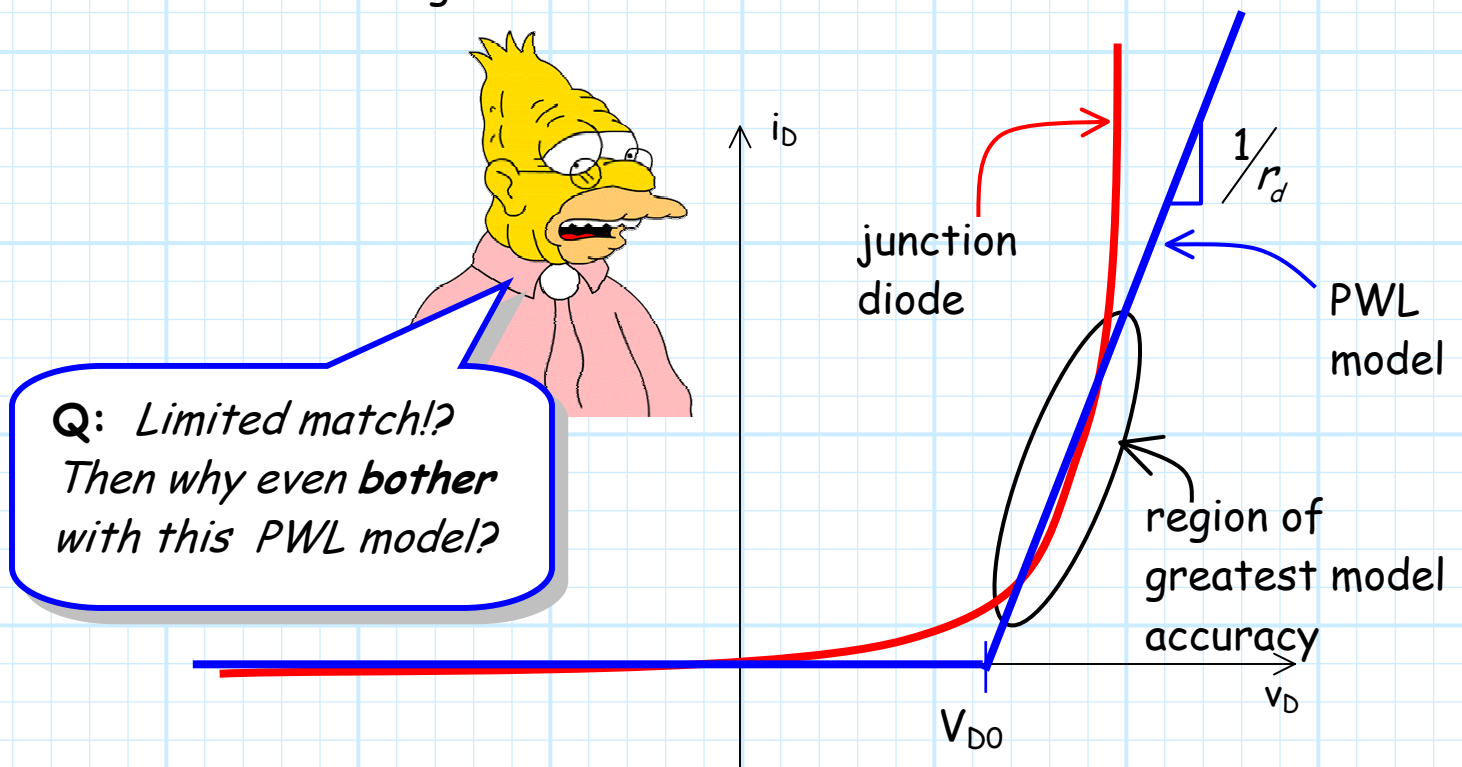
y = m x + b

**Compare** the above to the forward biased junction diode approximation:

$$i_D = I_s e^{v_D/nV_T}$$

An **exponential** equation!

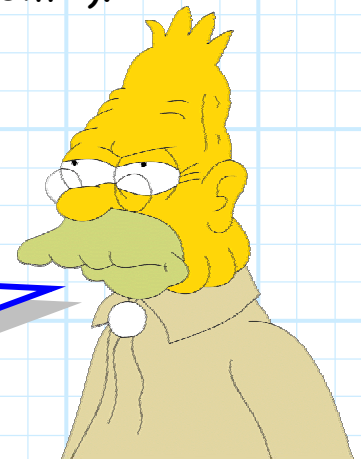
An exponential function and the equation of a line are **very** different—the two functions can approximately “match” only over a **limited** region:



**A:** Remember, the PWL model is **more accurate** than our two **alternatives**—the ideal diode model and the CVD model.

At the very least, the PWL model (**unlike** the two alternatives) shows an **increasing** voltage  $v_D$  with **increasing**  $i_D$ . Moreover, if we select the values of  $V_{D0}$  and  $r_d$  properly, the PWL can **very** accurately “match” the actual (exponential) junction diode curve over a **decade** or more of current (e.g., accurate from  $i_D = 1$  mA to 10 mA, or from  $i_D = 20$  mA to 200 mA).

**Q:** *Yes well I asked you a long time ago what  $r_d$  and  $V_{D0}$  should be, but you **still** have not given me an **answer!***



**A:** OK. We now know that the values of  $r_d$  and  $V_{D0}$  specify a **line**. We also know there are **4** potential ways to **specify** a line:

1. Specify **two points** on the line.
2. Specify one **point** on the line, as well as its **slope  $m$** .
3. Specify one **point** on the line, as well as its  **$y$ -intercept  $b$** .
4. Specify both its **slope** and its  **$y$ -intercept  $b$** .

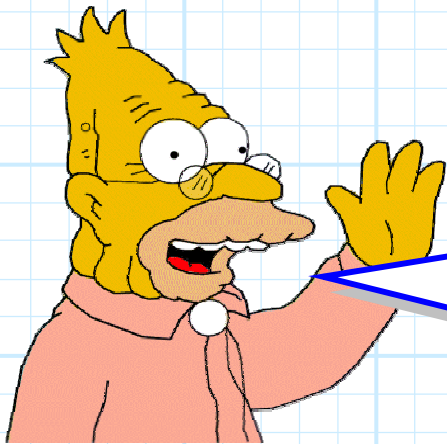
We will find that the **first two** methods are the most useful. Let's address them one at a time.

## 1. Specify two points on the line

The **obvious** question here is: **Which** two points ?

Hopefully it is **equally** obvious that the two points should be points lying on the **junction diode** exponential curve (after all, it is this curve that we are **attempting to approximate!**).

Typically, we pick **two current values** separated by about a **decade** (i.e., 10 times). For **example**, we might select  $i_{D1}=10$  mA and  $i_{D2}=100$  mA. We will find that the resulting PWL model will be **fairly accurate** over this region.



**Q:** *I've got a **question!** How do we find the corresponding **voltage** values  $v_{D1}$  and  $v_{D2}$  for these two currents?*

**A:** Remember, we are selecting two points **on** the exponential junction diode curve. Thus, we can use the **junction diode equation** to determine the corresponding voltages:

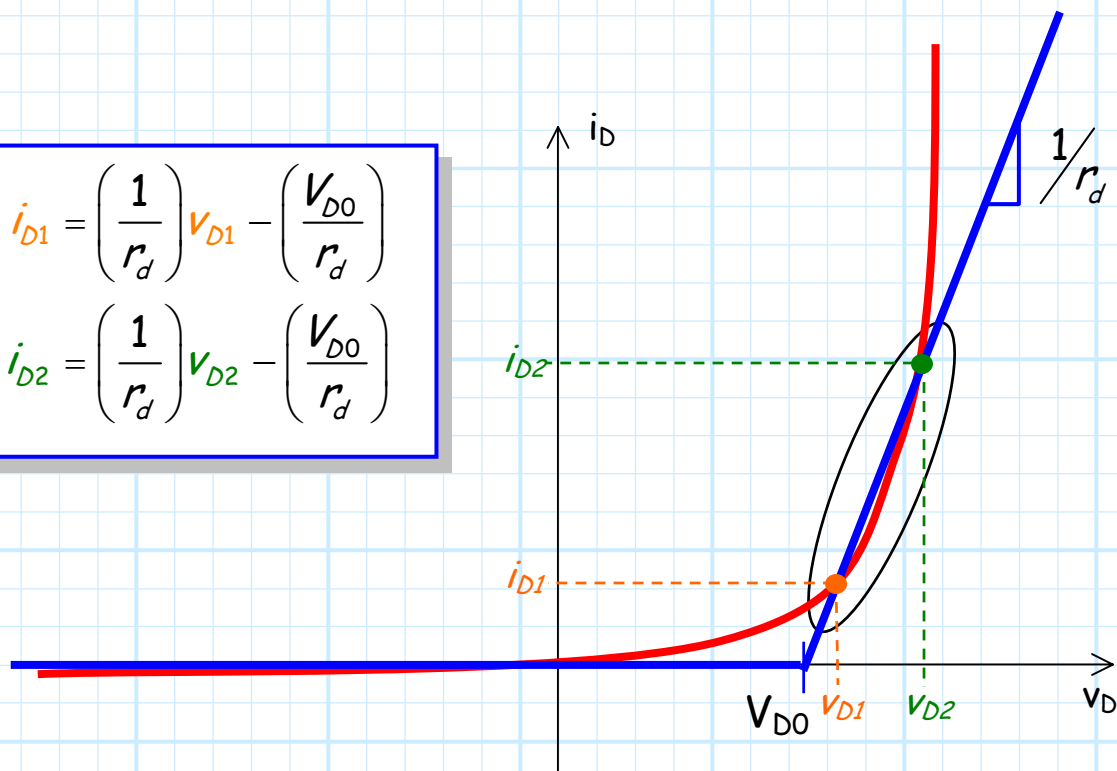
$$v_{D1} = nV_T \ln \left[ \frac{i_{D1}}{I_s} \right]$$

$$v_{D2} = nV_T \ln \left[ \frac{i_{D2}}{I_s} \right]$$

Now, the rest is simply **Middle School mathematics**. If our PWL "line" intersects these two points, then:

$$i_{D1} = \left( \frac{1}{r_d} \right) v_{D1} - \left( \frac{V_{D0}}{r_d} \right)$$

$$i_{D2} = \left( \frac{1}{r_d} \right) v_{D2} - \left( \frac{V_{D0}}{r_d} \right)$$



Thus, we can solve the above **two equations** to determine the **two unknown** values of  $V_{D0}$  and  $r_d$ , such that our PWL "line" will intersect the two specified points on the junction diode curve:

$$m = \frac{1}{r_d} = \frac{i_{D2} - i_{D1}}{v_{D2} - v_{D1}} \quad \therefore \quad r_d = \frac{v_{D2} - v_{D1}}{i_{D2} - i_{D1}}$$

And then we use our PWL "line" equation to find  $r_d$ :

$$V_{D0} = v_{D1} - i_{D1} r_d \quad \text{or} \quad V_{D0} = v_{D2} - i_{D2} r_d$$

(note these two equations are **KVL!**).

## 2. Specify one point and the slope

Now let's examine **another** way of constructing our PWL model. We first specify just **one** point that the PWL "line" must intersect. Let's denote this point as  $(I_D, V_D)$  and call this point our **bias point**.

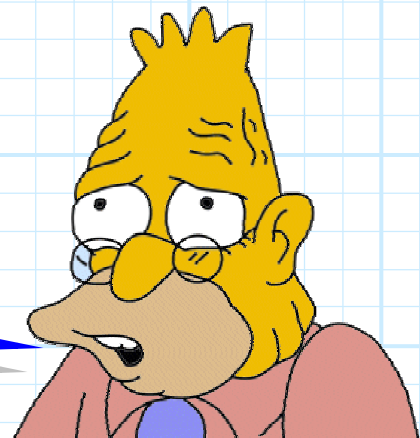
Of course, we want our bias point to **lie on** the exponential junction diode curve, i.e.:

$$I_D = I_s e^{V_D/nV_T} \quad \text{or equivalently} \quad V_D = nV_T \ln \left[ \frac{I_D}{I_s} \right]$$

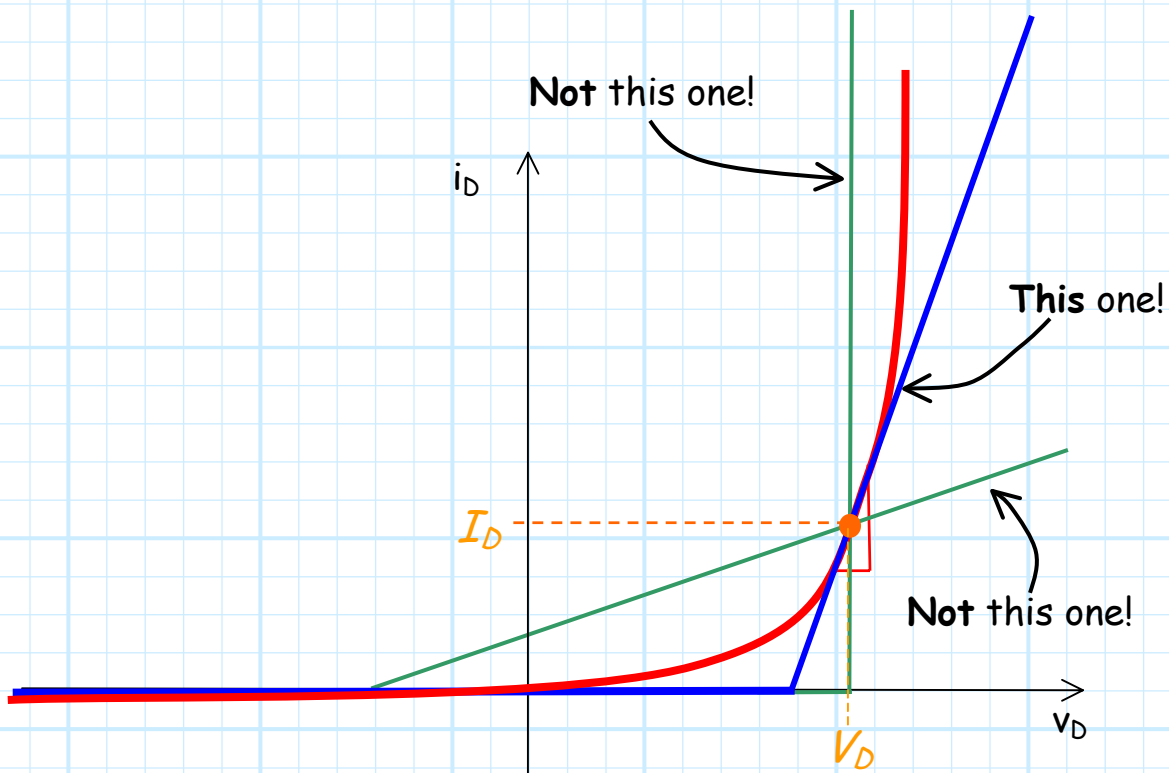
Now, **instead** of specifying a **second** intersection point, we merely **specify directly** the PWL line **slope** (i.e., directly specify the value of  $r_d$ ):

$$m = \frac{1}{r_d}$$

**Q:** *But I have no idea what the value of this slope should be!?!*



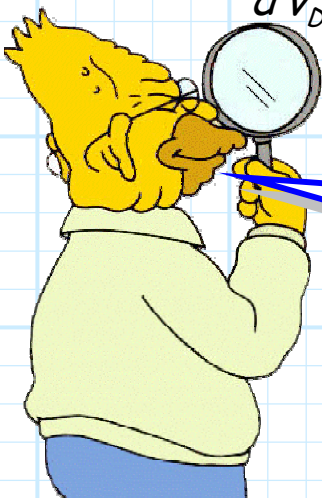
**A:** **Think** about it. Of all possible PWL models that intersect the bias point, the one that is most accurate is the one that has a slope **equal** to the slope of the exponential junction diode curve (that is, **at** the bias point)!



**Q:** *What! Just how is it possible to determine the slope of the junction diode curve at the bias point?!?*

**A:** Easy! We simply take the **first derivative** of the junction diode equation:

$$\begin{aligned} \frac{di_D}{dv_D} &= \frac{d}{dv_D} \left( I_s e^{v_D/nV_T} \right) \\ &= \frac{I_s e^{v_D/nV_T}}{nV_T} \end{aligned}$$



**Q:** *Of course! This equation is the slope of the junction diode curve at the bias point!*



**A:** Actually **no**. The above equation is **not** the slope of the junction diode curve at the bias point. This equation provides the slope of the curve **as a function diode voltage  $v_D$** . The slope of the junction diode curve is in fact different at **every** point on the junction diode curve.

In fact, as the equation above clearly states, the slope of the junction diode curve **exponential increases** with increasing  $v_D$ !

**Q:** *Yikes! So what is the derivate equation good for?*

**A:** Remember, we are interested in the value of the slope of the curve at **one** particular point—the **bias point**. Thus, we simply **evaluate** the derivative function at that point. The result is a numeric value of the slope **at our bias point!**

$$\begin{aligned}
 m &= \frac{d}{dv_D} \left( I_s e^{v_D/nV_T} \right) \Big|_{v_D=V_D} \\
 &= \frac{I_s e^{v_D/nV_T}}{nV_T} \Big|_{v_D=V_D} \\
 &= \frac{I_s e^{V_D/nV_T}}{nV_T}
 \end{aligned}$$

Note the **numerator** of this result! We recognize this numerator as simply the value of the **bias current  $I_D$** :

$$I_D = I_s e^{V_D/nV_T}$$



Therefore, we find that the **slope** at the bias point is:

$$m = \frac{I_s e^{V_D/nV_T}}{nV_T} = \frac{I_D}{nV_T}$$

Now, we want the slope of our **PWL model** line to be **equal** to the slope of the **junction diode curve** at our bias point.

Therefore, we desire:

$$\frac{1}{r_d} = m = \frac{I_D}{nV_T}$$

Thus, **rearranging** this equation, we find that the **PWL model resistor value** should be:

$$r_d = \frac{nV_T}{I_D}$$

We likewise can rearrange the PWL "line" equation to determine the value of the **model voltage source**  $V_{D0}$ :

$$V_{D0} = V_D - I_D r_d \quad (\text{KVL !})$$

Now, combining the previous two equations, we find:

$$\begin{aligned} V_{D0} &= V_D - I_D r_d \\ &= V_D - I_D \left( \frac{nV_T}{I_D} \right) \\ &= V_D - nV_T \end{aligned}$$

So, let's **recap** what we have learned about constructing a PWL model using this particular approach.

1. We first select a single **bias point** ( $I_D$ ,  $V_D$ ), a point that lies on the junction diode curve, i.e.:

$$I_D = I_s e^{V_D/nV_T}$$

2. Using the current and voltage values of this bias point, we can then determine **directly** the PWL model **resistor value**:

$$r_d = \frac{nV_T}{I_D}$$

3. We can also directly determine the **value** of the model **voltage source**:

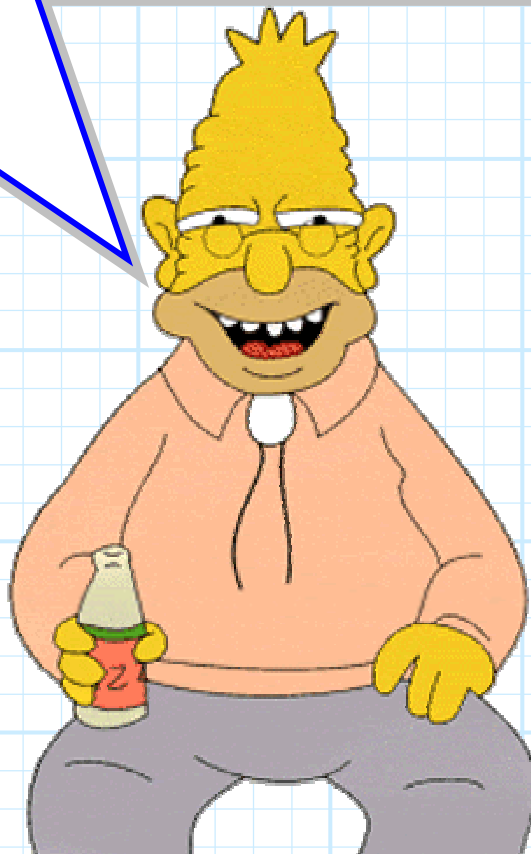
$$V_{D0} = V_D - nV_T$$

*This method for constructing a **PWL model** produces a very **precise** match over a relatively small region of the junction diode curve.*

*We will find that this is **very useful** for many practical diode circuit problems and analysis!*

*This PWL model produced by this last method (as described by the equations of the previous page) is called the junction diode **small-signal model**.*

*We will use the **small-signal model** again—make sure that you know **what** it is and **how** we construct it!*



# Example: Constructing a PWL Model

For a certain junction diode, we **know** that:

$$i_D = 10 \text{ mA} \quad \text{when} \quad v_D = 0.7 \text{ V}$$

and

$$i_D = 1 \text{ mA} \quad \text{when} \quad v_D = 0.6 \text{ V}$$

Say we wish to **construct a PWL model** that will approximate this junction diode behavior for diode currents from, say, approximately 1 mA to approximately 10 mA.

Recall that the resulting model will relate diode voltage  $V_D$  to diode current  $i_D$  as a **line** of the form:

$$i_D = \left( \frac{1}{r_d} \right) v_D - \left( \frac{V_{D0}}{r_d} \right)$$

We therefore need to determine the values of  $V_{D0}$  and  $r_d$  such that this PWL model "line" will **intersect** the two points  $i_{D1}=1$ ,  $v_{D1}=0.6$  and  $i_{D1}=10$ ,  $v_{D1}=0.7$ .

The **slope** of this line must therefore be:

$$m = \frac{i_{D2} - i_{D1}}{v_{D2} - v_{D1}} = \frac{10 - 1}{0.7 - 0.6} = \frac{9}{0.1} = 90 \text{ K mhos}$$

Thus our PWL model **resistor value**  $r_d$  must be:

$$r_d = \frac{1}{m} = \frac{0.1}{9} = 0.0111 \text{ K}\Omega$$

Or in other words,  $r_d = 11.1 \Omega$ .

**Q:** *Wow! That's a **very small** resistance value. Are you **sure** we calculated  $r_d$  correctly?*

**A:** Typically, we find that the resistor value in the PWL model is small. In fact, it is frequently **less than 1  $\Omega$**  when we attempt to match the junction diode curve in a "high" current region (e.g., from  $i_D = 50 \text{ mA}$  to  $i_D = 500 \text{ mA}$ ).

Now that we have determined  $r_d$ , we can insert **either** point into the model **line equation** and solve for  $V_{D0}$ . For example, the equations:

$$i_{D1} = \left( \frac{1}{r_d} \right) v_{D1} - \left( \frac{V_{D0}}{r_d} \right) \quad \text{or} \quad i_{D2} = \left( \frac{1}{r_d} \right) v_{D2} - \left( \frac{V_{D0}}{r_d} \right)$$

become either:

$$\begin{aligned} V_{D0} &= v_{D1} - i_{D1} r_d \\ &= 0.6 - 1(0.0111) \\ &= 0.589 \text{ V} \end{aligned}$$

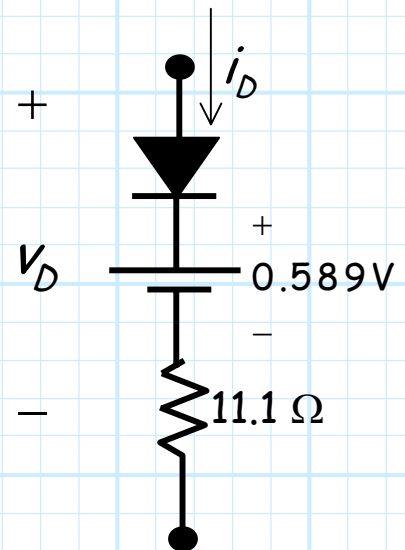
or

$$\begin{aligned} V_{D0} &= v_{D2} - i_{D2} r_d \\ &= 0.7 - 10(0.0111) \\ &= 0.589 \text{ V} \end{aligned}$$

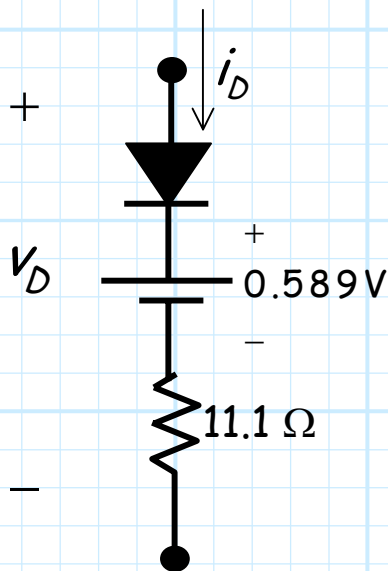
In other words, we can use **either** point to determine  $V_{D0}$ .

Our PWL model is therefore:

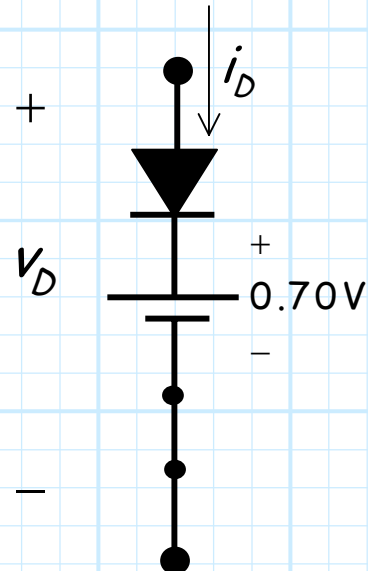
$$i_D = \begin{cases} 0 & \text{for } v_D < 0.589 \text{ V} \\ \frac{v_D}{0.0111} - \frac{0.589}{0.0111} \text{ mA} & \text{for } v_D > 0.589 \text{ V} \end{cases}$$



Now, **compare** this PWL model to the CVD model:



PWL



CVD

Note that the CVD model can be viewed as a PWL model with  $V_{D0} = 0.7 \text{ V}$  and  $r_d = 0.0$ . **Compare** those values with our model ( $V_{D0} = 0.589 \text{ V}$  and  $r_d = 11.1 \Omega$ )—**not** much difference!

Thus, the PWL model is **not** a radical departure from the CVD model (typically  $V_{D0}$  is close to  $0.7 \text{ V}$  and  $r_d$  is **very** small). Instead the PWL can be view as **slight improvement** of the CVD model.

# Example: Constructing a Diode Small-Signal Model

Recall that one method for constructing a diode PWL model is to specify a single point (i.e., the **bias point**) on the junction diode curve, and then determine the **slope** of the junction diode curve at that point.

We can then select our **PWL model parameters**  $r_d$  and  $V_{D0}$  such that the PWL model "line" will **intersect** the specified bias point, and so that the slope of the line will **match** that of the junction diode curve at the bias point.

We call this model the **small-signal PWL diode model**!

For **example**, say a junction diode with  $n=1$  pulls a diode current of  $i_D = 10 \text{ mA}$  at a diode voltage of  $v_D = 0.6 \text{ V}$ .

→ Let's build a **small-signal PWL model** for this diode!

First, we need to **select a bias point** ( $I_D, V_D$ ). Recall that this can be any point on the **junction diode curve**.



Q: *But which point do we select? How can we decide?*



**A:** Remember, a PWL model (with a **linear**  $i_D, v_D$  relationship) can only “match” the junction diode curve (with an **exponential**  $i_D, v_D$  relationship) over a relatively small region. Thus, we want our PWL model to accurately “match” the junction diode curve over the region where the **correct** junction diode solution  $i_D, v_D$  actually lies.



**Q:** *Whoa! How can we do that? We are constructing the PWL model so that we can accurately estimate the **unknown** junction diode values  $i_D, v_D$ . But now you say that we must first **know** the solution in order to construct a useful PWL model!*

**A:** It is of course **true** that if we already know the **exact** value of junction diode  $i_D$  and  $v_D$ , we might as well **stop working**—we already have the final answer!

However, we do **not** require the **exact** junction diode solution in order to construct a useful PWL model. Rather, we need only to have **approximate** knowledge (i.e., a “rough idea”).

Often, we can do a **quick analysis** of a circuit to get a rough idea of the diode current. For example, we can use the **ideal diode model** (or the **CVD model**) to determine an **approximate** value for  $i_D$ .

You can then use this approximate **current** value to **select your bias point** (on the junction diode curve). Now you can construct an accurate small-signal PWL diode model!

OK, now back to our **example**. Say that **somehow** we know that the actual junction diode current in our circuit is in the **vicinity** of 10 mA. Let's therefore use as our bias point the values that we were **initially** given—values that describe a point lying on the **junction diode curve**:

$$I_D = 10 \text{ mA} \quad V_D = 0.6 \text{ V}$$

Note that this was the **hardest** part of the whole process! Determining the model parameters is now **straightforward**.

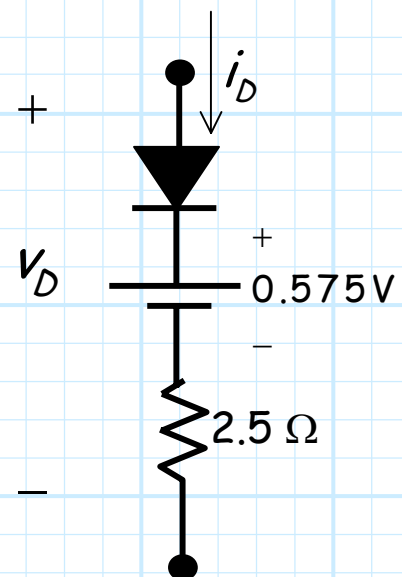
Using the results of a previous handout, we find:

$$r_d = \frac{nV_T}{I_D} = \frac{1(0.025)}{10} = 0.0025 \text{ K} = 2.5 \Omega$$

and

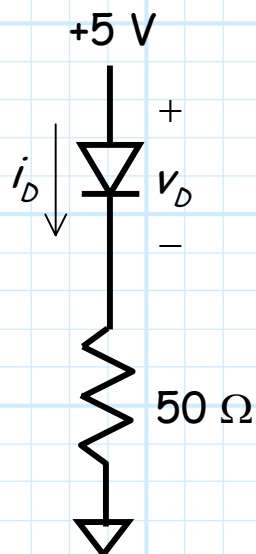
$$\begin{aligned} V_{D0} &= V_D - nV_T \\ &= 0.6 - 0.025 \\ &= 0.575 \text{ V} \end{aligned}$$

We're done!



# Example: Junction Diode Models

Consider the **junction** diode circuit, where the junction diode has device parameters  $I_S = 10^{-12}$  A, and  $n = 1$ :



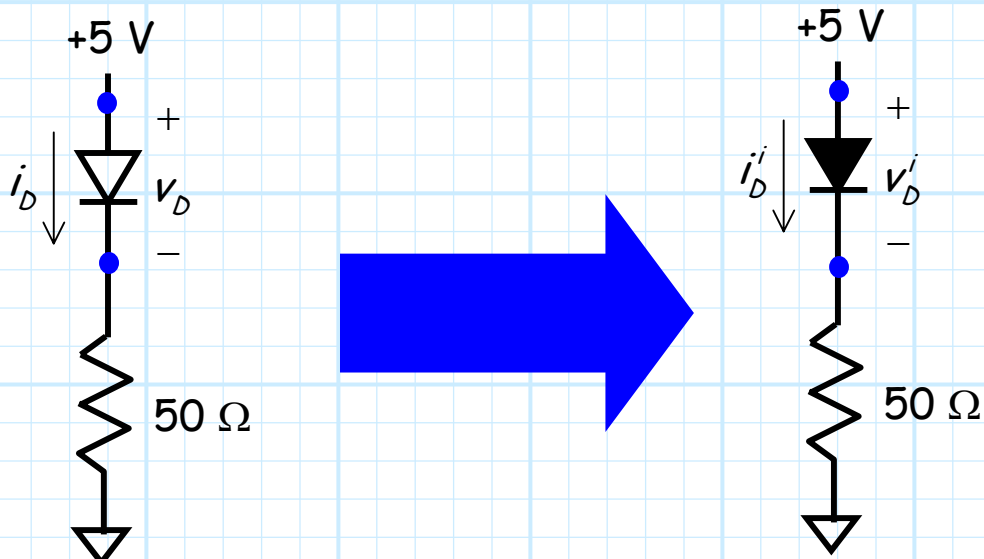
I **numerically** solved the resulting transcendental equation, and determined the **exact** solution:

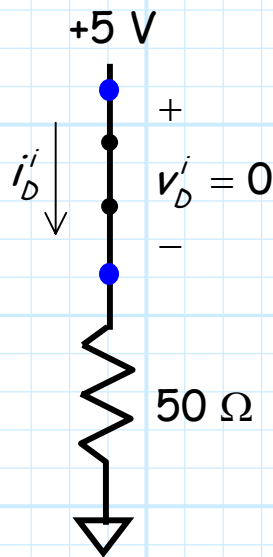
$$i_D = 87.40\ \text{mA}$$

$$v_D = 0.630\ \text{V}$$

Now, let's determine **approximate** values using diode **models** !

First, let's try the **ideal diode model**.





Assume **IDEAL** diode is "on".

Enforce  $v_D^i = 0$ .

Analyze the **IDEAL** diode circuit:

Check result:

We therefore can **approximate** the **junction diode** current as the current through the ideal diode **model**:

$$i_D \approx i_D^i = 100 \text{ mA}$$

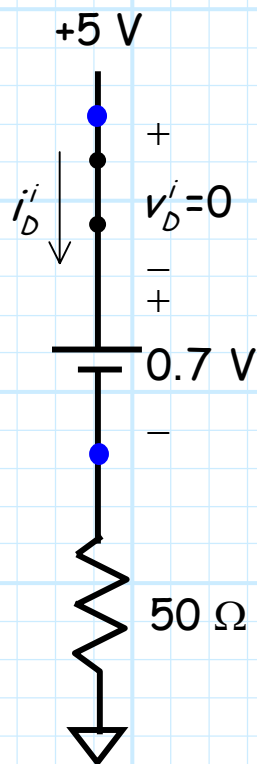
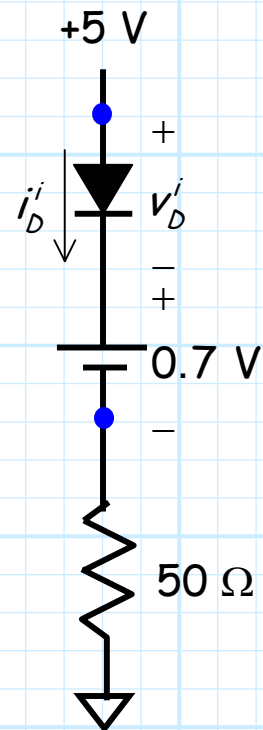
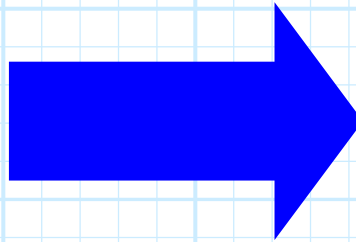
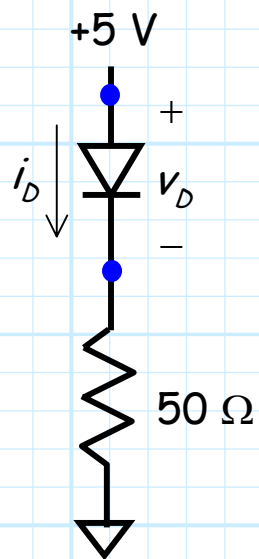
And **approximate** the **junction** diode voltage as the voltage across the ideal diode **model**:

$$v_D \approx v_D^i = 0$$

Compare these approximations to the **exact** solutions:

$$i_D = 87.4 \text{ mA and } v_D = 0.630 \text{ V}$$

Close, but we can do better! Let's use the **CVD** model.



Assume **IDEAL** diode is "on".

Enforce  $v_D^i = 0$ .

Analyze the **IDEAL** diode circuit:

Check the result:

We therefore can **approximate** the **junction diode current** as the current through the **CVD model**:

$$i_D \approx i_D^i = 86 \text{ mA}$$

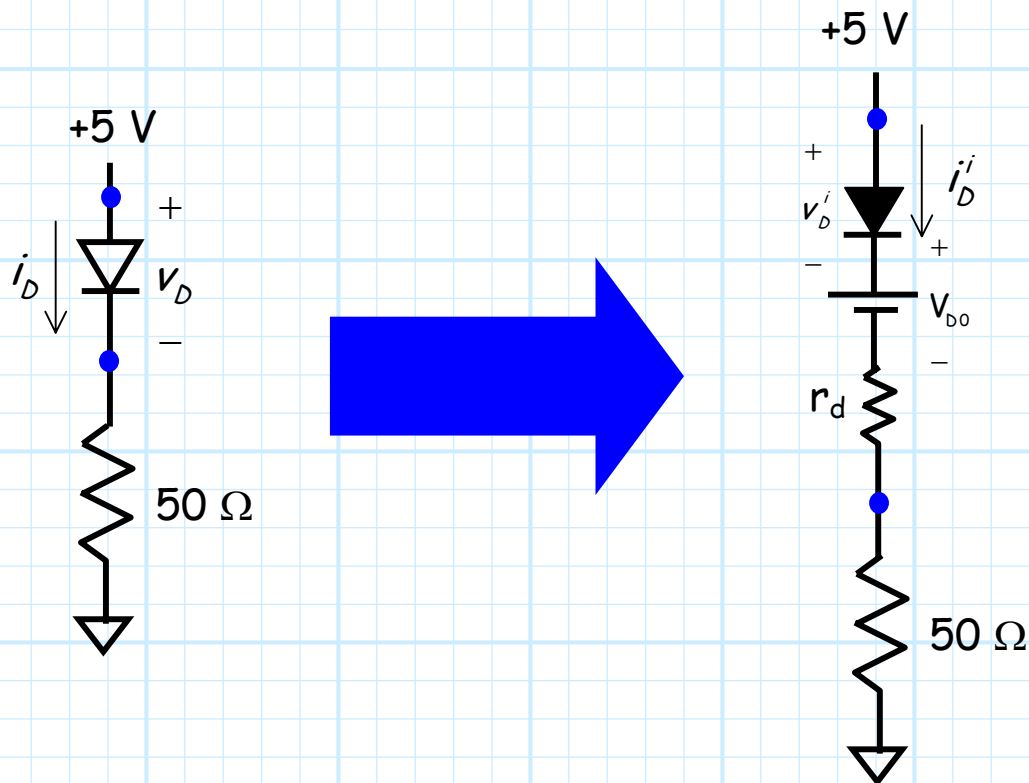
And **approximate** the **junction diode voltage** as the voltage across the **CVD model**:

$$\begin{aligned} v_D &\approx v_D^i + 0.7 \\ &= 0 + 0.7 \\ &= 0.7 \text{ V} \end{aligned}$$

Compare these approximations to the **exact** solutions:

$$i_D = 87.4 \text{ mA} \quad \text{and} \quad v_D = 0.630 \text{ V}$$

**Much better** than before, but we can do even better! Let's use the **PWL model**.



**Q:** *But, what values should we use for model parameters  $V_{D0}$  and  $r_d$ ??*

**A:** From the CVD model, we know that  $i_D$  is approximately 86mA. Therefore, let's create a **PWL model** that is accurate in the region between, say,  $50 \text{ mA} < i_D < 125 \text{ mA}$ .

**First**, we determine  $v_D$  at 50 mA and 125 mA.

$$\begin{aligned} v_D &= nV_T \ln(i_D / I_S) \\ &= 0.616 \text{ V} \quad \text{for } 50 \text{ mA} \\ &= 0.639 \text{ V} \quad \text{for } 125 \text{ mA} \end{aligned}$$

We now know two points lying on the junction diode curve! Let's construct a PWL model whose "line" intersects these two points.

Recall that when the ideal diode is forward biased, applying KVL to the PWL model results in:

$$v_D = V_{D0} + i_D r_d$$

or equivalently:

$$i_D = \frac{v_D}{r_d} - \frac{V_{D0}}{r_d}$$

Inserting the junction diode values into this PWL model equation provides:

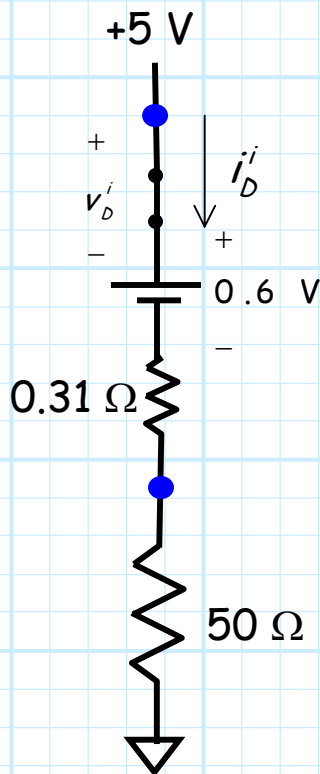
$$0.616 = V_{D0} + (0.05)r_d$$

$$0.639 = V_{D0} + (0.125)r_d$$

Two equations and two unknowns !! Solving, we get:

$$V_{D0} = 0.600 \text{ V and } r_d = 0.31 \Omega \text{ (small !!)}$$

Therefore, the ideal diode circuit is:



Assume the **IDEAL** diode is "on".

Enforce  $v_D^i = 0$ .

Analyze the **IDEAL** diode circuit:

Check the result:



We can therefore **approximate** the **junction** diode current as the current through the PWL model:

$$i_D \approx i_D^i = 87.5 \text{ mA}$$

and **approximate** the **junction** diode voltage as the voltage across the PWL model:

$$\begin{aligned} v_D &= v_D^i + V_{D0} + i_D^i r_D \\ &= 0 + 0.600 + (0.087)0.31 \\ &= 0.627 \text{ V} \end{aligned}$$

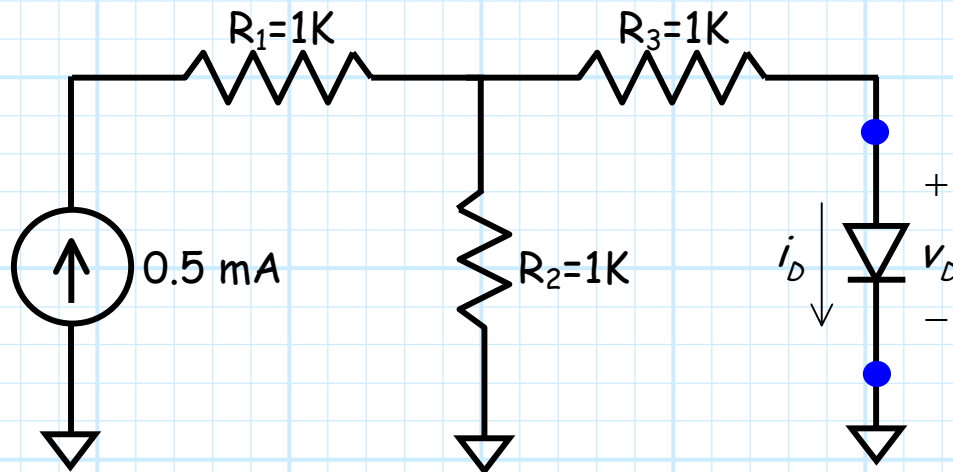
Now, compare these values to the **exact** values  $v_D = 0.630 \text{ V}$  and  $i_D = 87.4 \text{ mA}$ .

The **error** of the PWL model estimates is just 0.003 Volts and 0.1 mA !

Each model provides **better** estimates than the previous one!

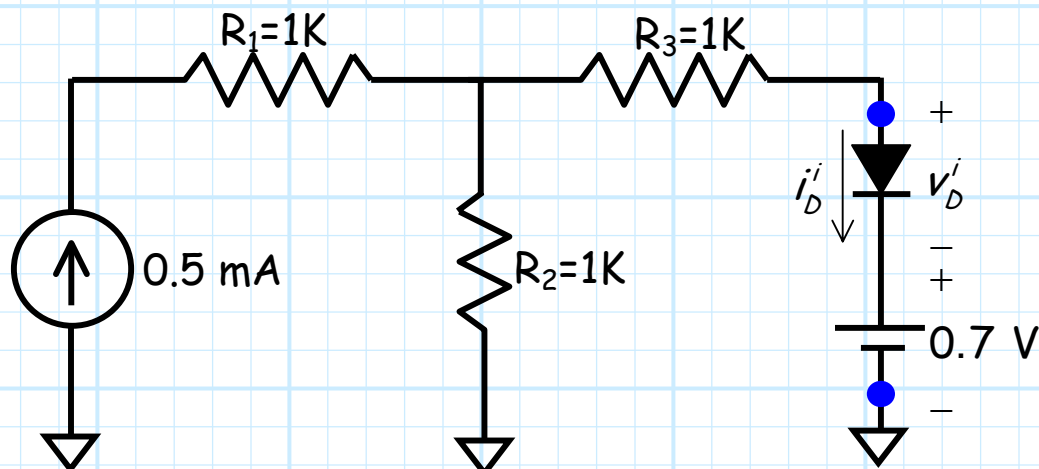
# Example: Another Junction Diode Model Example

Consider now this circuit:



Using the **CVD model**, let's estimate the **voltage** across, and **current** through, the **junction diode**.

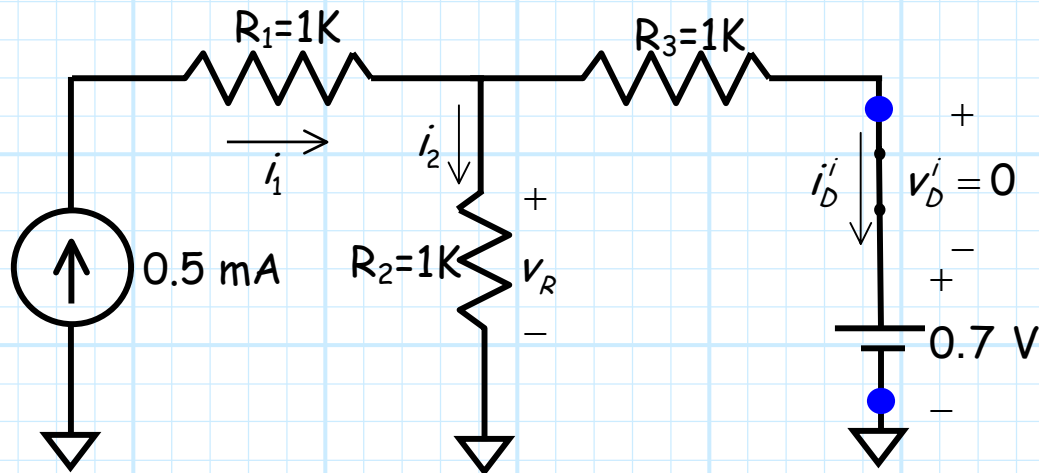
First, replace the junction diode with the **CVD model**:



Now we have an **IDEAL** diode circuit, and therefore we analyze it **precisely** as we did in section 3.1 !!

**ASSUME** the **IDEAL** diode is forward biased (why not ?).

**ENFORCE** the condition that  $v_D^i = 0.0 \text{ V}$  (a **short** circuit).



**ANALYZE** the IDEAL diode circuit:

From KCL  $\rightarrow i_1 = i_2 + i_D^i$

Where  $\rightarrow i_1 = 0.5 \text{ mA}$

$$i_2 = \frac{V_R}{R_2} = \frac{V_R}{1} = V_R$$

$$i_D^i = \frac{V_R - 0.7}{R_3} = \frac{V_R - 0.7}{1} = V_R - 0.7$$

Therefore  $\rightarrow 0.5 = V_R + (V_R - 0.7) = 2V_R - 0.7$

And thus: 
$$V_R = \frac{0.5 + 0.7}{2} = 0.6 \text{ V}$$

So that: 
$$i_D^i = V_R - 0.7 = 0.6 - 0.7 = -0.1 \text{ mA}$$

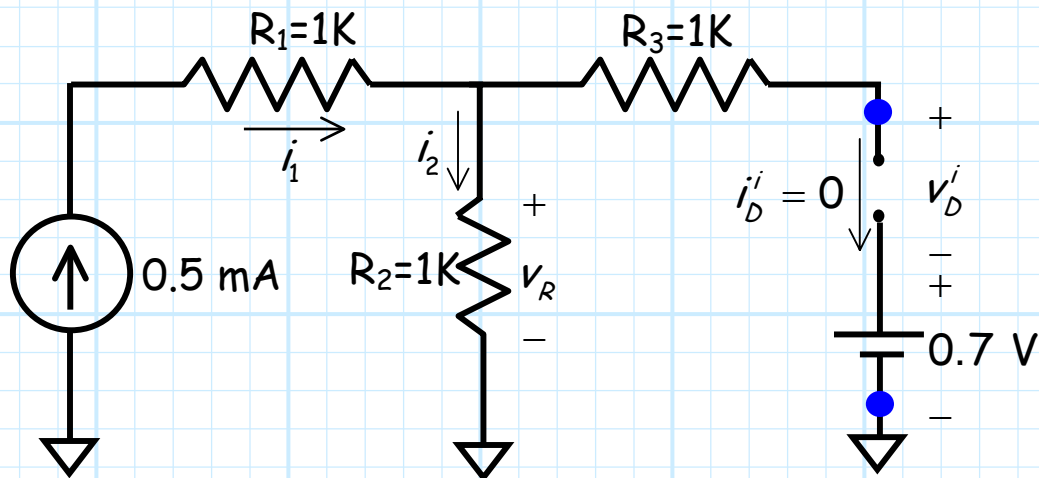
**CHECK** the **IDEAL** diode assumption:

$$i_D^i = -0.1 \text{ mA} < 0 \quad \times$$

Yikes! We made the **wrong** assumption! Let's change our assumption and try again.

**ASSUME** the **IDEAL** diode is **reverse** biased.

**ENFORCE** the condition that  $i_D^i = 0.0 \text{ mA}$  (an **open** circuit).



**ANALYZE** the **IDEAL** diode circuit:

From KCL  $\rightarrow$  
$$i_1 = i_2 + i_D^i$$

Where  $\rightarrow i_1 = 0.5 \text{ mA}$

$$i_2 = \frac{V_R}{R_2} = \frac{V_R}{1} = V_R$$

$$i_D^i = 0$$

Therefore  $\rightarrow 0.5 = V_R + 0 = V_R$

Note that we must find the numeric value of  $v_D^i$ , the **voltage** across the reverse biased **IDEAL** diode.

From KVL:  $V_R - R_3 i_D^i - v_D^i - 0.7 = 0$

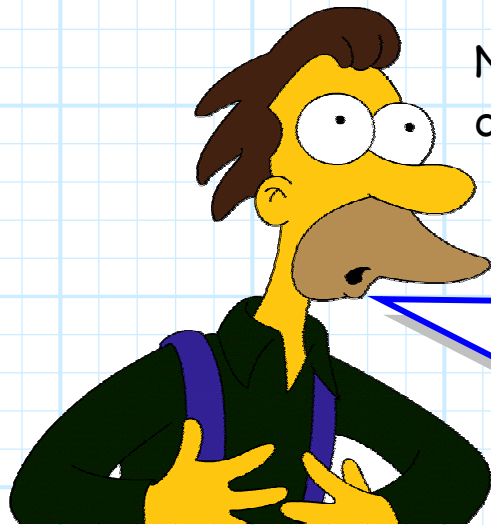
And since  $i_D^i = 0$ , we find that:

$$\begin{aligned} v_D^i &= V_R - R_3 i_D^i - 0.7 \\ &= V_R - 0.7 \\ &= 0.5 - 0.7 \\ &= -0.2 \text{ V} \end{aligned}$$

**CHECK** the **IDEAL** diode assumption:

$$v_D^i = -0.2 \text{ V} < 0 \quad \checkmark$$

Our assumption was **correct!**



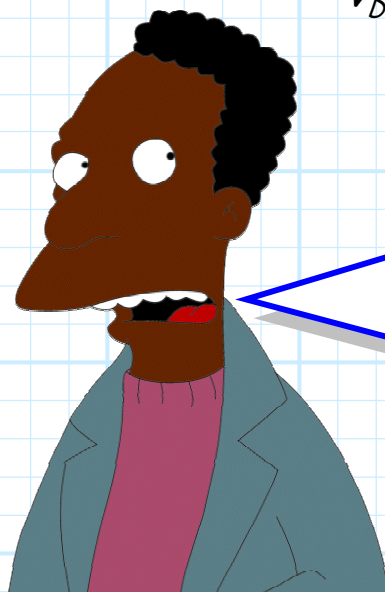
Now, we must estimate the **junction diode current** and **voltage**!

*Q: What do you mean? I thought we just did that! The diode current is  $i_D=0.0$  and the diode voltage is  $v_D=-0.2$  V. Right?*

**A: NO!** We have determined the current and voltage of the **IDEAL** diode voltage in our CVD model. These are **not** the estimated values of the **junction** diode in our circuit!

Instead, we estimate the **junction** diode voltage by calculating the voltage across the **entire CVD model** (i.e., ideal diode and 0.7 V source):

$$\begin{aligned} v_D &= v_D' + 0.7 \\ &= -0.2 + 0.7 \\ &= 0.5 \text{ V} \end{aligned}$$



*What an interesting result! Although the **IDEAL** diode in the CVD model is **reversed** biased, our **junction** diode voltage estimate is **positive**  $v_D=0.5$  V !!!*

We likewise estimate the **current** through the junction diode by determining the current through the **PWL model** (OK, the current through the model is **also** the current through the **ideal diode**):

$$i_d = i_d^i = 0$$

# DC and Small-Signal Components

Note that we have used **DC** sources in all of our example circuits thus far. We have done this just to **simplify** the analysis—generally speaking, realistic (i.e., useful) junction diode circuits will have sources that are **time-varying!**

The result will be voltages and currents in the circuit that will **likewise vary with time** (e.g.,  $i(t)$  and  $v(t)$ ). For example, we can express the forward bias junction diode equation as:

$$i_D(t) = I_S e^{v_D(t)/nV_T}$$

Although source voltages  $v_S(t)$  or currents  $i_S(t)$  can be **any** general function of time, we will find that often, in realistic and useful electronic circuits, that the source can be decomposed into **two** separate components—the **DC component**  $V_S$ , and the **small-signal component**  $v_s(t)$ . I.E.:

$$v_S(t) = V_S + v_s(t)$$



Let's look at each of these components individually:

\* The **DC component**  $V_S$  is exactly what you would expect—the DC component of source  $v_S(t)$ ! Note this DC value is **not** a function of time (otherwise it would not be DC!) and therefore is expressed as a **constant** ( e.g.,  $V_S = 12.3V$  ).

Mathematically, this value is the **time-averaged** value of  $v_S(t)$ :

$$V_S = \frac{1}{T} \int_0^T v_S(t) dt$$

where  $T$  is the **time duration** of function  $v_S(t)$ .

\* As the notation indicates, the **small-signal component**  $v_s(t)$  is a function of time! Moreover, we can see that this signal is an **AC signal**, that is, its time-averaged value is **zero**! I.E.:

$$\frac{1}{T} \int_0^T v_s(t) dt = 0$$

This signal  $v_s(t)$  is also referred to as the **small-signal component**.

\* The **total** signal  $v_S(t)$  is the **sum** of the DC and small signal components. Therefore, it is **neither** a DC nor an AC signal!

Pay attention to the **notation** we have used here. We will use this notation for the remainder of the course!

- \* **DC values** are denoted as **upper-case** variables (e.g.,  $V_S$ ,  $I_R$ , or  $V_D$ ).
- \* **Time-varying signals** are denoted as **lower-case** variables (e.g.,  $v_S(t)$ ,  $v_r(t)$ ,  $i_D(t)$ ).
- \* **AC signals** (i.e., zero time average) are denoted with **lower-case subscripts** (e.g.,  $v_s(t)$ ,  $v_d(t)$ ,  $i_r(t)$ ).
- \* Signals that are **not AC** (i.e., they have a non-zero DC component!) are denoted with **upper-case subscripts** (e.g.,  $V_S(t)$ ,  $V_D(t)$ ,  $I_R(t)$ ,  $V_D$ ).

Note we should **never** use variables of the form  $V_i$ ,  $I_e$ ,  $V_b$ . Do you see why??

**Q:** *You say that we will often find sources with **both** components—a DC and small-signal component. **Why** is that? What is the significance or physical reason for each component?*



**A1:** First, the DC component is typically just a DC **bias**. It is a **known** value, selected and determined by the design engineer. It carries or relates **no** information—the only reason it exists is to make the electronic devices work the way we want!

**A2:** Conversely, the small signal component is typically **unknown!** It is the signal that we are often attempting to **process** in some manner (e.g., amplify, filter, integrate). The signal itself represents **information** such as audio, video, or data.

Sometimes, however, this small, AC, unknown signal represents not information—but **noise!** Noise is a **random**, unknown signal that in fact masks and **corrupts** information. Our job as designers is to **suppress** it, or otherwise minimize its deleterious effects.

- \* This noise may be changing **very rapidly** with time (e.g., MHz), or may be changing **very slowly** (e.g., mHz).
- \* Rapidly changing noise is generally “**thermal noise**”, whereas slowly varying noise is typically due to slowly varying environmental conditions, such as **temperature**.

Note that in addition to (or perhaps because of) the source voltage  $v_s(t)$  having both a DC bias and small-signal component, **all the currents and voltages** (e.g.,  $i_R(t)$ ,  $v_D(t)$ ) within our circuits will likewise have **both** a DC bias and small-signal component!

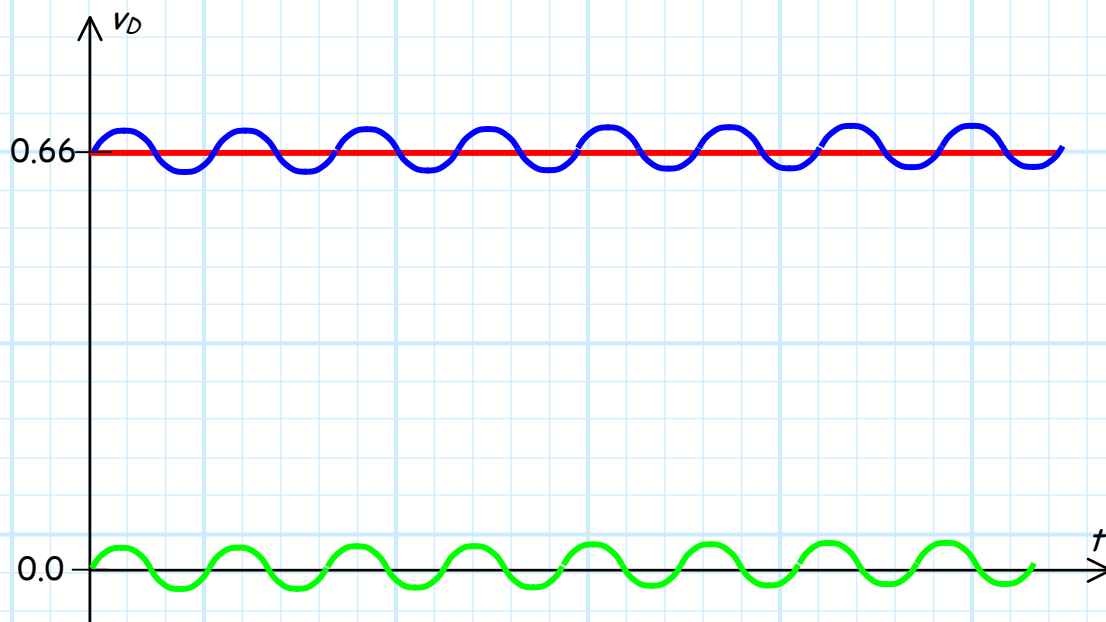
For example, the junction **diode voltage** might have the form:

$$v_D(t) = 0.66 + 0.001 \cos \omega t$$

It is hopefully evident that:

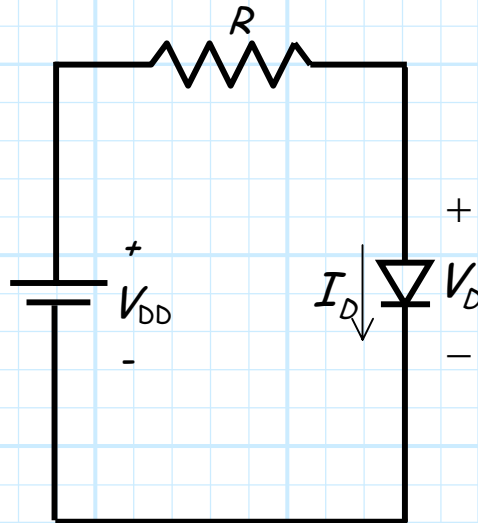
$$V_D = 0.66 \text{ V}$$

$$v_d(t) = 0.001 \cos \omega t$$



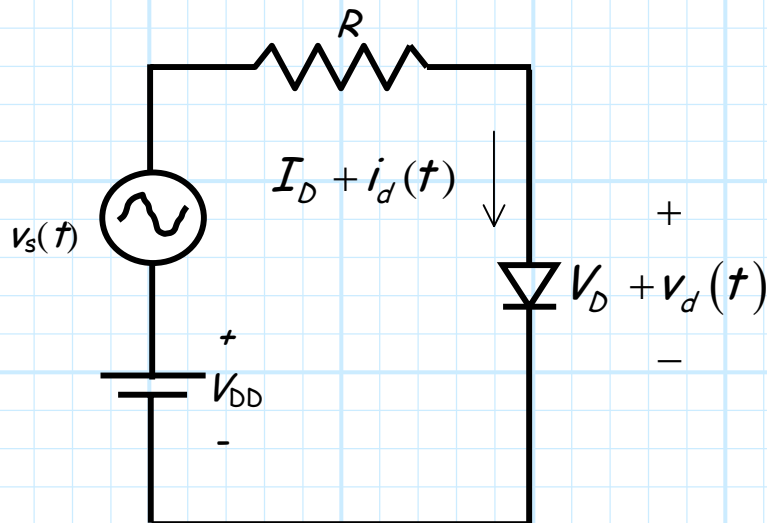
# Small-Signal Analysis

Consider this simple junction diode circuit:



The DC voltage source ( $V_{DD}$ ) results in a DC current ( $I_D$ ), as well as a DC voltage across the junction diode  $V_D$ .

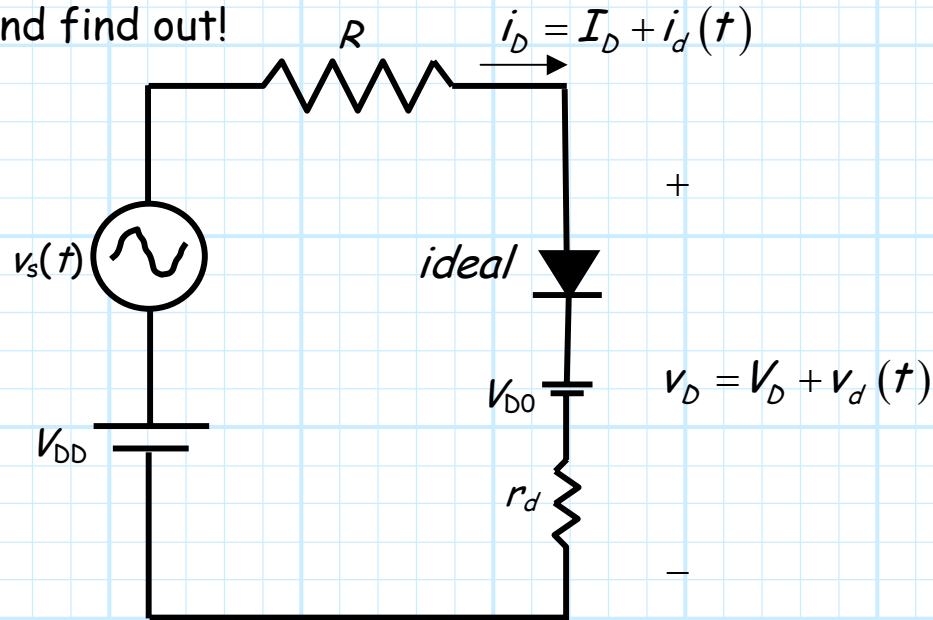
Now let's add an AC (e.g., small-signal) source ( $v_d$ ) to the circuit:



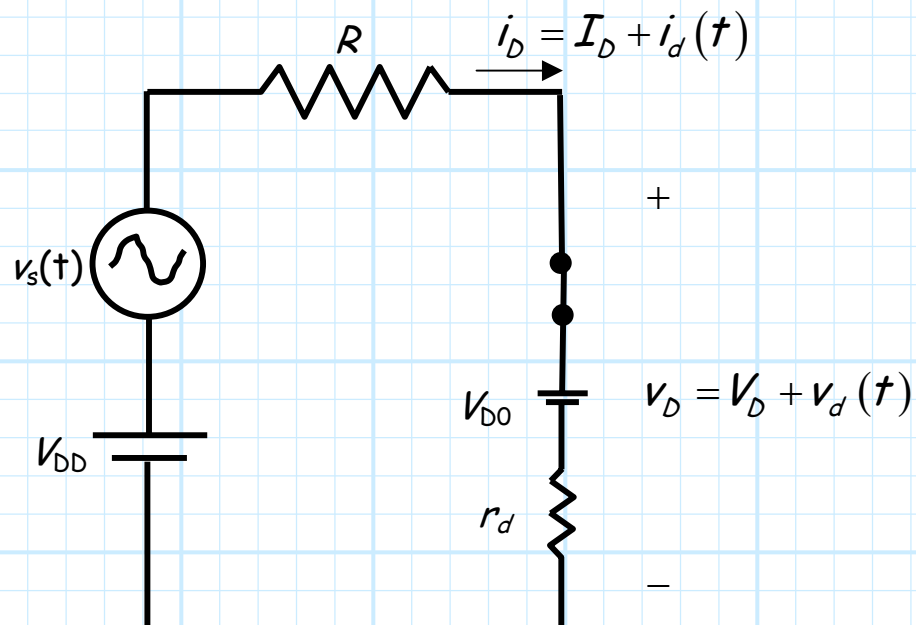
Note that this results in an **additional AC** (small-signal) component for the junction diode current and voltage.

**Q:** What are the DC and small-signal components of the diode current and voltage, and how are they related to the DC ( $V_{DD}$ ) and small-signal ( $v_s$ ) voltage sources?

**A:** Let's replace the junction diode with a small-signal PWL model and find out!



If the DC voltage source is sufficiently large (e.g.,  $V_{DD} \gg V_{D0}$ ), we will find that the ideal diode is **forward biased** ( $v_D^i = 0$ ):



Now, let's apply **KVL** and analyze the circuit!

First, we'll consider the case where the **small-signal voltage source is zero** ( $v_s(t) = 0$ ). In this case, the remaining **DC sources** ( $V_{DD}$  and  $V_{D0}$ ) produce a DC voltage and current ( $V_D$  and  $I_D$ ).

These DC values are related from KVL as:

$$V_{DD} = I_D(R + r_d) + V_{D0}$$

We call this the **DC circuit equation**.

Now let's "**turn on**" the small-signal source, so that  $v_s(t) \neq 0$ . Now we have, in **addition** to the DC currents and voltages, **small-signal components**  $i_d$  and  $v_d$  as well!

Again using **KVL**, we find that the DC and small-signal components are related as:

$$\begin{aligned} V_{DD} + v_s &= (I_D + i_d)R + V_{D0} + (I_D + i_d)r_d \\ &= (R + r_d)I_D + V_{D0} + (R + r_d)i_d \end{aligned}$$

Now, just for fun, let's **subtract** the **DC equation** from this KVL:

$$\begin{aligned} v_s + V_{DD} &= (R + r_d)I_D + V_{D0} + (R + r_d)i_d \\ -V_{DD} &= -(R + r_d)I_D - V_{D0} \end{aligned}$$

---


$$v_s = (R + r_d)i_d$$

The resulting equation:

$$v_s(t) = (R + r_d)i_d(t)$$

is known as the AC, or **small-signal circuit equation**.

Thus, the **total KVL** can be divided into two parts, the **DC equation** and the **small-signal equation**, i.e.:

$$V_{DD} + v_s = (R + r_d)I_D + V_{D0} + (R + r_d)i_d$$

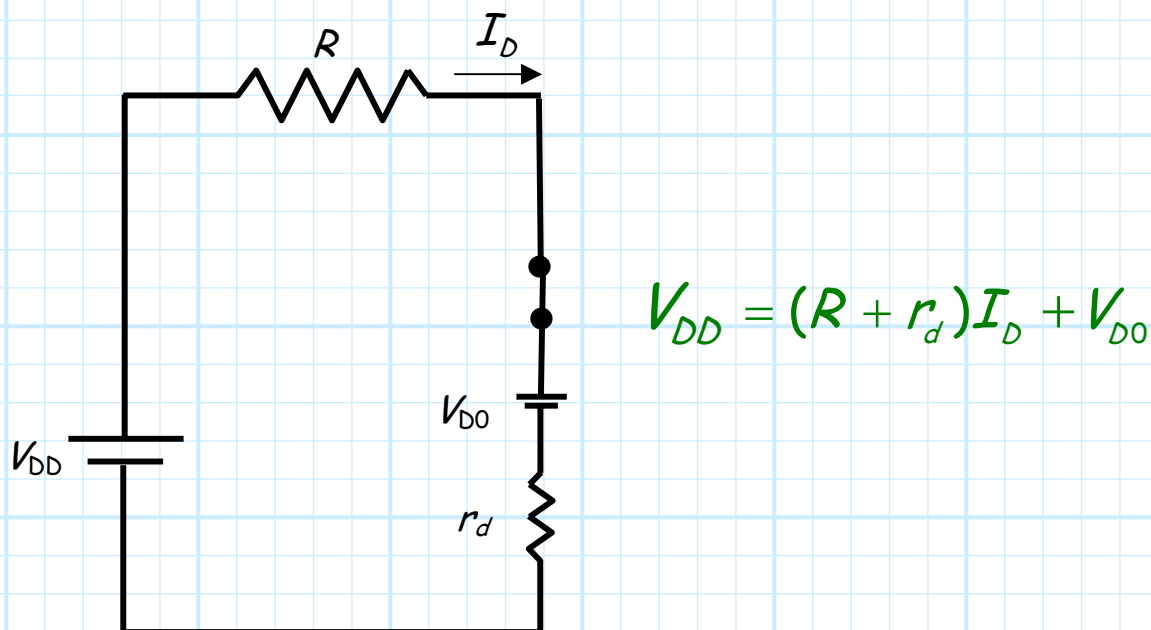
where the **DC equation** is:

$$V_{DD} = (R + r_d)I_D + V_{D0}$$

and the **small-signal equation** is:

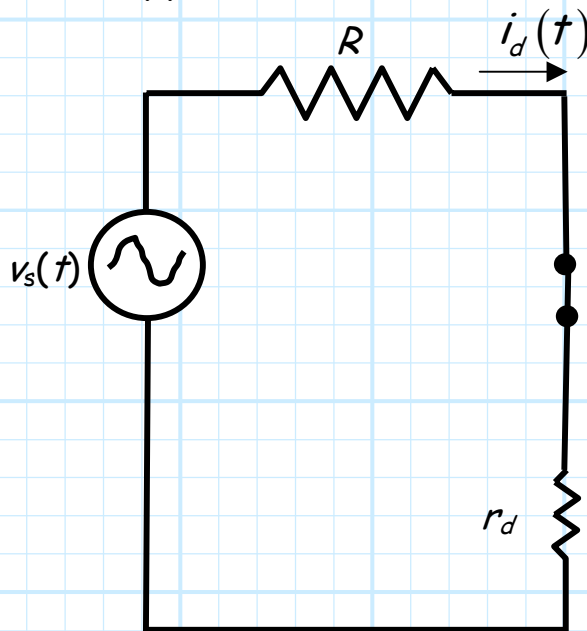
$$v_s = (R + r_d)i_d$$

Now, it is **very important** that you note this interesting result. The **DC equation** can be **directly derived** from KVL applied to this circuit:





Likewise, the **small-signal equation** can be **directly derived** from KVL applied to **this** circuit:



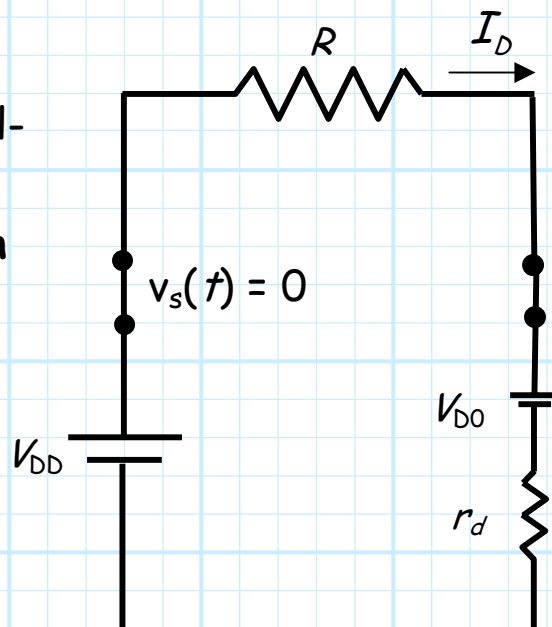
$$v_s(t) = (R + r_d) i_d(t)$$

**Just** as we can separate the total circuit KVL equation into DC and small-signal equations, we can **separate** the total **circuit** into DC and small-signal **circuits**!

Look **closely** at the two circuits. All we really have done is apply **superposition**! I.E.:

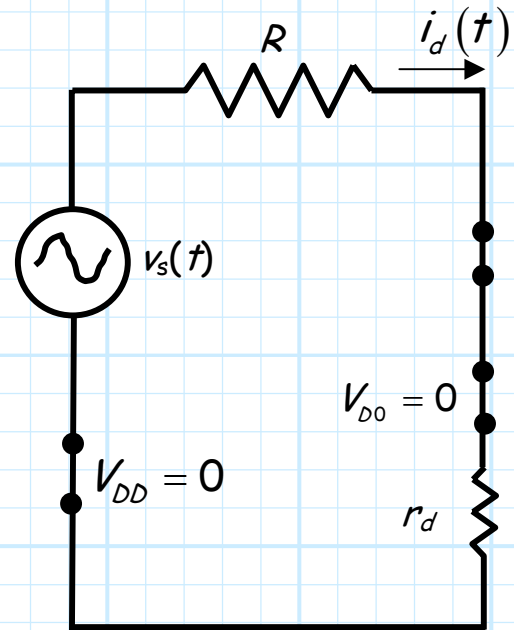
1. We turned **off** the small-signal source and then determined the **DC solution** (i.e., the DC equation):

$$V_{DD} = (R + r_d) I_D + V_{D0}$$



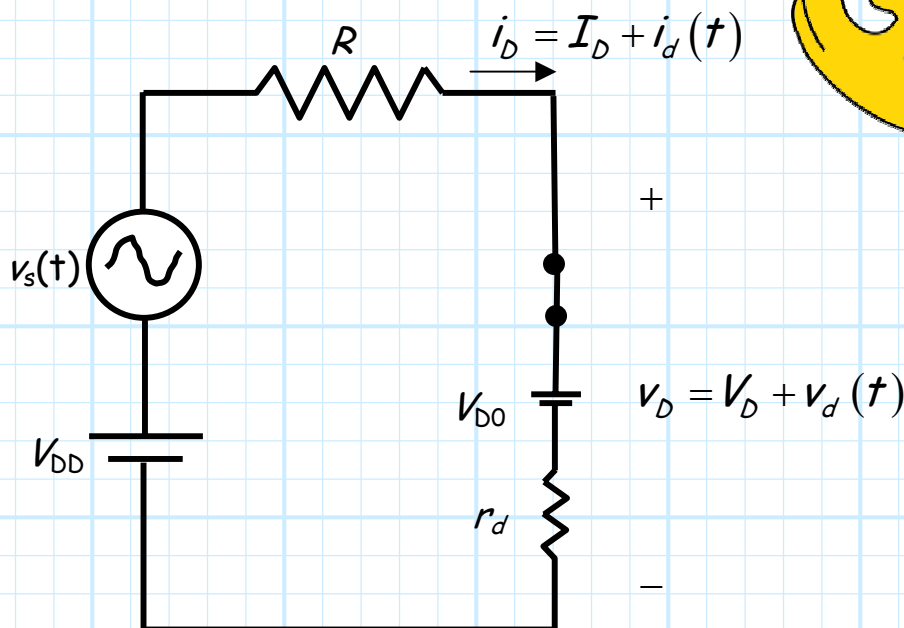
2. We then turned **off** the DC sources and determined the **small-signal solution** (i.e., the small-signal equation):

$$v_s(t) = (R + r_d) i_d(t)$$



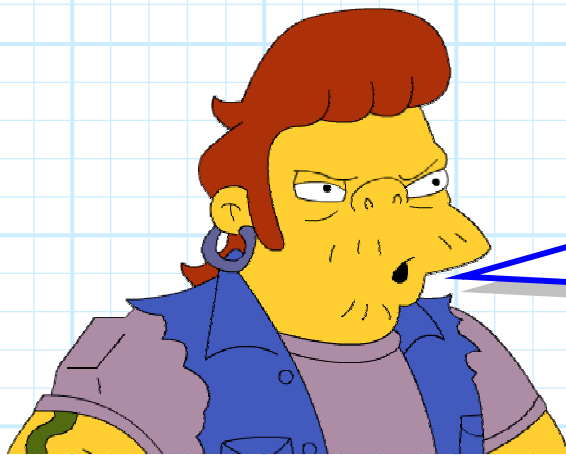
**Q:** *Hold on dude! Earlier in the course you said that diodes are **non-linear** devices, meaning that superposition **cannot** be applied!?!*

**A:** True! But look at the circuit we are analyzing—there are **no diodes** in this circuit!



- \* Recall the (assumed) forward biased ideal diode was replaced with a **short circuit**—and a short circuit is a linear device!
- \* Thus, applying superposition to this circuit is a valid analysis technique, provided that **ideal diode remains forward biased** for all time  $t$  (i.e.,  $i_d(t) > 0$  for all time  $t$ ).
- \* If the DC source is sufficiently large to place the ideal diode “firmly” into forward bias (i.e.,  $I_D \gg 0$ ), then the addition of a small AC source (i.e., the small signal source) will typically **not** change the ideal bias state (i.e.,  $I_D + i_d(t) > 0$  for all  $t$ ).

Thus, we can perform a **small-signal analysis** of a junction diode circuit (once a junction diode **model** is applied) by applying **superposition**—turn off the DC sources and analyze the resulting **small-signal circuit!**



**Q:** *But what junction diode model should I use when performing a small-signal analysis??*

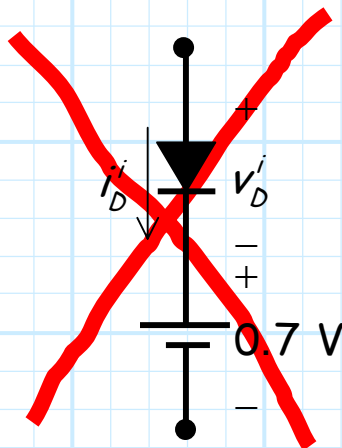
**A:** We can theoretically use **any** valid diode model (e.g., CVD, PWL) in a small-signal analysis. However, when we consider the type of small signal problem that we **typically** encounter, we find that one model stands out as **most** appropriate.

Consider the **total** diode current and **total** diode voltage when **both** DC and small-signal components are present:

$$i_D(t) = I_D + i_d(t)$$

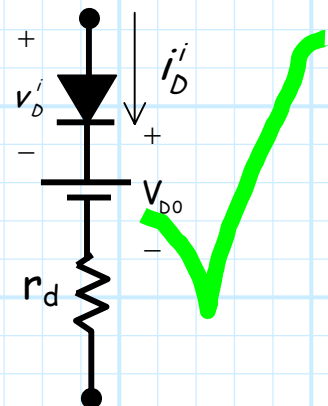
$$v_D(t) = V_D + v_d(t)$$

First of all, we can assume that the small-signal current  $i_d$  and small-signal voltage  $v_d$  is indeed—**small**. As such, we typically need some **precision** in our diode model if we are in search of **accurate** small-signal estimates.



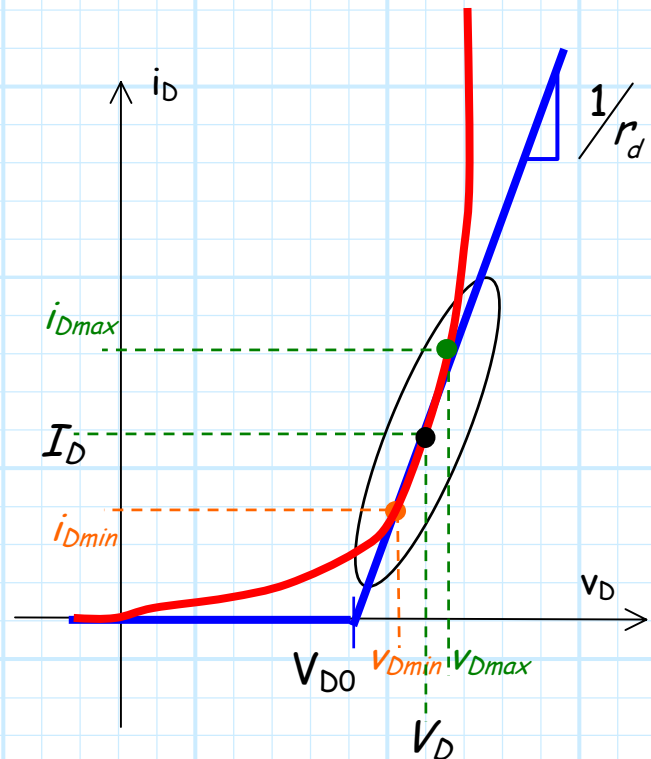
For example, the **CVD** model would **always** provide an estimate of the small-signal diode voltage of  $v_d(t)=0$  (i.e., for CVD  $v_D=0.7$  V always, thus  $V_D=0.7$  V and  $v_d=0$  **always!**)—this is **not** precise enough!

Thus we might conclude that a **PWL model** is our best bet. The problem then becomes how to **construct** this model (i.e., **what values** of  $r_D$  and  $V_{D0}$  should we use??).



First, we note that since if the small-signal diode currents and voltages are **small**, the **largest total** diode current and **total** diode voltage ( $i_D(t)$  and  $v_D(t)$ ) will **never** be much larger than the **DC** diode current and voltage  $I_D$  and  $V_D$ .

Likewise, the **smallest total** diode voltage and **total** diode current will **never** be much smaller than the **DC** diode current and voltage  $I_D$  and  $V_D$ .



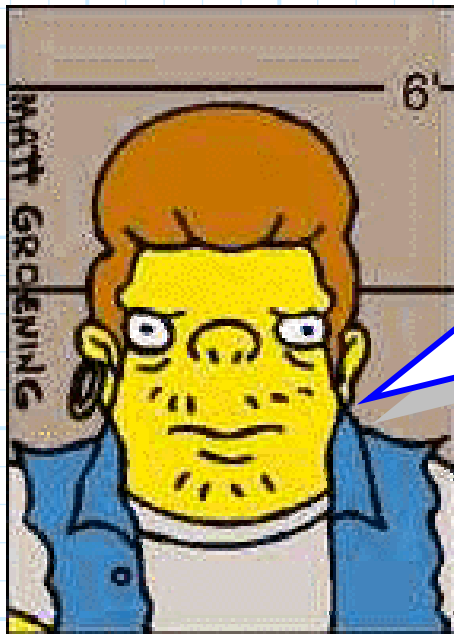
→ We need a model that **matches** the junction diode curve around the DC diode voltages  $I_D$  and  $V_D$ !

**Q:** Hey! Doesn't the *small-signal PWL model* do that?

**A:** Precisely! That's **why** we called it the small-signal PWL model—it works **best** for accurate **small-signal analysis**!

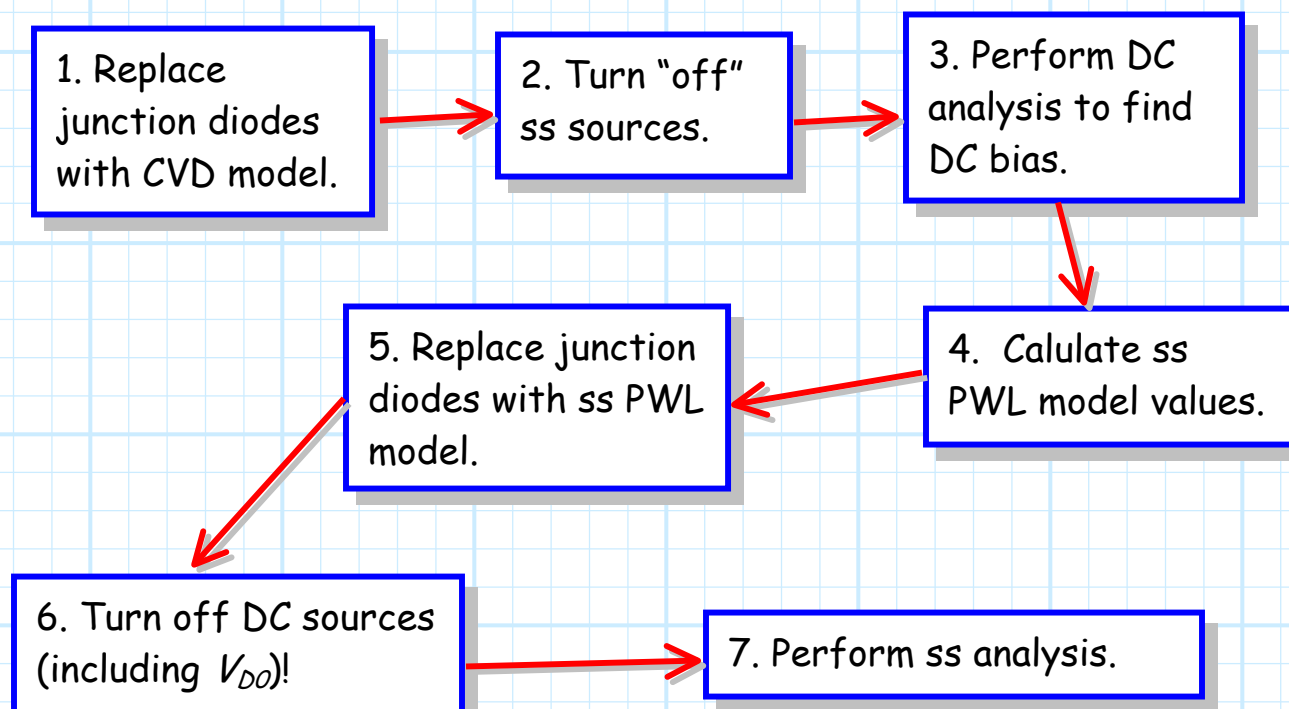
The DC diode current  $I_D$  and voltage  $V_D$  is the "**bias point**" that we spoke of when explaining the small-signal PWL model. Recall that **once** we determine these DC bias values, we can **immediately** find the model values of  $V_{D0}$  and  $r_D$ !





**Q:** *But dude, how can I determine the DC "bias" values  $I_D$  and  $V_D$  if I do not **first** know the parameters ( $V_{D0}$  and  $r_D$ ) of my PWL junction diode model?*

**A:** Easy! We simply perform a **DC analysis** with the **DC circuit** to find  $I_D$  and  $V_D$ . The "trick" is that we perform the DC analysis using the **CVD model**—and we **know** the model parameters of the CVD model!




# Small-Signal Analysis Steps

Complete **each** of these steps if you choose to correctly complete a diode **small-signal** analysis.

## Step 1: Complete a **D.C. Analysis**

Turn **off** all **small-signal** sources, and then complete a circuit analysis with the remaining **D.C. sources** only.

 Good news! The **CVD** model is accurate enough for this step (but make sure you complete every step of the **ideal** circuit analysis).

Estimate  $I_D$  for **each** junction diode.

## Step 2: Calculate diode **small-signal resistance** $r_D$

For each junction diode, determine  $r_D$  as:

$$r_D = \frac{n V_T}{I_D}$$

### Step 3: Replace junction diode with a **small-signal PWL model**

The **ideal** diode in the PWL model will be in the same bias state as the **ideal** diode in the CVD model in step 1.


In other words, if you determined in step 1 that an ideal diode is forward biased, then rest assured the same ideal diode is forward biased in this step!

### Step 4: Set all **D.C. sources** to zero.

Remember:

A zero **voltage** source is a **short**.

A zero **current** source is an **open**.

 More good news! Since source  $V_{D0}$  is a **DC** source, then we set it to zero--there is **no need** to calculate  $V_{D0}$ !

### Step 5: Analyze the **small-signal circuit**.

Analyze the circuit with small-signal sources only to find all **small-signal** voltages and currents.

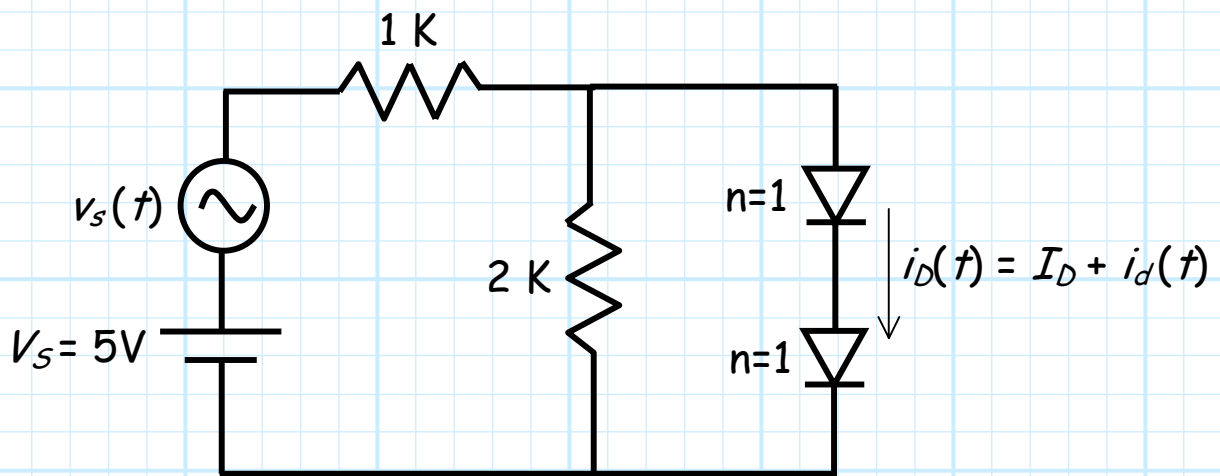
Note if  $i_d$  is the small-signal **current** through the diode, then the small signal **voltage** across the diode is:

$$V_d = i_d r_D$$



# Example: Diode Small-Signal Analysis

Consider the circuit:

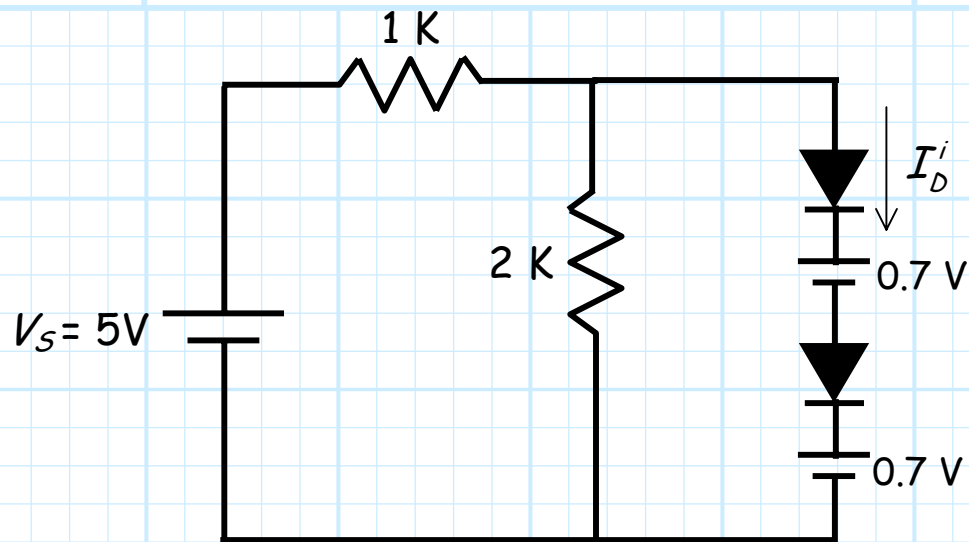


**Q:** If  $v_s(t) = 0.01 \sin \omega t$ , what is  $i_d(t)$ ?

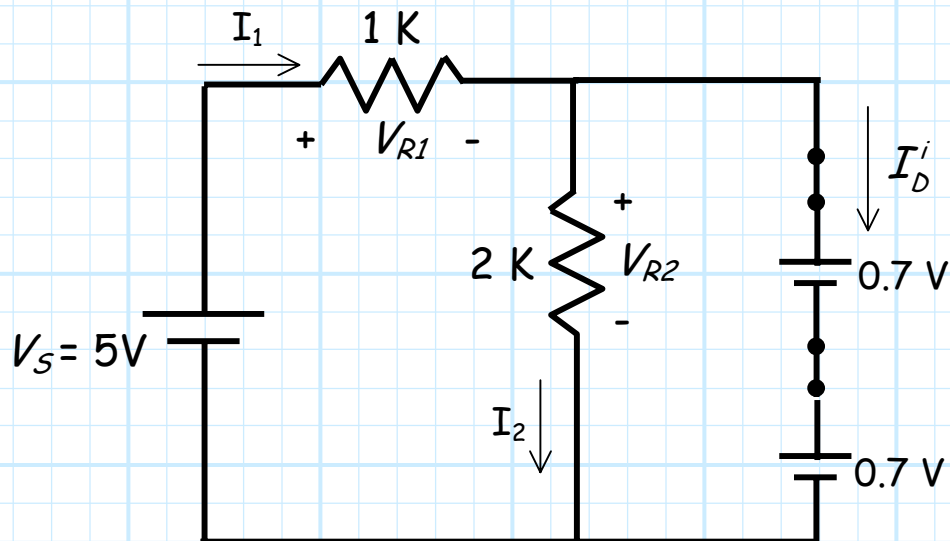
**A:** Follow the small-signal analysis steps!

Step 1: Complete a **D.C. Analysis**

Turn **off** the small-signal source and replace the junction diodes with the CVD model.



Assume the ideal diodes are "on", enforce with short circuits.



Now analyze the D.C. circuit:

From KVL  $V_{R2} = 0.7 + 0.7 = 1.4 \text{ V}$

$$\therefore I_2 = \frac{V_{R2}}{2} = 0.7 \text{ mA}$$

From KVL:  $V_{R1} = 5.0 - V_{R2} = 5.0 - 1.4 = 3.6 \text{ V}$

Thus from Ohm's Law:  $I_1 = \frac{V_{R1}}{1} = 3.6 \text{ mA}$

And finally from KCL:  $I_D^i = I_1 - I_2$   
 $= 3.6 - 0.7$   
 $= 2.9 \text{ mA}$

Now **checking** our result:

$$I_D^i = 2.9 \text{ mA} > 0 \quad \checkmark$$

Therefore our estimate of the D.C. diode current is:

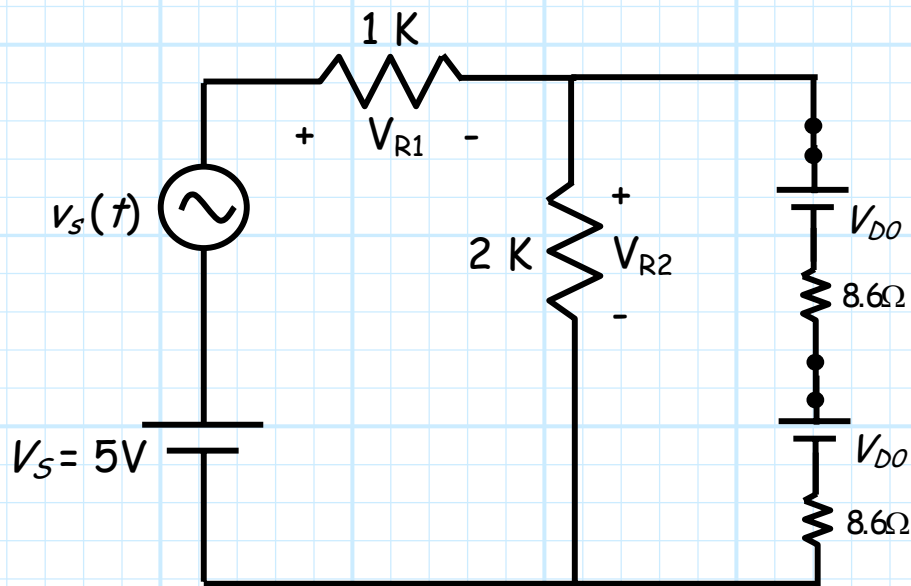
$$I_D = I_D^i = 2.9 \text{ mA}$$

Step 2: Calculate the diode small-signal resistance  $r_d$ :

$$r_d = \frac{nV_T}{I_D} = \frac{0.025}{0.0029} = 8.6 \Omega$$

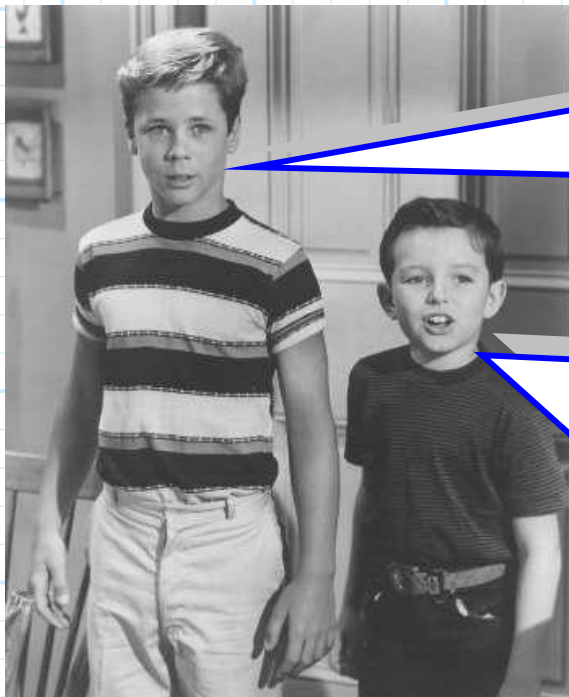
Note since the junction diodes are **identical**, and since each has the **same** current  $I_D = 2.9 \text{ mA}$  flowing through it, the small-signal resistance of each junction diode is the **same** ( $r_d = 8.6 \Omega$ ).

Step 3: Replace junction diodes with **small-signal PWL model**



Step 4: Turn off **all** D.C. sources.

This means turn off the  $5\text{ V}$  source **and** the  $V_{D0}$  sources in the **PWL model** !

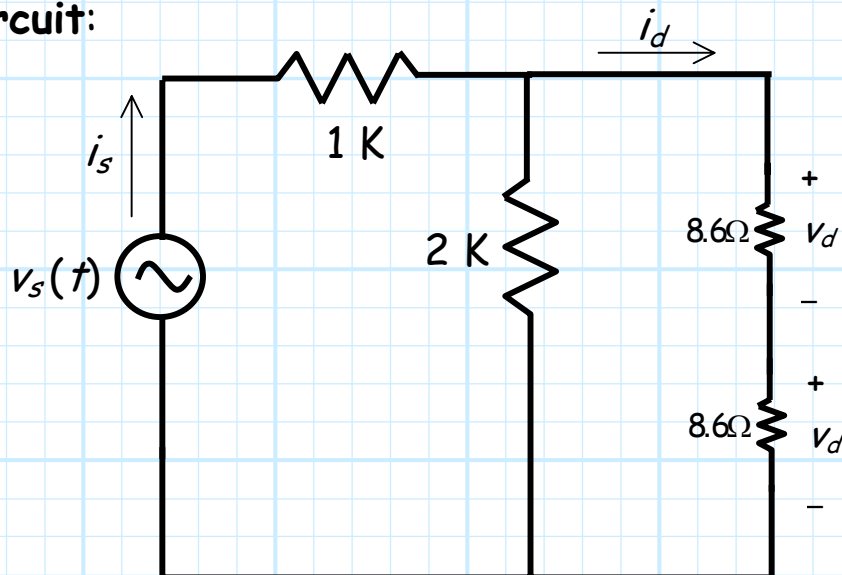


**Q:** *Jeepers! How can we turn off the  $V_{D0}$  sources in the PWL model? We haven't yet determined their **value!**?*

**A:** *Gosh Wally, don't you see! Since we're just going to set these DC sources to **zero** (i.e.,  $V_{D0}=0$ ) anyway, there is **no reason** to calculate their voltage values!*

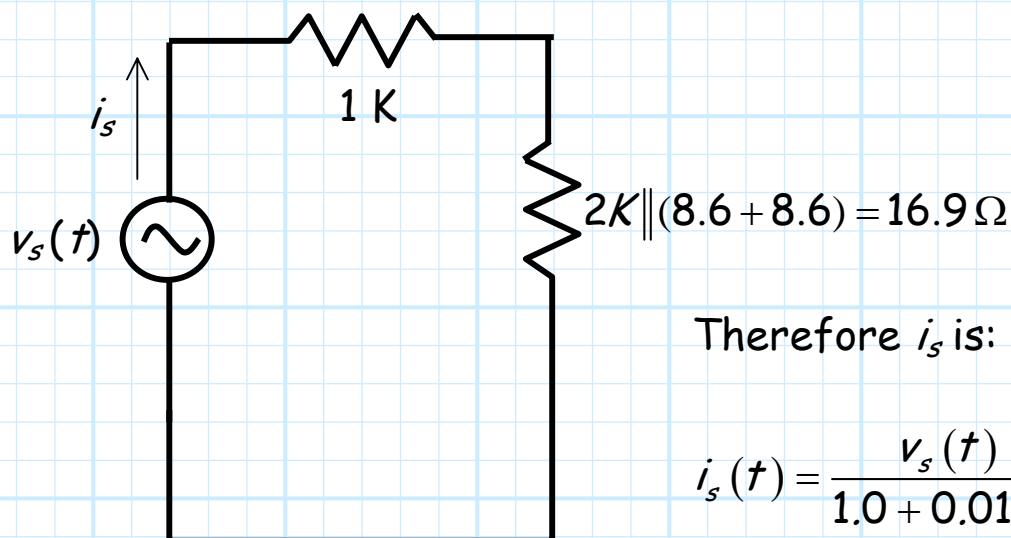
That's right! There is **no need** to determine the value of PWL model sources  $V_{D0}$ .

After turning off all DC sources, we are left with our **small-signal circuit**:



Step 5: Analyze the small-signal circuit.

Combining the parallel resistors, we get:

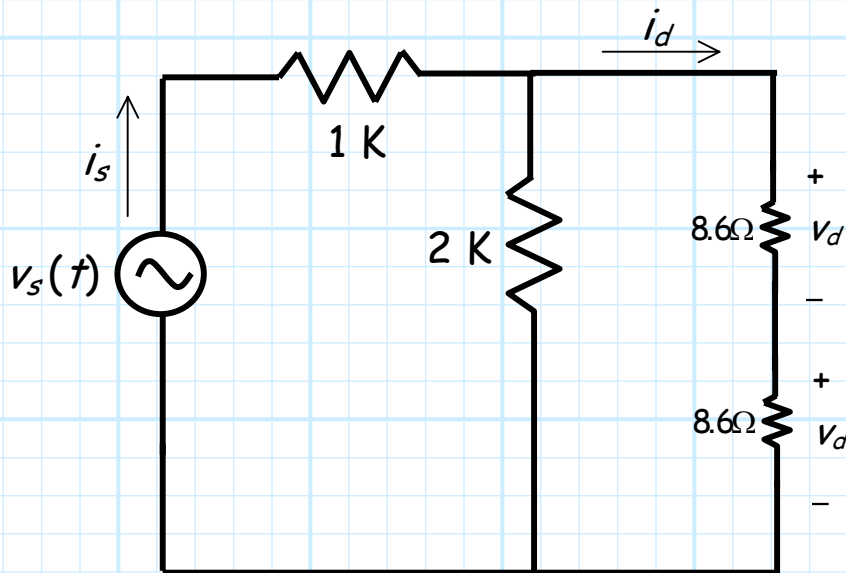


Therefore  $i_s$  is:

$$i_s(t) = \frac{v_s(t)}{1.0 + 0.0169}$$

$$= 9.83 \sin \omega t \text{ } \mu\text{A}$$

We can now find  $i_d$  using **current division**:



$$i_d(t) = i_s(t) \left( \frac{2}{2 + 0.0169} \right)$$

$$= 9.75 \sin \omega t \quad \mu\text{A}$$

And the **small signal diode voltage** is therefore:

$$v_d(t) = i_d(t) r_d$$

$$= 9.75(8.6) \sin \omega t \quad \mu\text{V}$$

$$= 83.85 \sin \omega t \quad \mu\text{V}$$