Steps for Analyzing Limiter Circuits

The junction diodes in most limiter circuits can/will be in forward bias, or reverse bias, or breakdown modes! Thus, the distinction between a Zener diode and a “normal” junction diode is essentially meaningless.

But, this presents us with a big problem—what diode model do we use to analyze a limiter? Recall that none of the diode models that we studied will provide accurate estimates for all three junction diode modes!

The solution we will use is to change the diode model we implement, as we consider each of the possible junction diode modes. Specifically:

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<th>Junction Diode Mode</th>
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<td>Forward Bias</td>
<td>CVD model with ideal diode f.b.</td>
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<td>Reverse Bias</td>
<td>Ideal diode model with ideal diode r.b.</td>
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<td>Breakdown</td>
<td>Zener CVD model with ideal diode f.b.</td>
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**Step 1:**

Assume that the limiter diode is forward biased, so replace

![diagram](diagram1.png)

with a CVD model, where the ideal diode is forward biased:

![diagram](diagram2.png)

Now, using this model, determine:

1. The output voltage $v_O$ in terms of input voltage $v_I$.

2. The ideal diode current $i_D^i$ in terms of input voltage $v_I$.

Finally, we solve the inequality $i_D^i > 0$ for $v_I$, thus determining when (i.e., for what values of $v_I$) this assumption, and thus the derived expression for output voltage $v_O$, is true.

**Step 2:**

Assume that the limiter diode is in breakdown, so replace

![diagram](diagram3.png)

or

![diagram](diagram4.png)
with a Zener CVD model, where the ideal diode is forward biased:

Now, using this model, determine:

1. The output voltage $v_O$ in terms of input voltage $v_I$.
2. The ideal diode current $i_D^I$ in terms of input voltage $v_I$.

Finally, we solve the inequality $\frac{i_D^I}{v_I} > 0$ for $v_I$, thus determining when (i.e., for what values of $v_I$) this assumption, and thus the derived expression for output voltage $v_O$, is true.

**Step 3:**

Assume that the limiter diode is reverse biased, so replace

with an Ideal Diode model, where the ideal diode is reversed biased:
Now, using this model, determine the output voltage \( v_O \) in terms of input voltage \( v_I \).

**Q:** What about \( v'_D \)? Don’t we need to likewise determine its value, and then determine when \( v'_D < 0 \)?

**A:** Actually, no. If the junction diode is not forward biased and it is not in breakdown, then it must be reverse biased! As obvious as this statement is, we can use it determine when the junction diode is reverse biased—it’s when the junction diode is not in forward bias and when it is not in reverse bias.

For example, say that we find that the junction diode is forward biased when:

\[
 v_I > 20 \text{ V},
\]

and that the junction diode is in breakdown when:

\[
 v_I < -15 \text{ V}.
\]

We can thus conclude that the junction diode is reverse biased when:

\[
 -15 \text{ V} < v_I < 20 \text{ V}
\]

**Step 4:**

We take the result of the previous 3 steps and form a continuous, piecewise linear transfer function (make sure it’s continuous, and that it’s a function!).