The Digital "Latch"

Consider two digital inverters that are "cross coupled":



Note that there are two stable states for this circuit:

W	X	У	Z	W
0	1	1	0	0
1	0	0	1	1

Thus, the latch will remain in either state until changed by an external input.

A memory device!

We of course can use CMOS inverters to build this latch:

