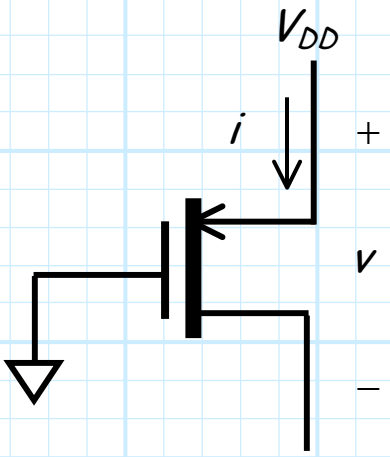
The Pseudo-NMOS Load

There is another type of active load that is used for NMOS logic, but this load is made from a **PMOS** transistor!

Hence, NMOS logic that uses this load is referred to as **Pseudo NMOS Logic,** since not all of the devices in the circuit will be NMOS (the **load** will be **PMOS**!).

We therefore call this load the "**Pseudo NMOS Load**", since it is the load used in **Pseudo NMOS logic**. But, keep in mind that the **pseudo NMOS load** is made from a **PMOS** device (this can cause great confusion!).



$$i_D = i$$
$$v_{GS} = 0 - V_{DD} = -V_{DD}$$
$$v_{DS} = -v$$
$$v_{GS} - V_t = -(V_{DD} + V_t)$$

The Pseudo-NMOS Load

Note that $v_{GS} = -V_{DD} < V_t$, so that the load is **not** in cutoff—it can either be in **saturation or triode**.

The PMOS will be in **triode** if:

$$\begin{aligned} v_{DS} &> v_{GS} - V_t \\ -v &> -\left(V_{DD} + V_t\right) \\ v &< \left(V_{DD} + V_t\right) \end{aligned}$$

In which case the **current** is:

$$\begin{aligned} i_D &= K\left[2\left(v_{GS} - V_t\right)v_{DS} - v_{DS}^2\right] \\ i &= K\left[-2\left(V_{DD} + V_t\right)(-v) - (-v)^2\right] \\ i &= K\left[2\left(V_{DD} + V_t\right)v - v^2\right] \end{aligned}$$

Likewise, the PMOS will be in saturation if:

$$\begin{aligned} v_{DS} &< v_{GS} - V_t \\ -v &< -\left(V_{DD} + V_t\right) \\ v &> \left(V_{DD} + V_t\right) \end{aligned}$$

In which case the **current** is:

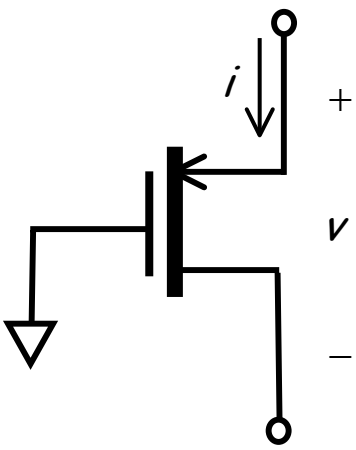
$$i_D = K\left(v_{GS} - V_t\right)^2 - \frac{v_{DS}}{r_o}$$

$$i = K\left(V_{DD} + V_t\right)^2 + \frac{v}{r_o}$$

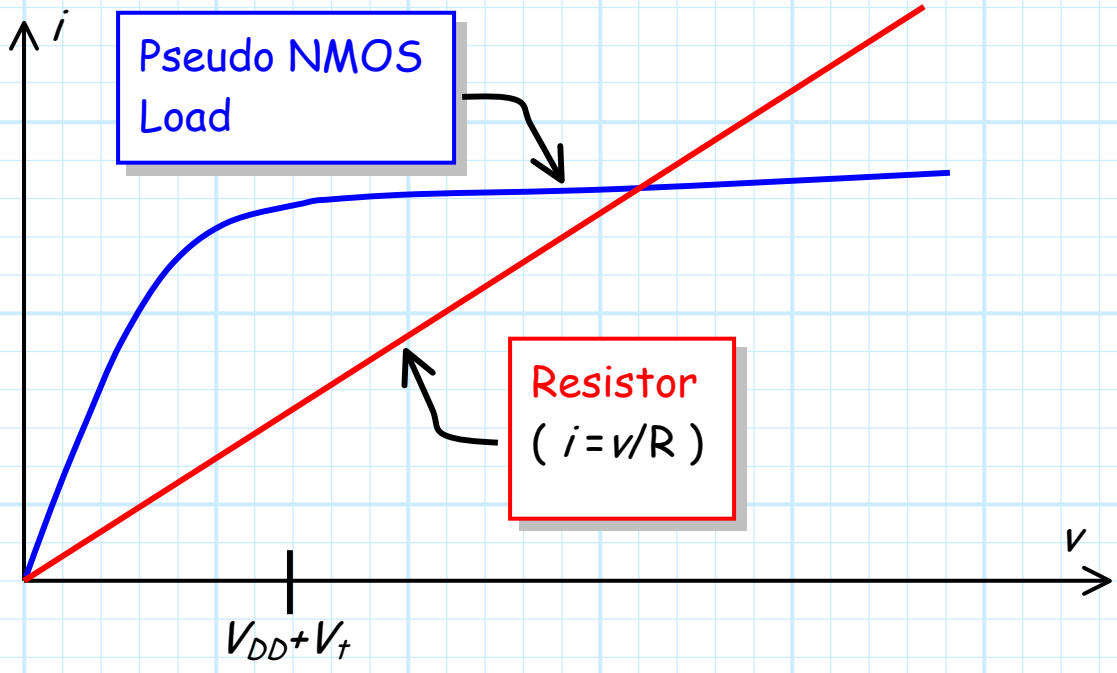
where in this case:

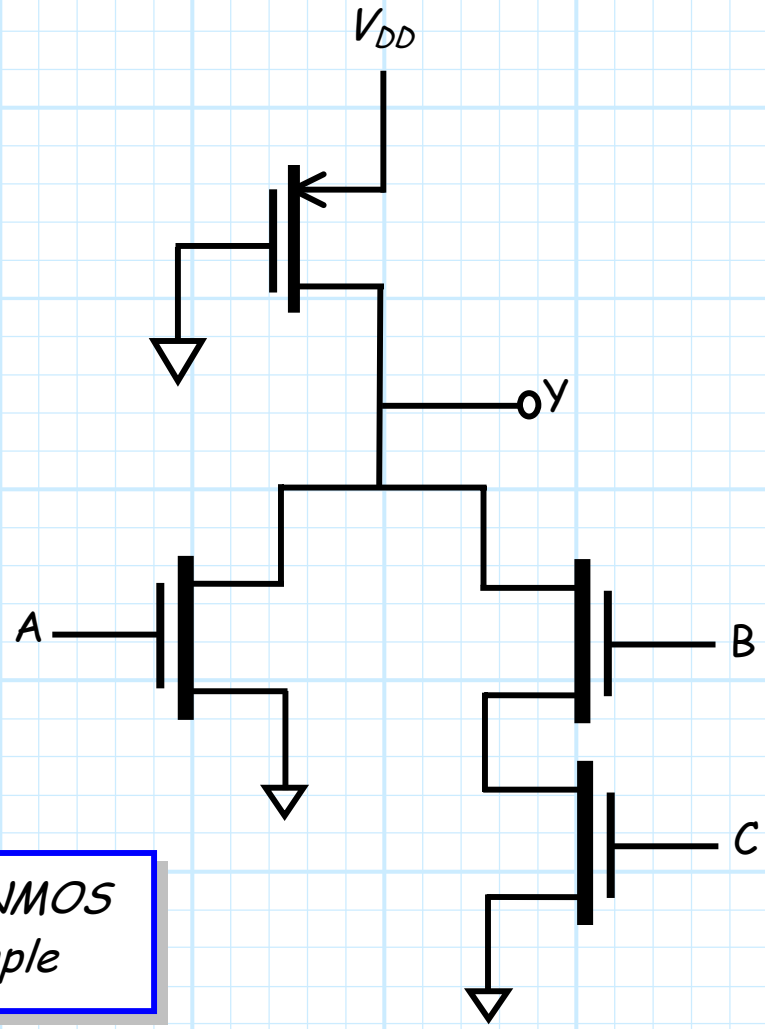
$$r_o = \frac{1}{\lambda K \left(v_{GS} - V_t\right)^2} = \frac{1}{\lambda K \left(V_{DD} + V_t\right)^2}$$

Combining these two results, we find that the pseudo NMOS load behaves very much like the depletion load:



$$i = \begin{cases} K\left[2\left(V_{DD} + V_t\right)v - v^2\right] & \text{if } 0 < v < \left(V_{DD} + V_t\right) \\ K\left(V_{DD} + V_t\right)^2 + \dfrac{v}{r_o} & \text{if } v > \left(V_{DD} + V_t\right) \end{cases}$$





A Pseudo-NMOS Logic Example