The Pseudo-NMOS Load

There is another type of active load that is used for NMOS logic, but this load is made from a PMOS transistor!

Hence, NMOS logic that uses this load is referred to as Pseudo NMOS Logic, since not all of the devices in the circuit will be NMOS (the load will be PMOS!).

We therefore call this load the "Pseudo NMOS Load", since it is the load used in Pseudo NMOS logic. But, keep in mind that the pseudo NMOS load is made from a PMOS device (this can cause great confusion!).

\[ V_{DD} \]
\[ i \]
\[ + \]
\[ i_{D} = i \]
\[ v_{GS} = 0 - V_{DD} = -V_{DD} \]
\[ v_{DS} = -V \]
\[ v_{GS} - V_{t} = -(V_{DD} + V_{t}) \]
Note that $v_{gs} = -V_{dd} < V_t$, so that the load is not in cutoff—it can either be in saturation or triode.

The PMOS will be in triode if:

\[
\begin{align*}
v_{ds} &> v_{gs} - V_t \\
\rightarrow v &> -(V_{dd} + V_t) \\
v &< (V_{dd} + V_t)
\end{align*}
\]

In which case the current is:

\[
\begin{align*}
i_o &= K \left[ 2(v_{gs} - V_t)v_{ds} - v_{ds}^2 \right] \\
i &= K \left[ -2(V_{dd} + V_t)(-v) - (-v)^2 \right] \\
i &= K \left[ 2(V_{dd} + V_t)v - v^2 \right]
\end{align*}
\]

Likewise, the PMOS will be in saturation if:

\[
\begin{align*}
v_{ds} &< v_{gs} - V_t \\
\rightarrow v &< -(V_{dd} + V_t) \\
v &> (V_{dd} + V_t)
\end{align*}
\]

In which case the current is:

\[
\begin{align*}
i_o &= K (v_{gs} - V_t)^2 - \frac{v_{ds}}{r_o} \\
i &= K (V_{dd} + V_t)^2 + \frac{v}{r_o}
\end{align*}
\]
where in this case:

\[
 r_o = \frac{1}{\lambda K (V_{GS} - V_t)^2} = \frac{1}{\lambda K (V_{DD} + V_t)^2}
\]

Combining these two results, we find that the pseudo NMOS load behaves very much like the depletion load:

\[
i = \begin{cases} 
K \left[ 2(V_{DD} + V_t) v - v^2 \right] & \text{if } 0 < v < (V_{DD} + V_t) \\
K (V_{DD} + V_t)^2 + \frac{v}{r_o} & \text{if } v > (V_{DD} + V_t)
\end{cases}
\]
A Pseudo-NMOS Logic Example