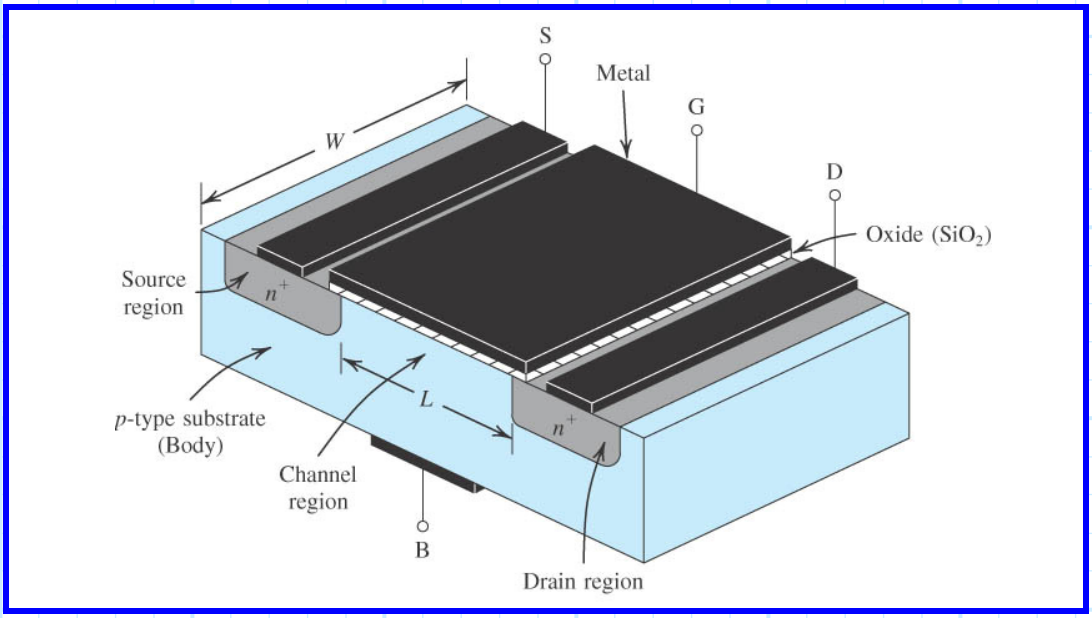
The Structure of an NMOS Enhancement FET



An **NMOS Enhancement FET** is a **FOUR** terminal device!

Moreover, each terminal has a specific **name**:

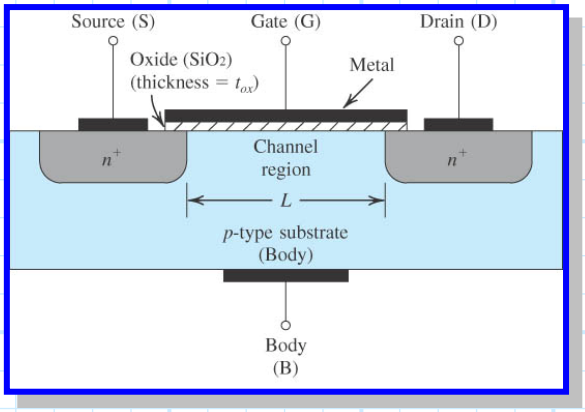
1. Source (**S**)
2. Drain (**D**)
3. Gate (**G**)
4. Body (**B**)

Each terminal is associated with a **metal electrode** that is attached to the semiconductor device.

* The **Body** electrode is connected directly to the *p*-type substrate.

* Two **heavily** doped *n*-type "wells" are implanted into the *p*-type substrate. The **Source** and **Drain** electrodes are each connected to one of these n^+ wells.

* The region between these n^+ wells is called the **channel**. The channel has **two** important geometries—**channel width** *W*, and **channel length** *L*.



* **Typical** values for channel **length** *L* are 0.1 to 3 μm (1 μm is 0.001 millimeter!), while channel **width** *W* is typically 0.2 to 100 μm.

* The **Gate** electrode rests on top of the channel, but is **not** connected directly to it. Instead, the channel and gate electrode are **separated** by a thin (e.g., 2-5 nm) layer of Silicon Dioxide (SiO_2).

* Silicon Dioxide is essentially glass! Glass is a very good **insulator**—thus, no current can flow from the gate into the MOSFET device!

* Thus, the Silicon Dioxide layer is **sandwiched** between the metal Gate electrode and the p-type channel. It is these **three** materials that give the **MOS**FET its name—**M**etal (Gate electrode) **O**xide (SiO_2) **S**emiconductor (*p*-type channel) FET.