4.3- Modeling the Diode Forward Characteristic

Reading Assignment: ***pp. 179-188***

How do we **analyze** circuits with junction diodes?

2 ways:

Exact Solutions → **Difficult!**

Approximate Solutions → **Easy (relatively).**

A. Exact Solutions

The junction diode equation often results in an "unsolvable" **transcendental equation**!

HO: TRANSCENDENTAL SOLUTIONS OF JUNCTION DIODE CIRCUITS

B. Approximate Solutions

To obtain a quick (but less accurate) solution, we replace all junction diodes with **approximate** circuit models.

3 kinds of models:

1. Ideal Diode
2. Constant Voltage Drop (CVD)
3. Piecewise-Linear (PWL)

HO:THE IDEAL DIODE MODEL

To improve on the ideal diode model, we simply add a **voltage source**!

HO: THE CONSTANT VOLTAGE DROP MODEL

Let's try a circuit analysis **example** with the **CVD model**.

EXAMPLE: JUNCTION DIODECIRCUIT ANALYSIS WITH THE CVD MODEL

A more accurate—but much more complex—model is the **Piecewise Linear Model** (PWL).

HO: The Piecewise Linear Model

There are at least **two good approaches** for constructing an accruate junction diode PWL model.

HO: Constructing the PWL Model

Let's try an **example** for constructing a PWL model.

Example: Constructing a PWL Model

It is **unfathomably important** that you learn how to correctly implement these models to analyze **junction** diode circuits!

Example: Junction Diode Models

Transcendental Solutions of Junction Diode Circuits

In a previous example, we were able to use the junction diode equation to **algebraically** analyze a circuit and find **numeric** solutions for all circuit currents and voltages.

However, we will find that this type of circuit analysis is, in general, often **impossible** to achieve using the junction diode equation!

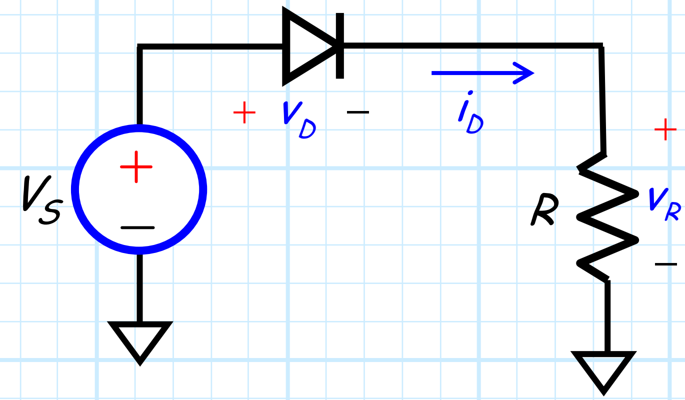
Q: *Impossible !?!*

If we have an explicit mathematical description of each device in a circuit (which we do for a junction diode), can't we can use KVL and KCL to analyze ***any*** *circuit.*

A: Although we can always determine a **numerical** solution, it is often impossible to find this solution **algebraically**.

One equation and one unknown—so what's the big deal

Consider this **simple** junction diode circuit:



From KVL:

$$V_S - v_D - v_R = 0$$
$$\therefore \; V_S - v_D - R\, i_D = 0$$
$$\therefore \; i_D = \frac{V_S - v_D}{R}$$

Likewise, from the **junction** diode equation:

$$i_D = I_s\left(e^{\frac{v_D}{nV_T}} - 1\right)$$

Equating these two, we have a **single** equation with a **single** unknown (v_D):

$$\frac{V_S - v_D}{R} = I_s\left(e^{\frac{v_D}{nV_T}} - 1\right)$$

Try solving this!

Q: *Right!*

*You have **1 equation** with **1 unknown**.*

Just solve this equation for v_D, and then you can determine all other unknown voltages and currents (i.e., i_D and v_R).

A: But that's the **problem**!

What **is** the algebraic solution of v_D for the equation:

$$\frac{V_S - v_D}{R} = I_s\left(e^{\frac{v_D}{nV_T}} - 1\right)$$

Q: *????*

A: The above equation is mystically known as a **transcendental equation**.

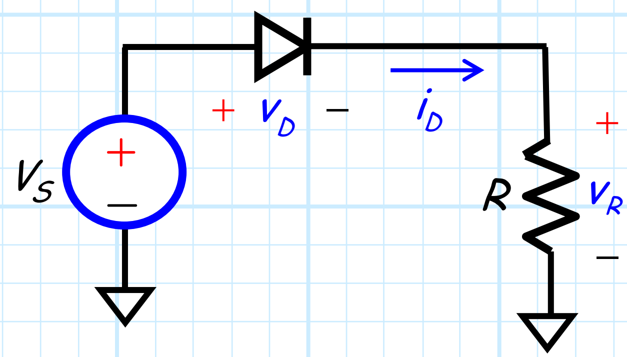
It is an algebraic expression for which there is **no algebraic solution**!

There is a solution, however

Examples of transcendental equations include:

$$x = cos\left[x\right], \quad y^2 = ln\left[y\right], \quad \text{or} \quad 4 - x = 2^x$$

Q: *But, we could **build** this simple junction diode circuit in the lab.*



*Therefore v_D, i_D and v_R must have **some** numeric value, right !?!*

A: Absolutely!

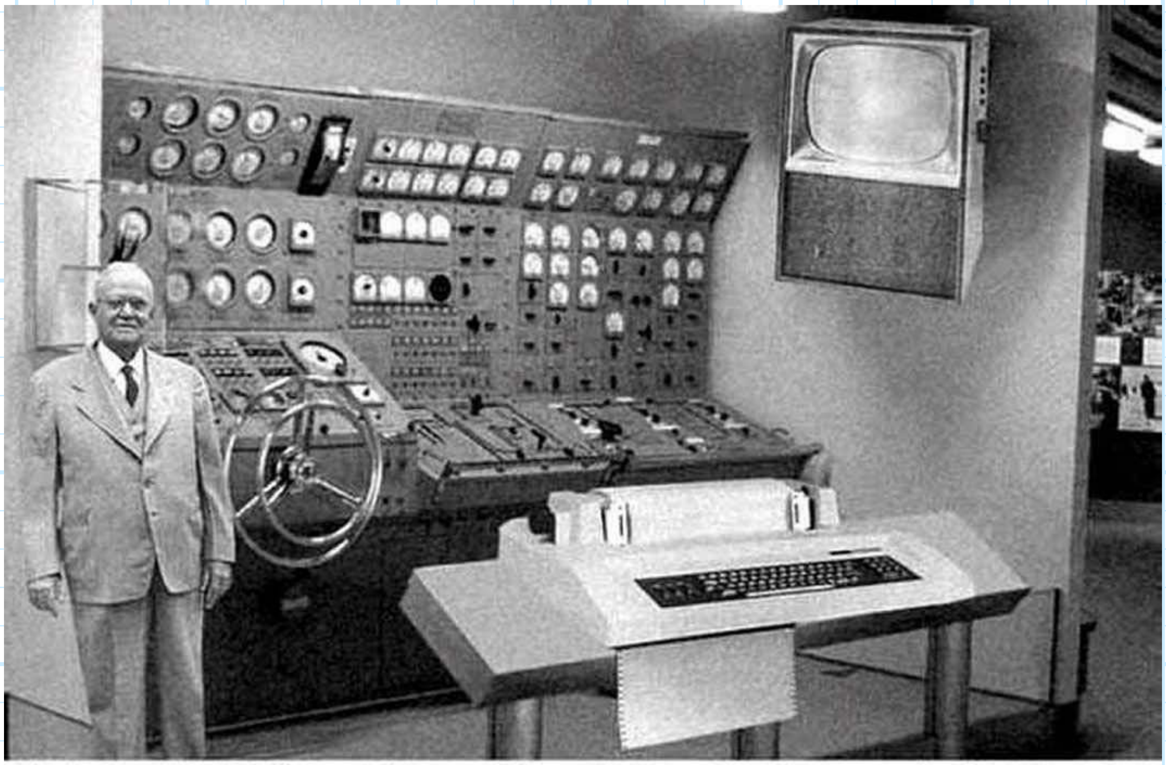
For every value of source voltage V_S, resistance R, and junction diode parameters n and I_s, there **is** a specific numerical solution for v_D, i_D and v_R.

However, we **cannot** find this **numerical** solution with **algebraic** methods!

The solution requires a computer

Q: *Well then how the heck **do** we find solution??*

A: We use what is know as **numerical methods**, often implementing some **iterative** approach, typically with the help of a **computer**.



Scientists from the RAND Corporation have created this model to illustrate how a "home computer" could look like in the year 2004. However the needed technology will not be economically feasible for the average home. Also the scientists readily admit that the computer will require not yet invented technology to actually work, but 50 years from now scientific progress is expected to solve these problems. With teletype interface and the Fortran language, the computer will be easy to use.

This generally involves **more work** than we wish to do when analyzing junction diode circuits (despite the help of Fortran and the teletype)!

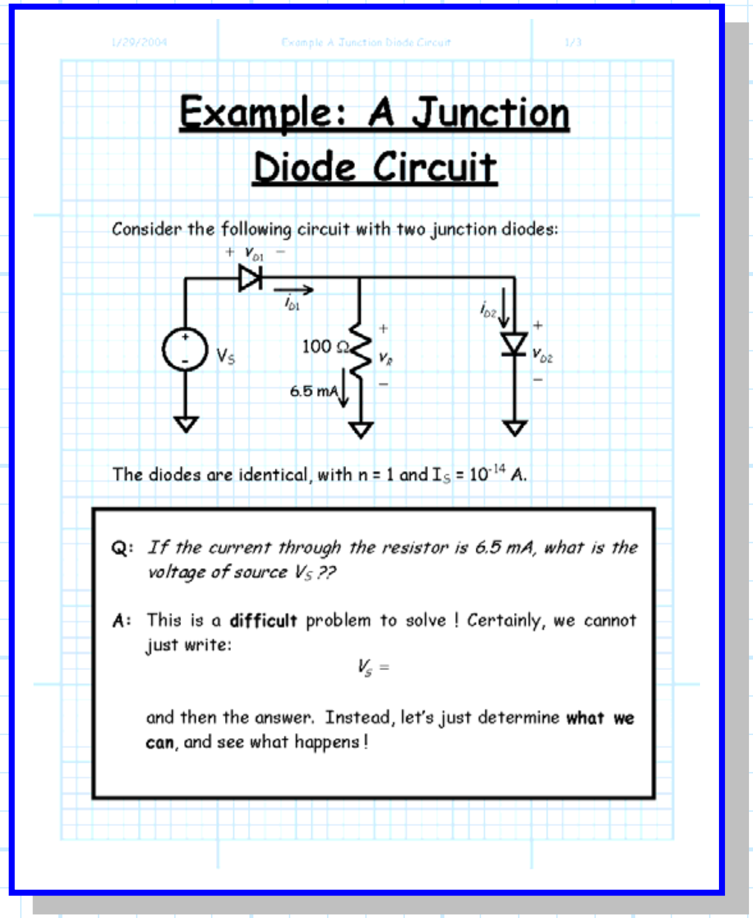
But, we did it before without a computer!

Q: *So just how **do** we analyze junction diode circuits??*

A: We replace the junction diodes with **circuit models** that **approximate** junction diode behavior!

Q: *Wait!*

*I recall an **earlier example** when analyzed a junction diode circuit, but we did **not** use "approximate models" nor "numerical methods" to find the answer!*



Example: A Junction Diode Circuit

Consider the following circuit with two junction diodes:

The diodes are identical, with $n = 1$ and $I_S = 10^{-14}$ A.

Q: *If the current through the resistor is 6.5 mA, what is the voltage of source V_S??*

A: This is a **difficult** problem to solve ! Certainly, we cannot just write:

$$V_S =$$

and then the answer. Instead, let's just determine **what we can**, and see what happens !

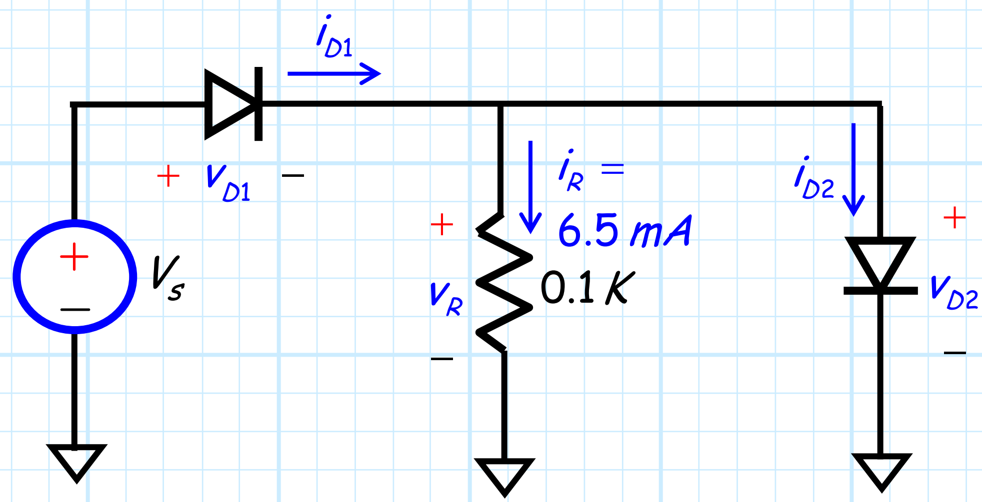
A: This is absolutely correct; we did **not** use approximate models or numerical methods to solve that problem.

However, if you look back at that example, you will find that the problem was a bit **contrived**.

Professors: they're so tricky!

Recall that effectively, we were **given** the voltage across one diode as part of the problem statement.

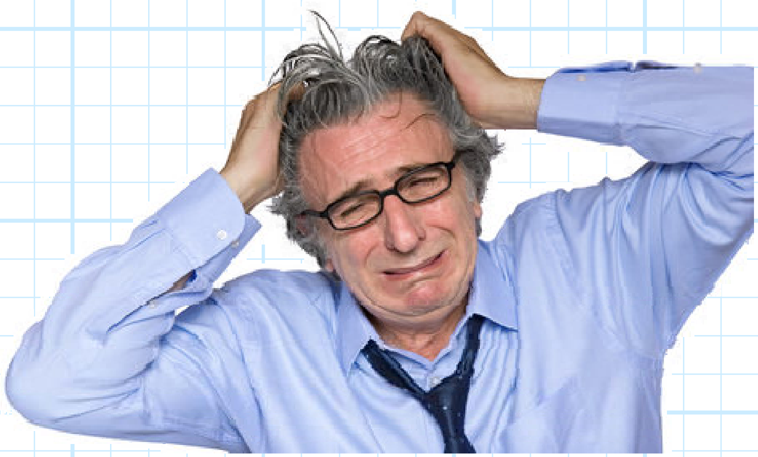
We were then asked to find the **source voltage** V_S.



This was a bit of an **academic** problem, as in the "real world" it is **unlikely** that we would somehow know the voltage across the diode without knowing the value of the voltage source that produced it!

Thus, problems like this previous example are sometimes used by **professors** to create junction diode circuit problems that are solvable, **without** encountering a dreaded **transcendental equation**!

Transcendental is the norm; circuit models are the solution



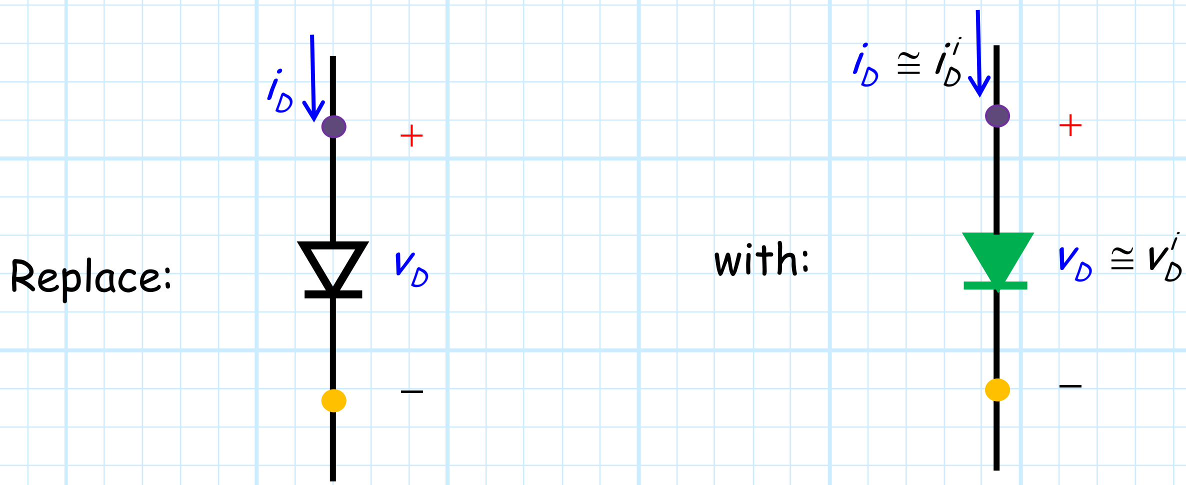
In the **real world**, we typically know **neither** the diode voltage **nor** the diode current directly—transcendental equations are most often the **sad** result!

Instead of applying numerical techniques, we will find it much **faster** (albeit slightly **less accurate**) to apply **approximate circuit models**.

The Ideal Diode Model

One way to analyze junction diode circuits is simply to **assume** the junction diodes are **ideal**.

In other words:



We **know** how to analyze **ideal** diode circuits (recall sect. 4.1)!

This is why we studied section 4.1

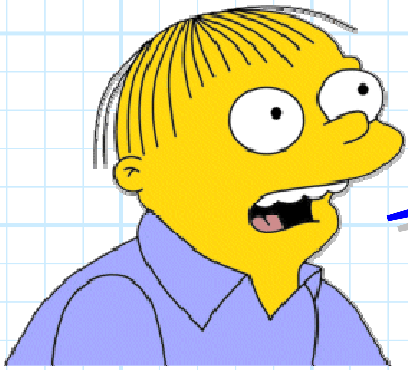
IMPORTANT NOTE !!! PLEASE READ THIS CAREFULLY:

Make sure you analyze the resulting circuit **precisely** as we did in section 4.1:

1. You **assume** the same **ideal** diode modes,
2. you **enforce** the same **ideal** diode values,
3. you **analyze** in the **exact same** manner,
4. and you **check** the same **ideal** diode results, precisely as before.

Once we replace the junction diodes with ideal diodes, we have an ideal diode circuit—**no junction diodes** are involved!

That's the thing about approximations—they give you answers that are only approximately correct



Q: *But, ideal diodes are **not** junction diodes; won't we get the **wrong** answer???*

A: **YES !!!** Darn right we won't !

However, the answers, albeit **incorrect**, will be **close** to the actual values.

In other words, our answers will be **approximately** correct.

We **approximate** a junction diode as an ideal diode.

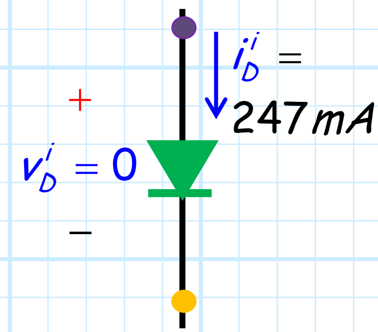
Our answers are therefore—**approximations** !!

For example

For **example**, say we replace the junction diode in a circuit with the ideal diode model.

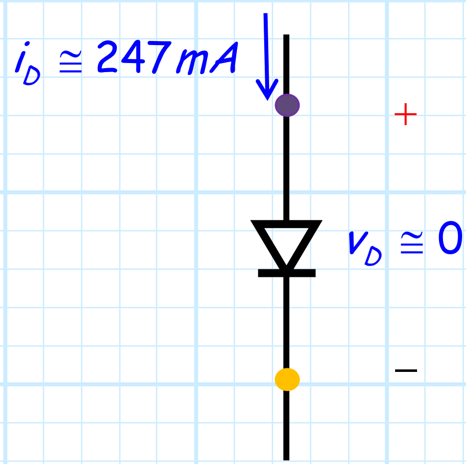
→ We now have an **ideal** diode circuit!

Say we then **assume**, **enforce**, **analyze** and **check**, and find that the **ideal** diode current and voltage are:



$$i_D^i = 247\,mA \qquad \text{and} \qquad v_D^i = 0$$

Thus, we conclude that the **junction** diode current is **approximately** 247 mA, and the **junction** diode current is **approximately zero**.

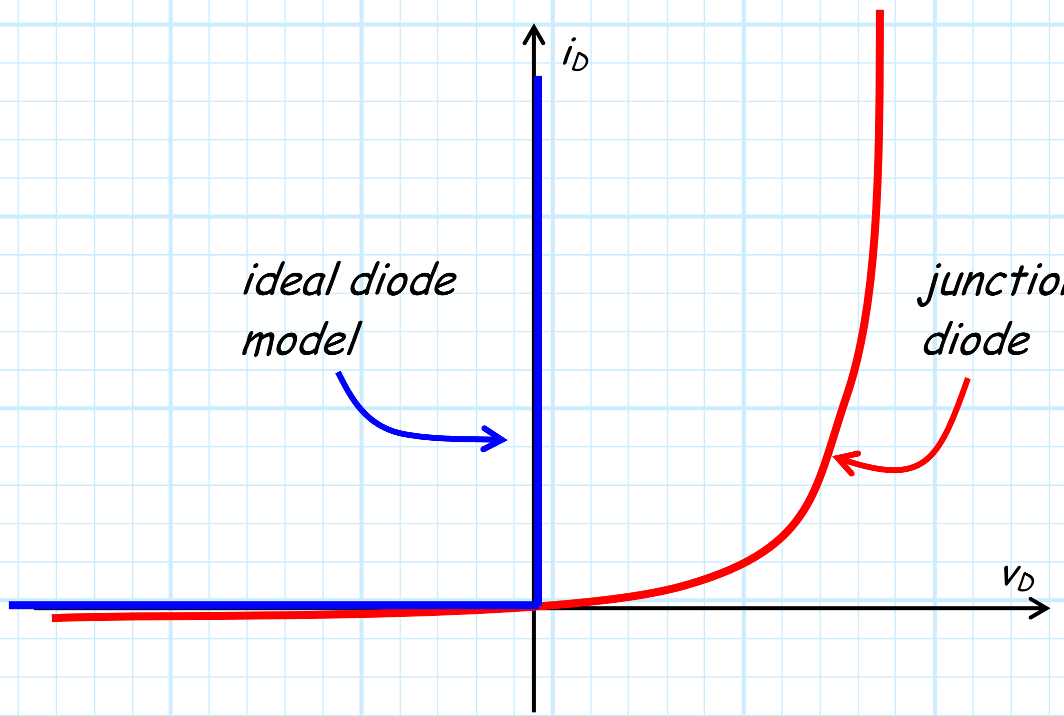


It's that approximation thing again—they're always in error

Q: *What?*

*I thought that if the junction diode current is positive, then the junction diode voltage is **approximately** 0.7 V—**not** zero volts!*

A: Yes, the ideal diode model provides a **course approximation**—with perhaps significant **error**—particularly if the junction diode is operating in the forward bias region.



The Constant Voltage Drop (CVD) Model

Q: *We know **if significant** positive current flows through a junction diode, the diode voltage will be some value **near 0.7** V.*

***Yet**, the ideal diode model provides an approximate answer of v_D=**0 V**.*

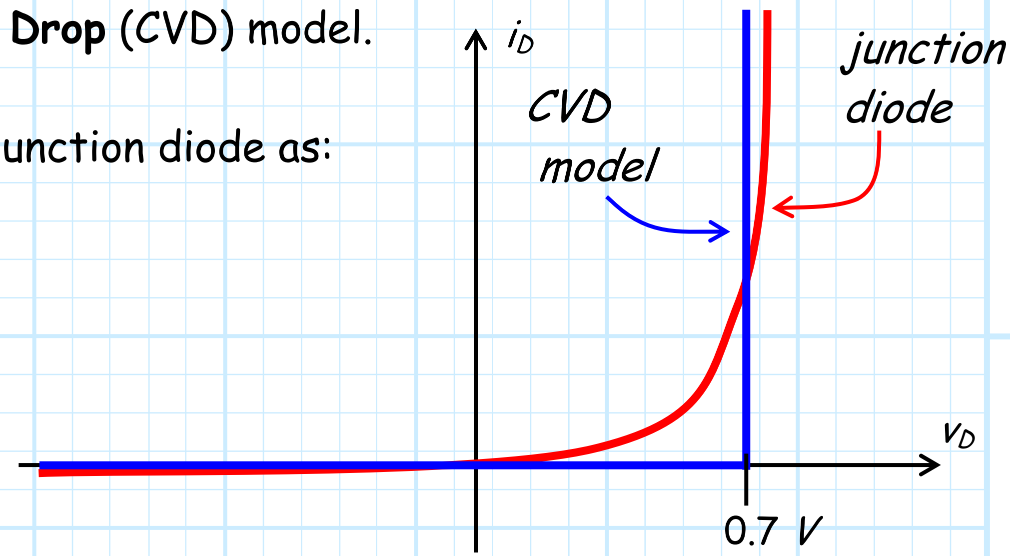
*Isn't there a more **accurate** model?*

A: Yes! Consider the **Constant Voltage Drop** (CVD) model.

For the **CVD model**, we approximate a junction diode as:

$$i_D = 0 \qquad if \qquad v_D < 0.7\,V$$

$$v_D = 0.7\,V \qquad if \qquad i_D > 0$$



Note this is a **fairly accurate** statement of junction diode behavior!

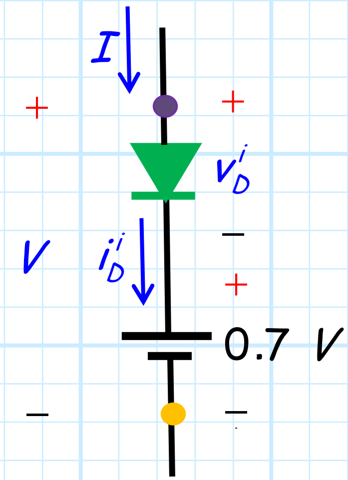
Models have more than one components

Q: *Yes, but what is the **circuit device** for the CVD model—I don't know of **any** component that behaves likes this?*

A: Our circuit models do **not** have to be a **single** device.

Instead, these models typically consist of **two or more** devices!

For example, consider an ideal diode in series with a **0.7 V voltage source**:



From **KVL** we find:

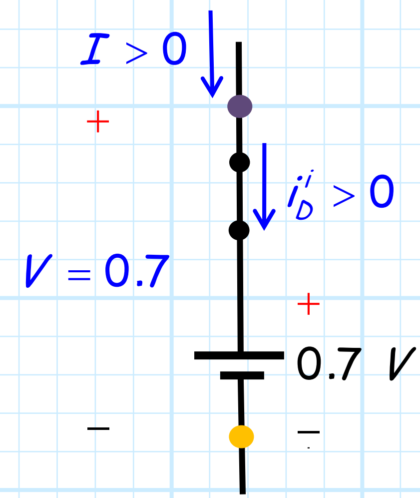
$$V = v_D^i + 0.7 \quad \Rightarrow \quad \therefore \; v_D^i = V - 0.7$$

And from **KCL**:

$$i_D^i = I$$

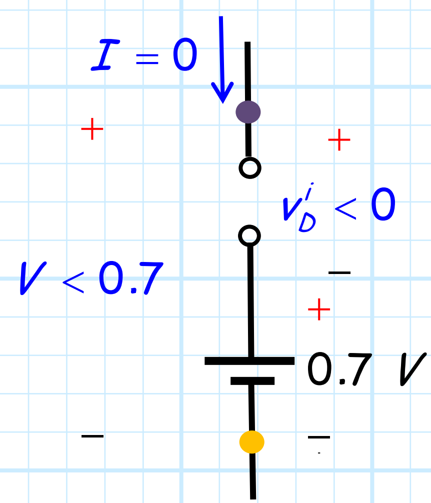
V is the voltage across the *entire* model!

Thus, **if** the **ideal** diode in this circuit is **forward biased** ($i_D^i > 0$ and $v_D^i = 0$), the model voltage and current is:



$$v_D^i = V - 0.7 = 0 \quad \Rightarrow \quad \therefore\ V = 0.7 \qquad \text{and} \qquad i_D^i = I > 0$$

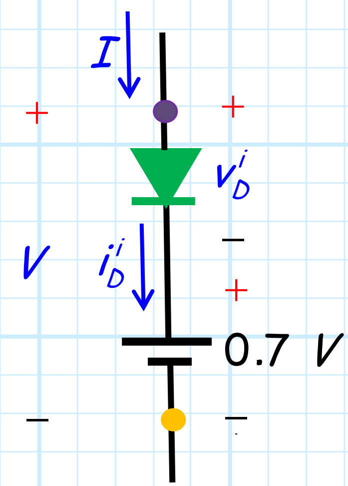
Or, **if** the **ideal** diode in this circuit is **reverse biased** ($v_D^i < 0$ and $i_D^i = 0$), the model voltage and current is:



$$i_D^i = I = 0 \qquad \text{and} \qquad v_D^i = V - 0.7 < 0 \quad \Rightarrow \quad \therefore\ V < 0.7$$

Smells like the CVD model!

In **summary**, we find that for this circuit model:



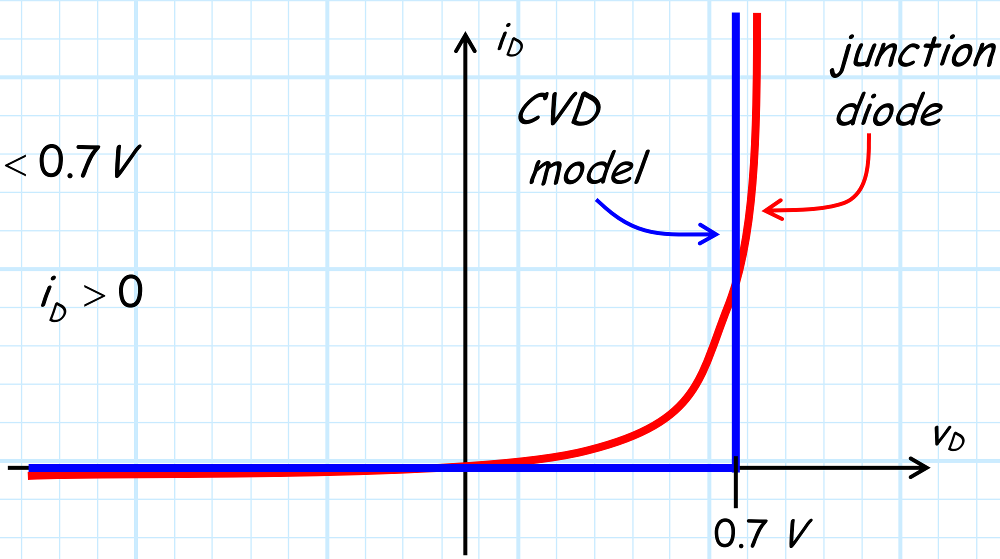
$$I = 0 \qquad if \qquad V < 0.7\,V$$

$$V = 0.7\,V \qquad if \qquad I > 0$$

Q: *Hey! Isn't this precisely the expression for the **CVD model**, only with $v_D = V$ and $i_D = I$??*

$$i_D = 0 \qquad if \qquad v_D < 0.7\,V$$

$$v_D = 0.7\,V \qquad if \qquad i_D > 0$$

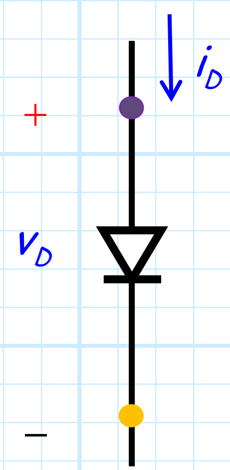


Just like we did for the ideal diode model

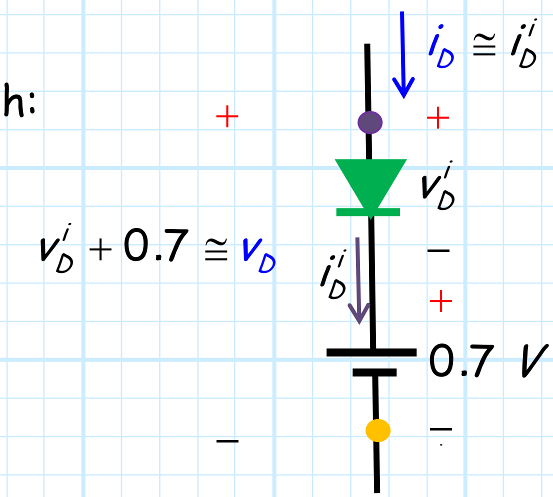
A: It **is**!

This circuit is the **CVD circuit model**, and we use it to analyze **junction** diode circuits in precisely the **same** manner as with the **ideal diode model**:

Replace:



with:



In other words, replace the junction diode with **two** devices—an **ideal diode** in series with a **0.7 V voltage source**.

Give me three steps..

To find **approximate** current and voltage values of a **junction** diode circuit, follow these **3 steps**:

Step 1 - **Replace** each junction diode with the **two** devices of the **CVD model**.

Note you now a have an **IDEAL** diode circuit! There are **no junction diodes** in the circuit, and therefore **no junction diode** knowledge need be (or should be) used to analyze it.

Step 2 - Now **analyze** the **IDEAL** diode circuit on your paper. Determine i_D' and v_D' for **each ideal** diode.

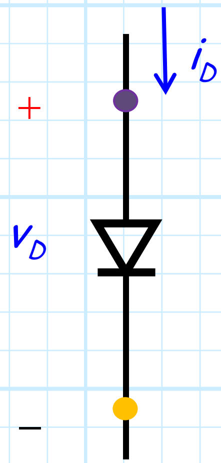
IMPORTANT NOTE!!! PLEASE READ THIS CAREFULLY:

Make sure you analyze the resulting circuit **precisely** as we did in section 4.1.

You **assume** the same **IDEAL** diode modes, you **enforce** the same **IDEAL** diode values, and you **check** the same **IDEAL** diode results, **precisely** as before. Once we replace the junction diodes with the CVD model, we have an **IDEAL** diode circuit—**no junction diodes** are involved!

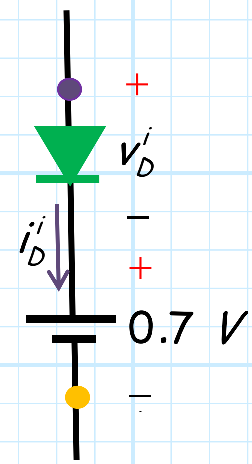
Step 3 gives the *approximate* answer

Step 3 - Determine the **approximate** values i_D and v_D of the **junction** diode from the **ideal** diode values i_D^i and v_D^i:



$$i_D \cong i_D^i$$

$$v_D \cong v_D^i + 0.7 \quad V$$



The junction voltage is always 0.7 higher

Note therefore, **if** the **IDEAL** diode (note here I said **IDEAL** diode) is **forward** biased ($i_D^i > 0$), then the **approximation** of the **junction** diode current will likewise be positive ($i_D > 0$), and the **approximation** of the **junction** diode voltage (unlike the **ideal** diode voltage of $v_D^i = 0$) will be:

$$\begin{aligned} v_D &= v_D^i + 0.7 \\ &= 0.0 + 0.7 \\ &= 0.7 \text{ V} \end{aligned}$$

However, **if** the **IDEAL** diode is **reversed** biased ($i_D^i = 0$), then the **approximation** of the **junction** diode current will likewise be zero ($i_D = 0$), and the approximation of the junction diode voltage (unlike the **ideal** diode voltage of $v_D^i < 0$) will be:

$$\begin{aligned} v_D &= v_D^i + 0.7 \\ &< 0.7 \text{ V} \end{aligned}$$

Note that the approximate **junction** diode voltage is **always 0.7V more** than the **ideal** diode voltage—don't forget to **add 0.7** to your calculated value of v_D^i!

If the voltage is positive, why isn't there current?

Q: *Wait a second!*

*Say the **ideal** diode in the CVD model turns out to be **reverse biased**, with:*

$$v_D^i = -0.1\,V \text{ and } i_D^i = 0\,.$$

*The "approximate" **junction** diode current and voltage would thus be:*

$$v_D \cong v_D^i + 0.7 = -0.1 + 0.7 = 0.6\,V$$

$$i_D \cong i_D^i = 0$$

*The junction diode voltage is **0.6 V**—this **instead** sounds like **forward** bias!*

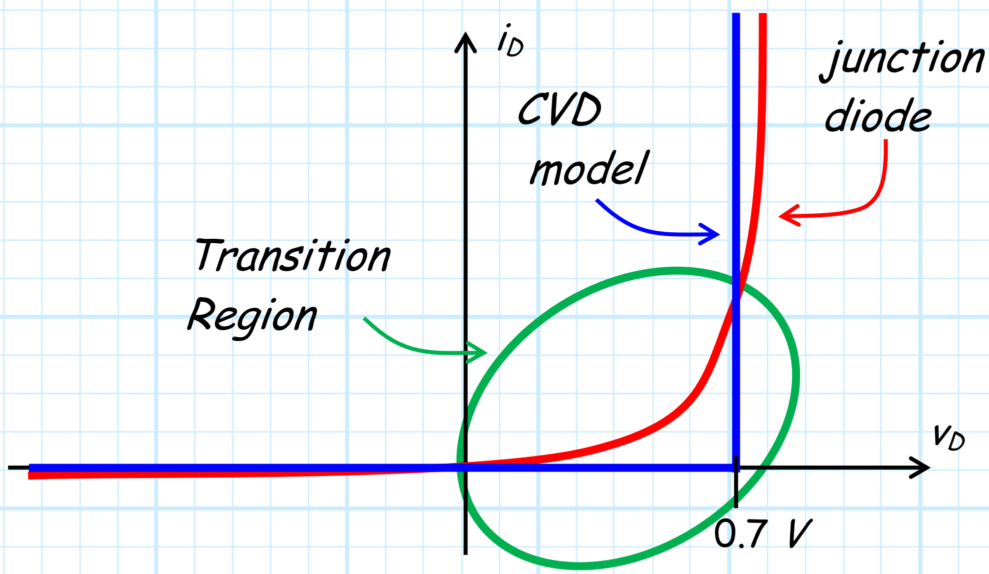
→ *How does this make sense?*

That ambiguous transistion!

A: Remember, an **ideal** diode must be **unambiguously** forward or reversed biased.

But, a **junction** diode operates in **ambiguously** defined "regions", whose **boundaries** are a bit **murky**.

Thus, a result like the **example above**, where $v_D \cong 0.6\ V$ (the **forward** bias region?) and $i_D \cong 0$ (the **reverse** bias region?), is indicative of junction diode operating in the **ambiguous transition region** between forward and reverse bias.



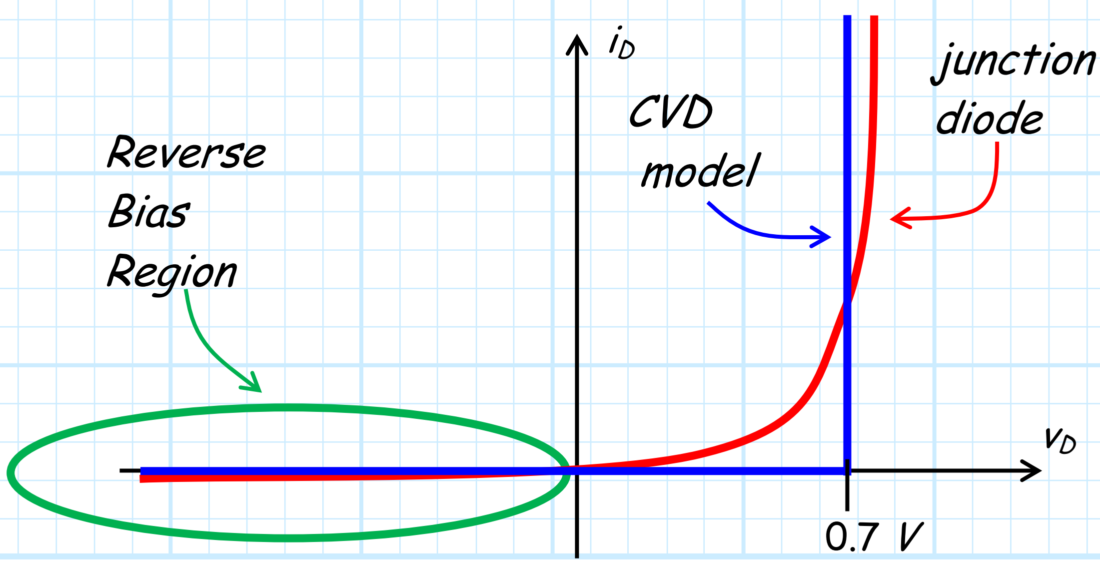
Works quite well for reverse bias region

In other words, the junction diode current is **not** sufficiently large to be unambiguously in the **forward** bias region, but **neither** is it sufficiently negative to be unambiguously in the **reverse** bias region!

Q: *But still, a junction diode with a voltage of $v_D = 0.6\ V$ would **not** have zero current—and **vice versa**.*

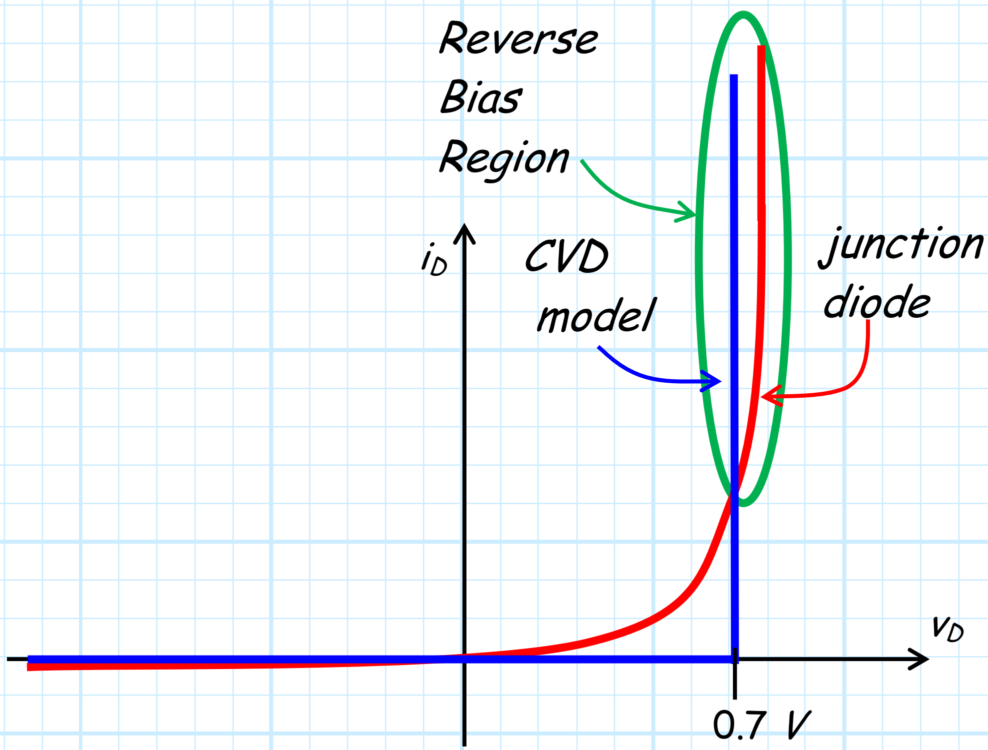
*This numerical result would seem to exhibit a **bunch of error**!*

A: True enough! If we plot **both** the junction diode curve and the CVD model curve, we see that they overlap very well in the **reverse bias region**, meaning the CVD model is **very** accurate **if** the junction diode is operating in that region:



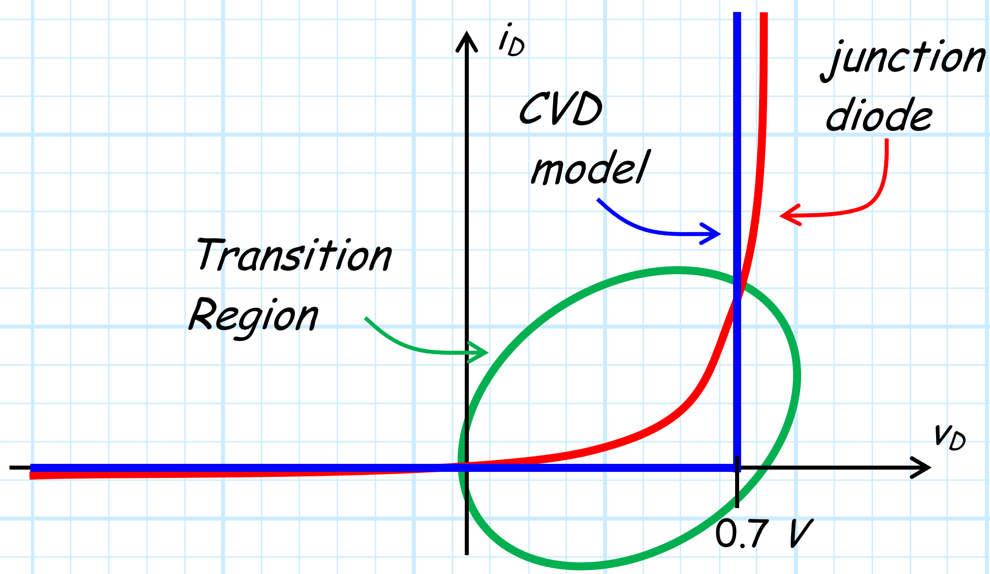
Works reasonably well in the forward bias region

And, the two curves overlap **reasonably well** in the **forward** bias region, meaning the CVD model is **reasonably** accurate **if** the junction diode is operating in that region:



Not so great in the transition region

But, the two curves **diverge significantly** in the **transition** region **between** reverse and forward bias—it is **here** where the approximations provided by the CVD model will typically exhibit the **most** (although often still acceptable) **error**.



No step 4—we're done!

Q: *OK, we're done with **step 3**, what about **step 4**?*

A: There is **no** step 4.

Once we use the results of our ideal diode circuit analysis to **estimate junction diode voltage**:

$$v_D \cong v_D^i + 0.7$$

and **junction diode current**:

$$i_D \cong i_D^i = 0$$

we're **done**!

What about CHECK?

Q: *Hold on!*

The math of the CVD model was ***conditional****; don't you remember:*

$$i_D = 0 \qquad if \qquad v_D < 0.7\ V$$

$$v_D = 0.7\ V \qquad if \qquad i_D > 0$$

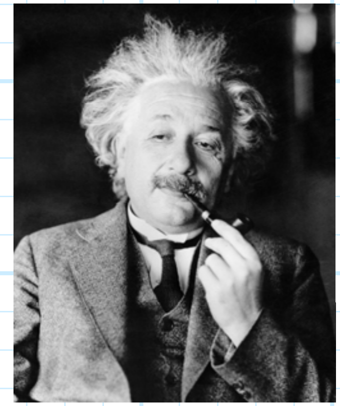
Shouldn't we now ***CHECK*** *these* ***inequalities****?*

A: Recall that we **never assumed** anything about the **junction** diode—thus there is **nothing to CHECK**.

Of course in **step 2**, we had to ASSUME and CHECK something about the **ideal** diode in the CVD circuit model.

But, once we determine for **certain** (in step 2) the ideal diode voltage and current, there are **no more** assumptions to check!

The smart thing to do!



However, it is always **smart** do a **sanity check** on your final answer:

* **If** your junction diode voltage estimate is **less than 0.7** volts, then the junction diode current estimate **must be zero**.

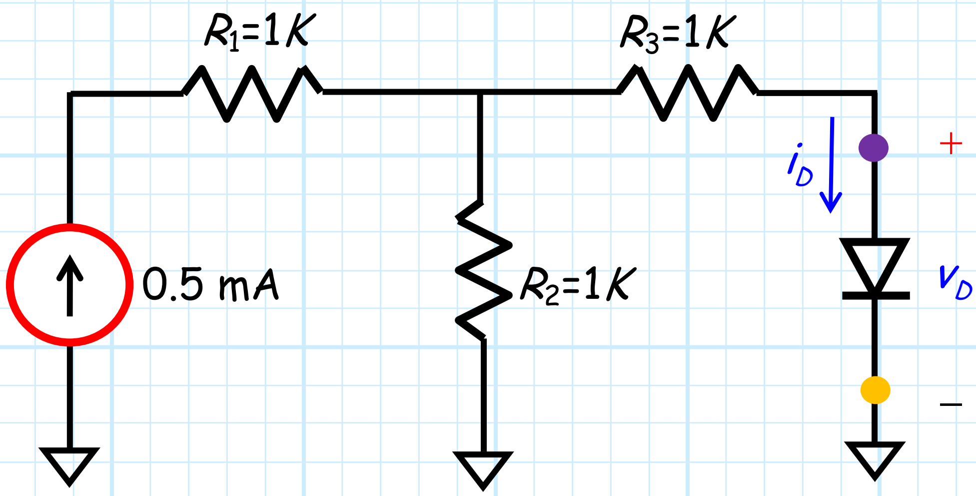
* **If** your junction diode current estimate is **positive**, then the junction diode voltage estimate **must be 0.7 V**.

* Your junction diode voltage estimate can **never** be greater than 0.7 volts, **nor** can your junction diode current estimate ever be **negative**.

If **any** of these statements are not true for your estimates, then you have **simply made a mistake**—go back and correct your error!

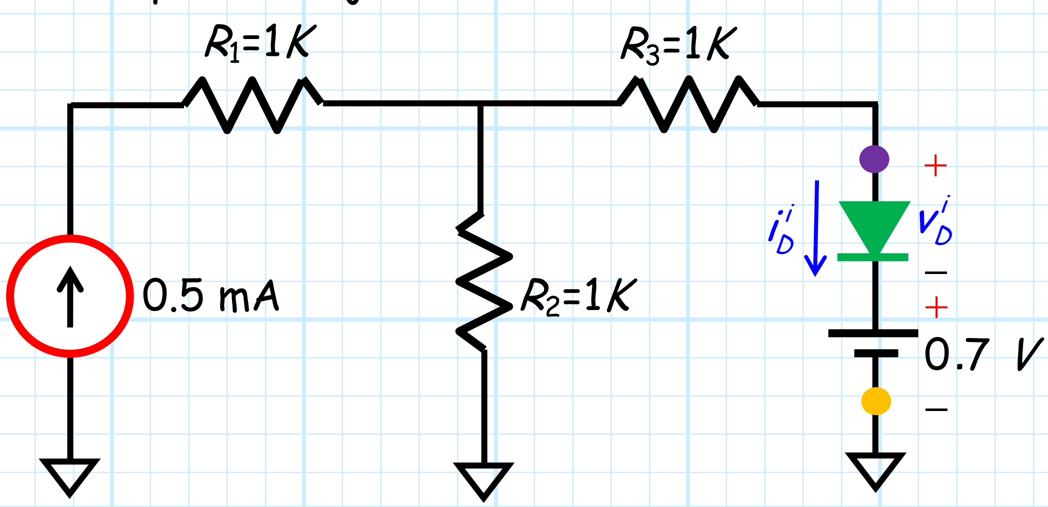
Example: Junction Diode Circuit Analysis with the CVD model

Consider now **this** circuit:



Using the **CVD model**, let's estimate the **voltage** across, and **current** through, the **junction diode**.

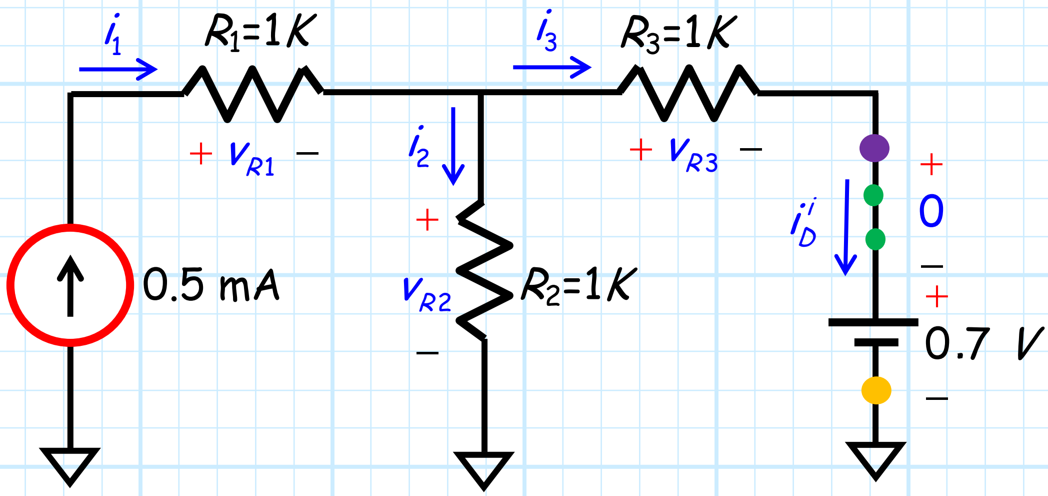
Step 1 is to replace the junction diode with the **CVD model**:



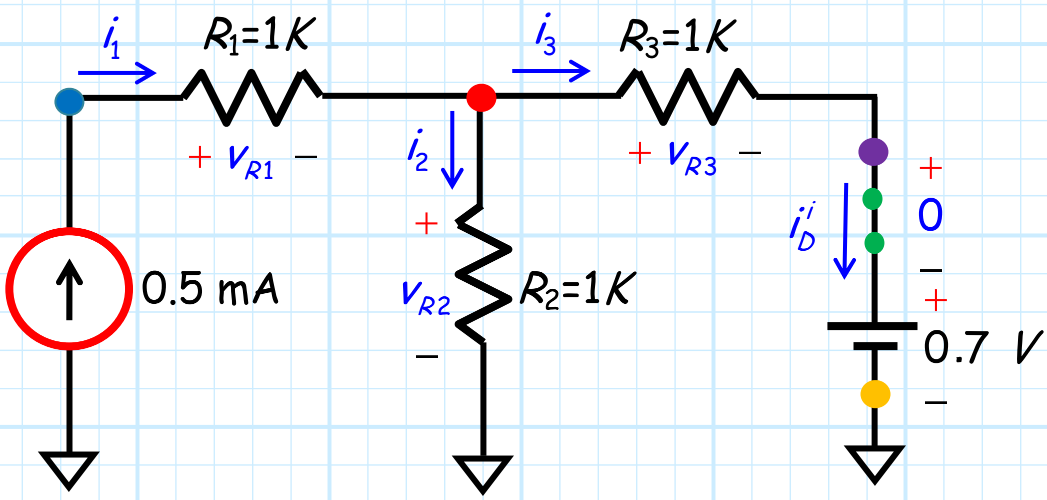
Now we have an **IDEAL** diode circuit, and therefore **Step 2** is to analyze it **precisely** as we did in **section 4.1** !!

ASSUME the **IDEAL** diode is forward biased (why not ?).

ENFORCE the equality condition that $v_D^i = 0.0\,V$ (a **short** circuit).



Now we **ANALYZE** this **IDEAL** diode circuit:



First, from **KCL:**

$$i_1 = 0.5\,mA$$

And a second application of **KCL:**

$$i_2 = i_1 - i_3 = 0.5 - i_3$$

And finally a third dose of **KCL:**

$$i_3 = i_D^i \qquad \therefore \; i_2 = 0.5 - i_3 = 0.5 - i_D^i$$

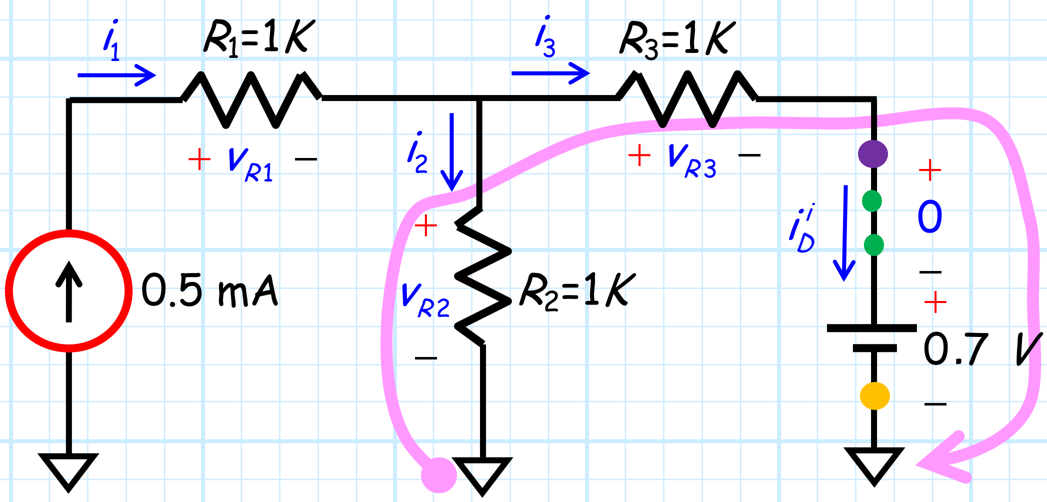
Now, we play the **Ohm's Law** card:

$$v_{R2} = i_2 R_2 = \left(0.5 - i_D^i\right)(1) = 0.5 - i_D^i$$

and

$$v_{R3} = i_3 R_3 = i_D^i(1) = i_D^i$$

And now **KVL**:



$$0 + v_{R2} - v_{R3} - 0 - 0.7 = 0$$

$$\Rightarrow \quad 0.70 = v_{R2} - v_{R3}$$

Combining with the results from Ohm's Law:

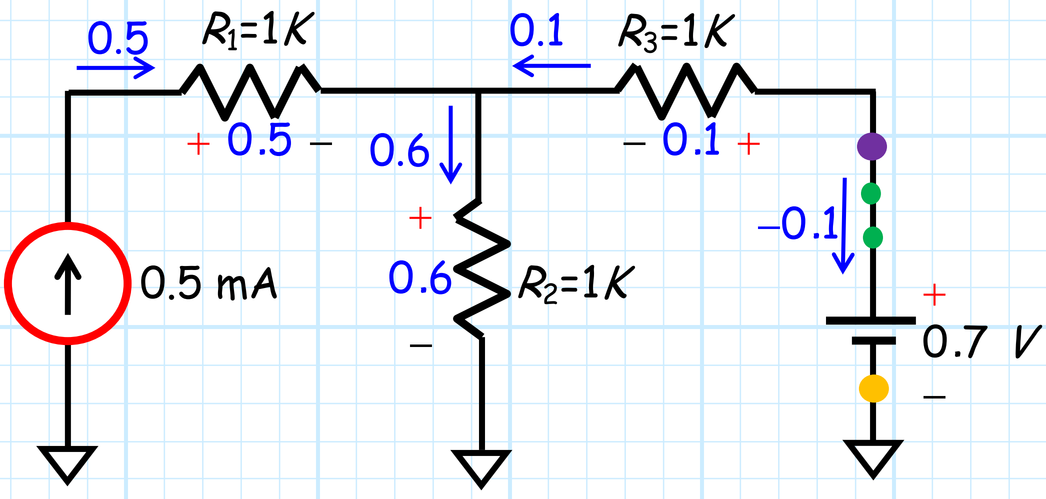
$$0.70 = v_{R2} - v_{R3}$$
$$= \left(0.5 - i_D^i\right) - i_D^i$$
$$= 0.5 - 2i_D^i$$

One equation and **one** unknown (i.e., i_D^i)!

Now solving for **IDEAL** diode current i_D^i:

$$i_D^i = \frac{0.7 - 0.5}{(-2)} = -0.1\ mA$$

Therefore:



Our **ANALYSIS** passes the **sanity** test!

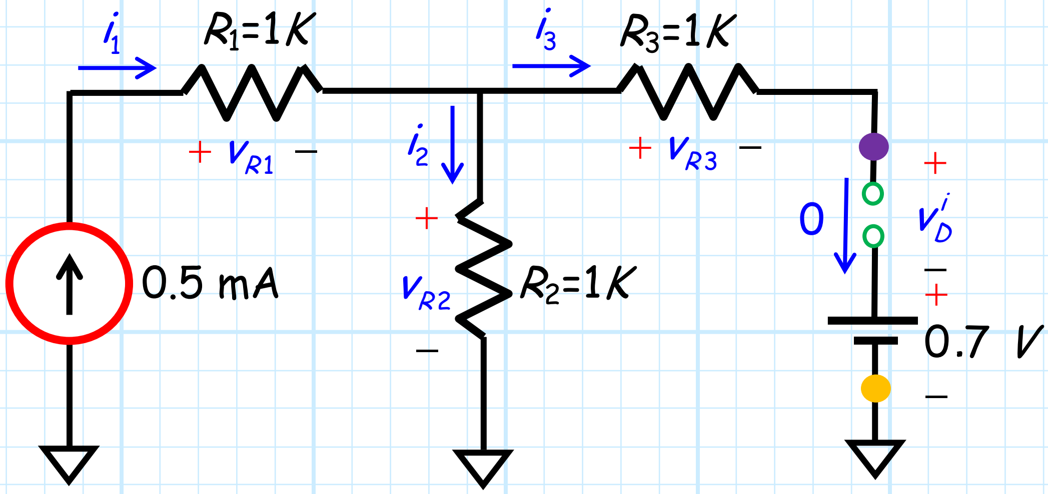
But now, we must **CHECK** the inequality associated with the **IDEAL** diode assumption:

$$i_D^i = -0.1\ mA \overset{?}{>} 0$$

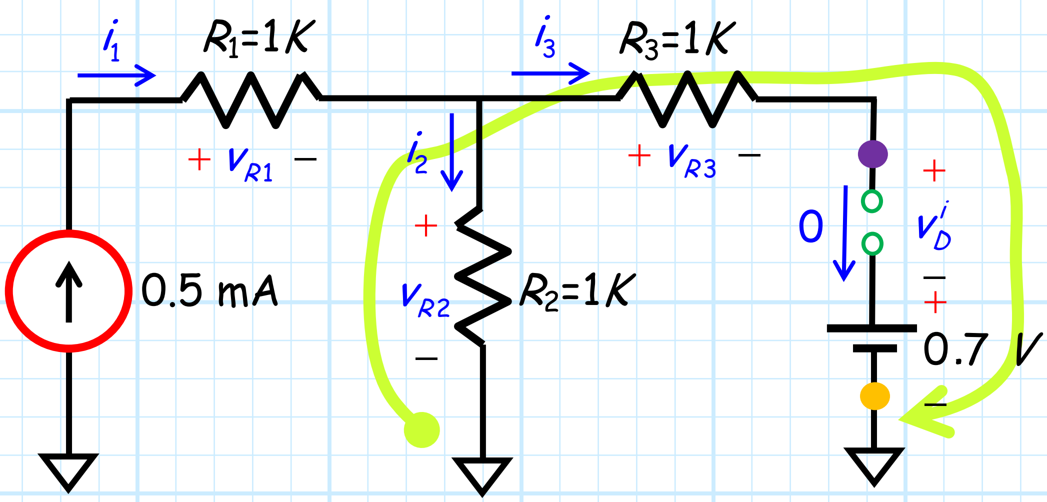
Yikes! We made the **wrong** assumption! Let's **MODIFY** our assumption and try again.

Now **ASSUME** the **IDEAL** diode is **reverse** biased.

ENFORCE the equality that $i_D^i = 0.0$ mA (an **open** circuit).



Now we **ANALYZE** the **IDEAL** diode circuit.



From KVL:

$$0 + v_{R2} - v_{R3} - v_D^i - 0.7 = 0$$

$$\Rightarrow \quad v_D^i = v_{R2} - v_{R3} - 0.7$$

From Ohm's Law:

$$v_{R2} = i_2 R_2 = i_2(1) = i_2$$

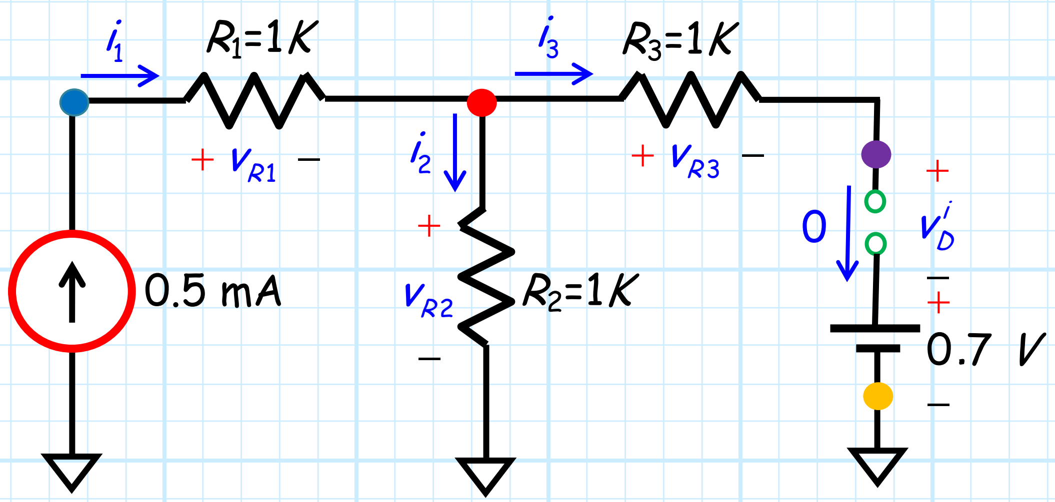
and

$$v_{R3} = i_3 R_3 = i_3(1) = i_3$$

Thus, combining with the KVL result:

$$v_D^i = i_2 - i_3 - 0.7$$

Now for **KCL** !



First, from **KCL**:

$$i_1 = 0.5\, mA$$

And a second application of **KCL**:

$$i_3 = i_D^i = 0$$

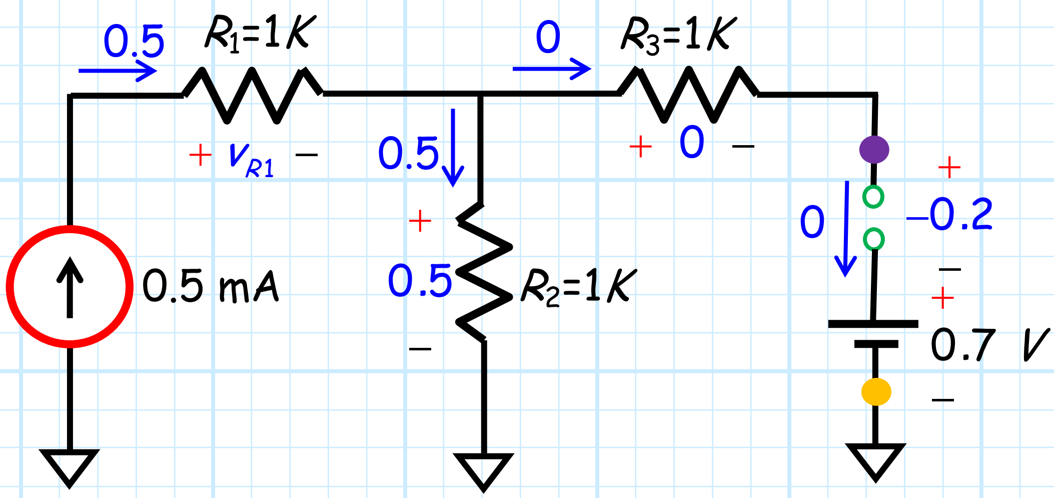
And finally a third dose of **KCL**:

$$i_2 = i_1 - i_3 = 0.5 - 0 = 0.5\ mA$$

Therefore, the **IDEAL** diode voltage is:

$$v_D^i = i_2 - i_3 - 0.7 = 0.5 - 0 - 0.7 = -0.2\ V$$

Now for the **sanity test**:



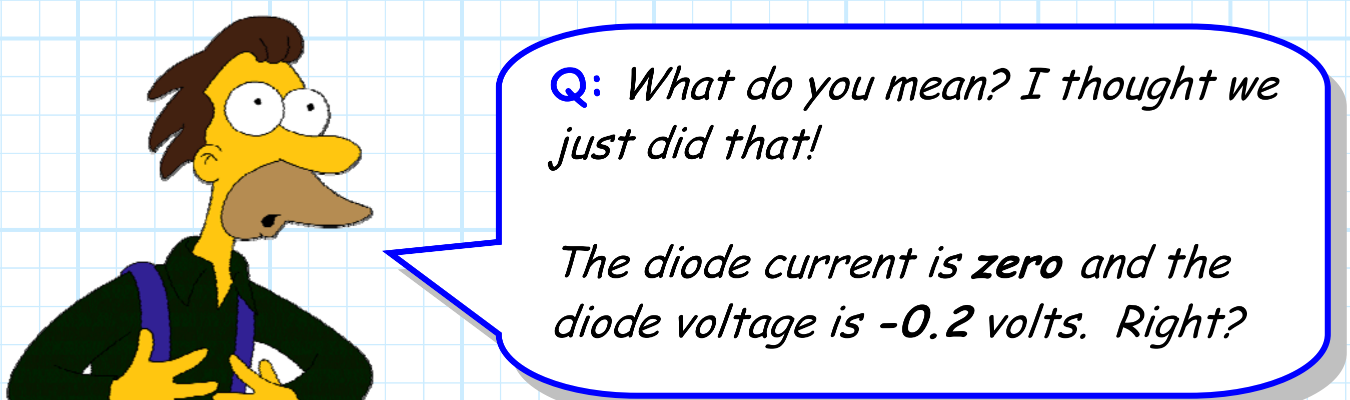
It **passed**!

Now, we **CHECK** to see if our assumption is correct (it better be!):

$$v_D^i = -0.2\ V \overset{?}{<} 0$$

Q: *Great! So we're **all done**?*

A: Holy smokes **no**! We need to find the **approximate** values of the **junction diode voltage** and **junction diode current**.



A: **NO!** We have **only** determined the current and voltage of the **IDEAL** diode voltage in our CVD model. These are **not** the estimated values of the **junction** diode in our circuit!

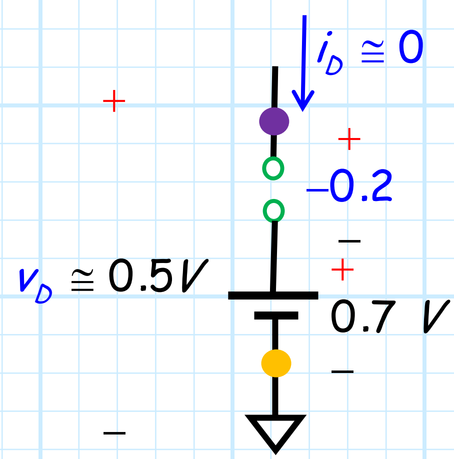
Instead, we estimate the **junction** diode voltage by calculating the voltage across the **entire CVD model** (i.e., ideal diode and 0.7 V source):

$$\begin{aligned} v_D &\cong v_D^i + 0.7 \\ &= -0.2 + 0.7 \\ &= 0.5\ V \end{aligned}$$

We likewise estimate the **current** through the junction diode by determining the current through the **PWL model** (OK, the current through the model is **also** the current through the **ideal** diode):

$$i_D \cong i_D^i = 0$$

Hopefully, this example has convinced you as to the **necessity** of carefully, patiently and precisely applying the junction diode **models**—models that include IDEAL diodes only.



Then, you must use the model results to carefully, patiently and precisely determine **approximate** values for the **junction** diode.

Each and **every** step of this process is **required** to achieve the correct answer—I'll find out **later** in the semester if **you** have been paying attention!

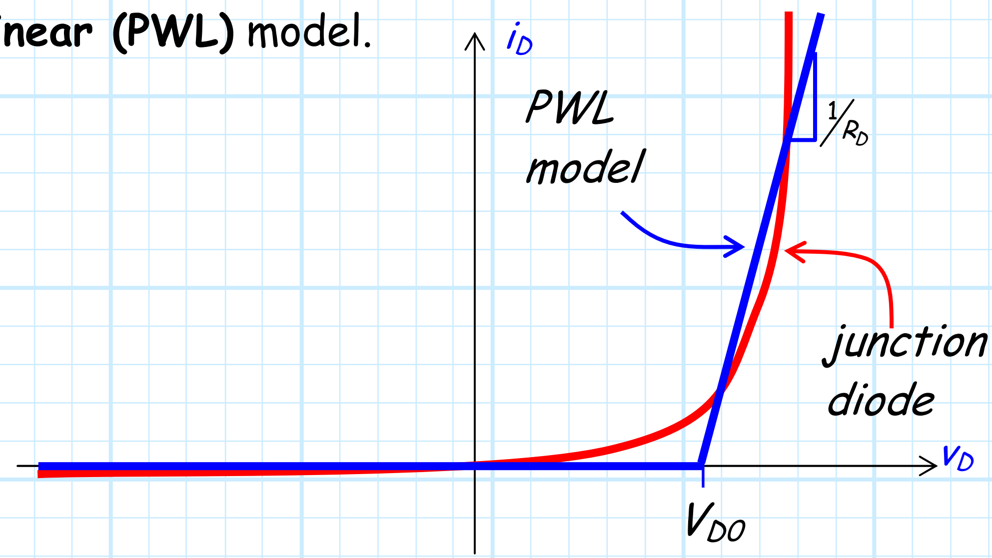
The Piece-Wise Linear Model

Q: *The CVD model approximates the forward biased junction diode voltage as $v_D = 0.7\ V$ regardless of the junction diode current.*

This of course is a good approximation, but in reality, the junction diode voltage ***increases*** *(logarithmically) with increasing diode current.*

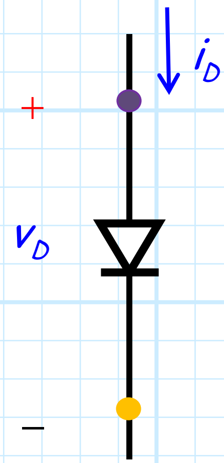
Isn't there a more ***accurate*** *model?*

A: Yes! Consider the **Piece-Wise Linear (PWL)** model.

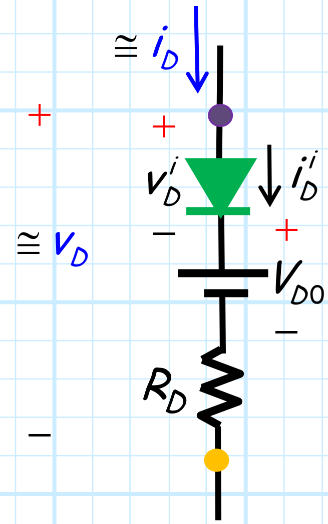


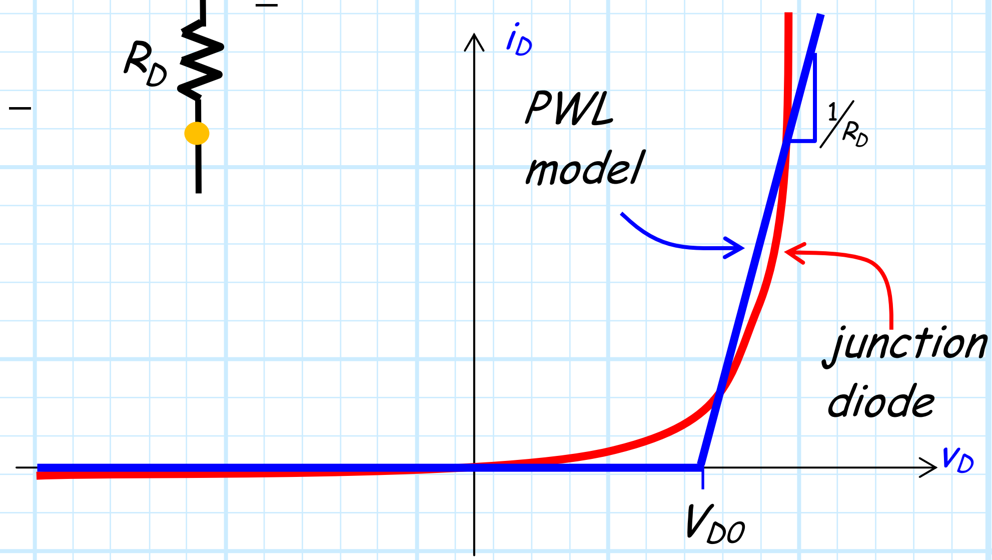
The PWL circuit model

Replace:



with:





In other words, replace the junction diode with **three** devices—an **ideal diode**, in series with some **voltage source** (**not** 0.7 V!) and a **resistor**.

Give me three steps..

To find **approximate** current and voltage values of a **junction** diode circuit, follow these **3 steps**:

Step 1 - **Replace** each junction diode with the **three** devices of the **PWL model**.

Note you now a have an **IDEAL** diode circuit! There are **no junction diodes** in the circuit, and therefore **no junction diode** knowledge need be (or should be) used to analyze it.

Step 2 - Now **analyze** the **IDEAL** diode circuit on your paper. Determine i_D^i and v_D^i for **each ideal** diode.

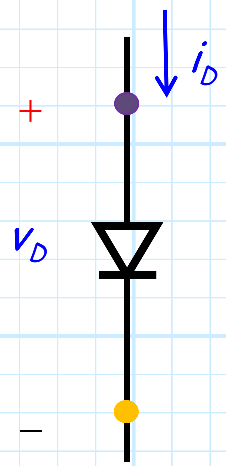
IMPORTANT NOTE!!! PLEASE READ THIS CAREFULLY:

Make sure you analyze the resulting circuit **precisely** as we did in section 4.1.

You **assume** the same **IDEAL** diode modes, you **enforce** the same **IDEAL** diode values, and you **check** the same **IDEAL** diode results, **precisely** as before. Once we replace the junction diodes with the PWL model, we have an **IDEAL** diode circuit—**no junction diodes** are involved!

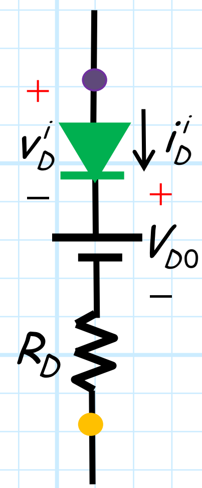
Step 3 gives the *approximate* answer

Step 3 - Determine the **approximate** values i_D and v_D of the **junction** diode from the **IDEAL** diode values i_D^i and v_D^i:



$$i_D \cong i_D^i$$

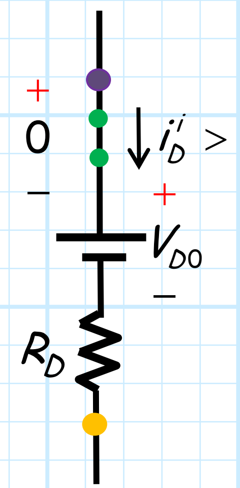
$$v_D \cong v_D^i + V_{D0} + i_D^i R_D$$



The PWL model when the *ideal* diode is forward biased

Note therefore, **if** the **IDEAL** diode (note here I said **IDEAL** diode) is **forward** biased ($i_D^i > 0$), then the **approximation** of the **junction** diode current will likewise be positive ($i_D > 0$), and the **approximation** of the **junction** diode voltage (unlike the **ideal** diode voltage of $v_D^i = 0$) will be:

$$
\begin{aligned}
v_D &= v_D^i + V_{D0} + i_D^i r_d \\
&= 0.0 + V_{D0} + i_D^i r_d \\
&= V_{D0} + i_D^i R_D
\end{aligned}
$$



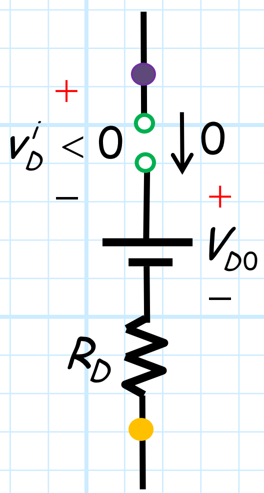
Thus, it is apparent that if the **IDEAL** diode is **forward** biased ($i_D^i > 0$), then the **junction** diode voltage **estimate** must be greater than voltage source V_{D0}:

$$v_D = V_{D0} + i_D^i R_D > V_{D0}$$

The PWL model when the *ideal* diode is reverse biased

However, **if** the **IDEAL** diode is **reversed** biased ($i_D^i = 0$), then the **approximation** of the **junction** diode current will likewise be zero ($i_D \cong 0$), and the approximation of the junction diode voltage (unlike the **ideal** diode voltage of $v_D^i < 0$) will be:

$$
\begin{aligned}
v_D &= v_D^i + V_{D0} + i_D^i R_D \\
&= v_D^i + V_{D0} + 0 \\
&= v_D^i + V_{D0}
\end{aligned}
$$



Thus, it is apparent that if the **IDEAL** diode is **reverse** biased ($v_D^i < 0$), then the **junction** diode voltage **estimate** must be greater than voltage source V_{D0}:

$$v_D = v_D^i + V_{D0} < V_{D0}$$

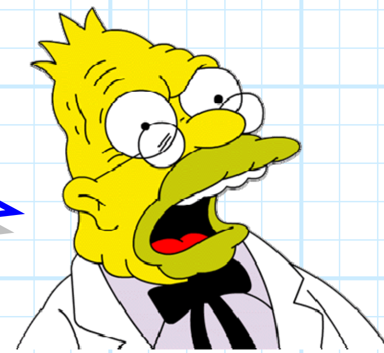
NOTE: Do **not** check the resulting **junction** diode approximations.

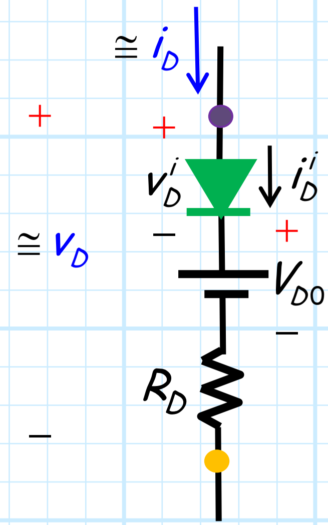
You do **not** assume anything about the **junction** diode, so there is **nothing** to check regarding the junction diode answers.

Constructing the PWL Junction Diode Model

Q: *Wait a minute! How the heck are we supposed to use the **PWL model** to analyze junction diode circuits?*

***You** have yet to tell us the numeric **values** of voltage source V_{DO} and resistor R_D !*





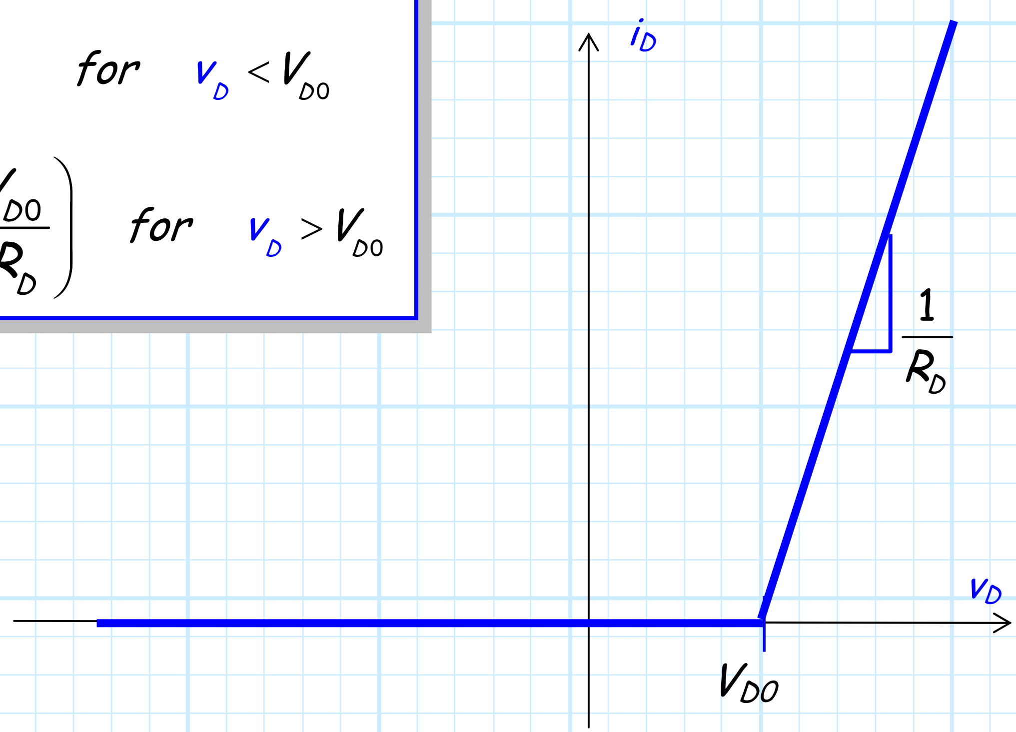
A: That's right!

The reason is that the **proper** values of voltage source V_{DO} and resistor R_D are up to **you** to determine!

The PWL circuit model

To see why it is up to you to determine, consider the current voltage relationship of the **PWL model**:

$$i_D = \begin{cases} 0 & \text{for} \quad v_D < V_{D0} \\ \left(\dfrac{1}{R_D}\right) v_D - \left(\dfrac{V_{D0}}{R_D}\right) & \text{for} \quad v_D > V_{D0} \end{cases}$$



em ex plus bee

Note that when the **ideal** diode in the PWL model is forward biased, the current-voltage relationship is simply the equation of a **line**!

$$i_D = \left(\frac{1}{R_D}\right) v_D - \left(\frac{V_{D0}}{R_D}\right)$$

$$\boxed{y} = \boxed{m}\ \boxed{x} + \boxed{b}$$

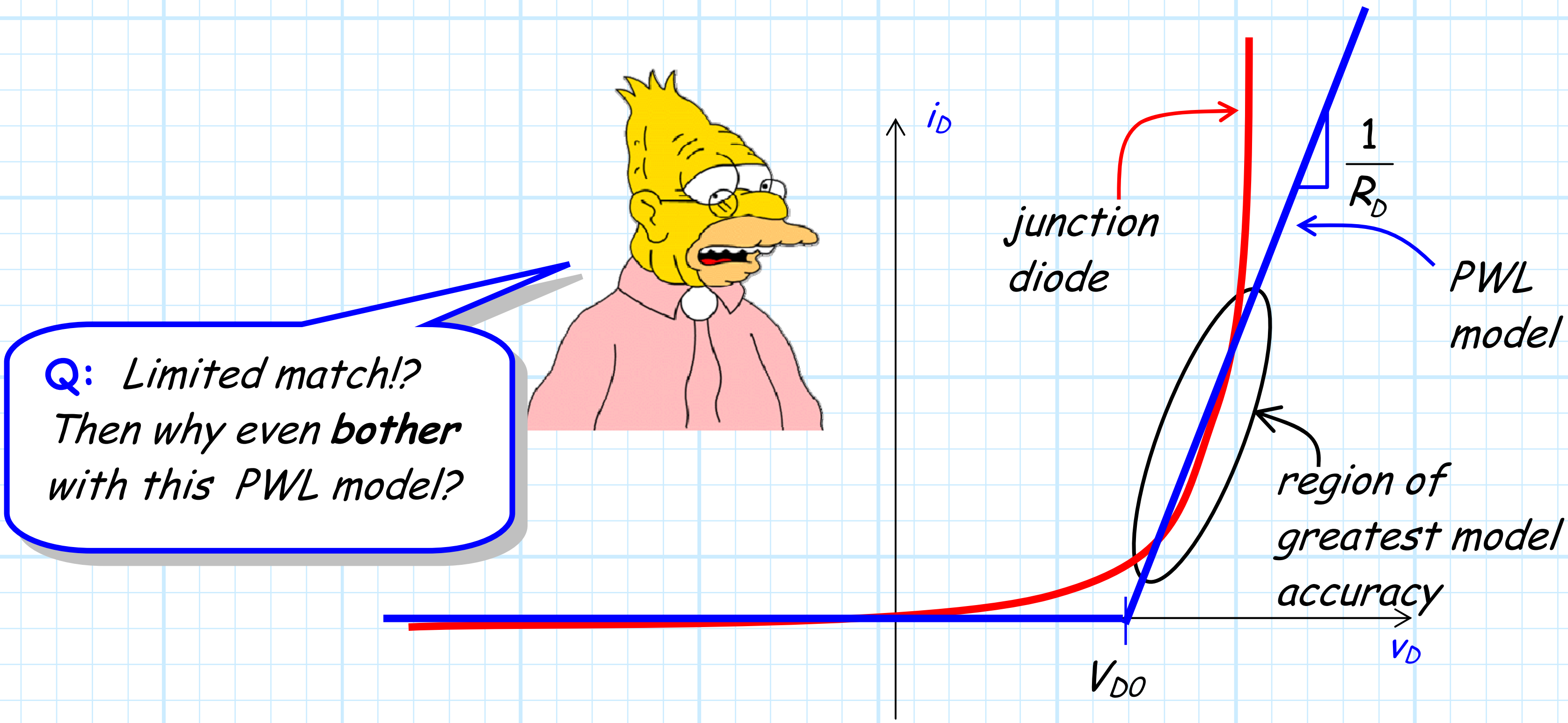
Compare the above to the forward biased junction diode approximation:

$$i_D = I_s e^{v_D / nV_T}$$

An **exponential** equation!

An exponential is not a line!

An exponential function and the equation of a line are **very** different—the two functions can approximately "match" only over a **limited** region:



A: Remember, the PWL model is **more accurate** than our two **alternatives**—the ideal diode model and the CVD model.

At the very least, the PWL model (**unlike** the two alternatives) shows an **increasing** voltage v_D with **increasing** i_D.

Four ways to construct the PWL model

Moreover, **if** we select the values of V_{D0} and R_D properly, the PWL can **very** accurately "match" the actual (exponential) junction diode curve over a **decade** or more of current (e.g., accurate from $i_D = 1mA$ to $10mA$, or from $i_D = 20mA$ to $200mA$).

Q: *Yes well I asked you a long time ago what R_D and V_{D0} should be, but you **still** have not given me an **answer**!*

A: OK. We now know that the values of R_D and V_{D0} specify a **line**. We also know there are **4** potential ways to **specify** a line:

1. Specify **two points** on the line.
2. Specify one **point** on the line, as well as its **slope** m.
3. Specify one **point** on the line, as well as its ***y*-intercept** b.
4. Specify both its **slope** and its ***y*-intercept** b.

We will find that the **first two** methods are the most useful. Let's address them one at a time.

Method 1: Specify two points on the line

The **obvious** question here is: **Which** two points ?

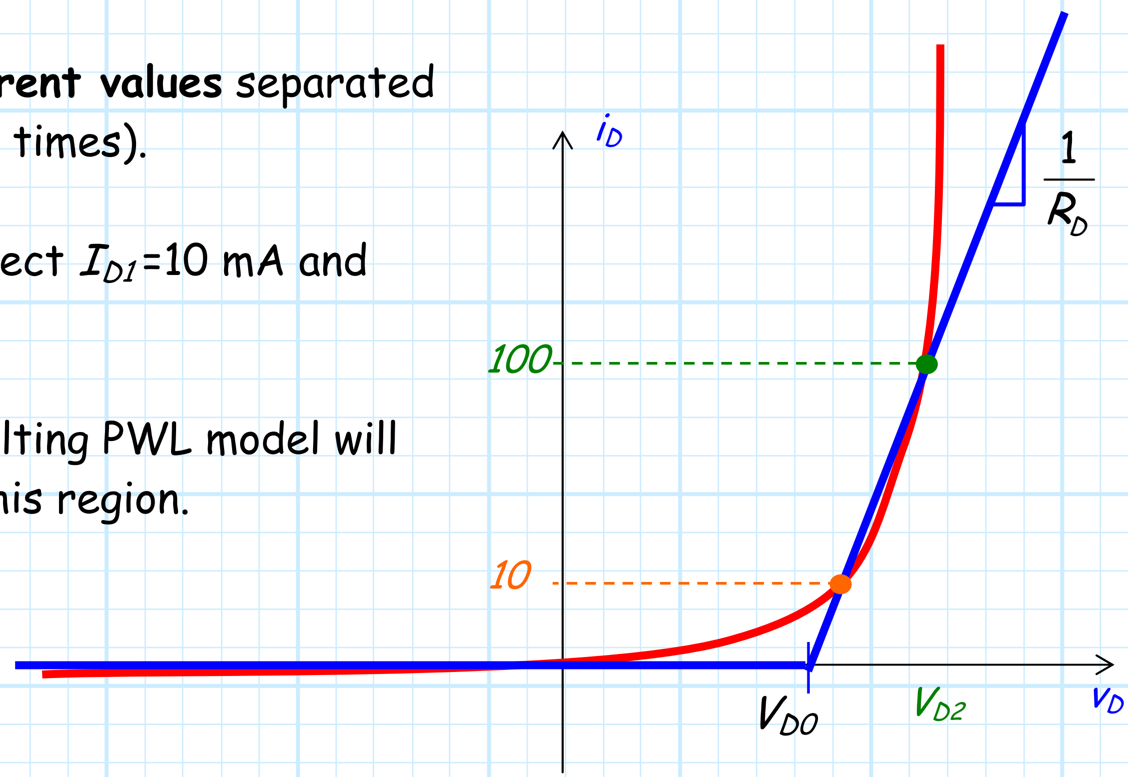
Q: *Which two points?*

A: Hopefully it is **equally** obvious that the two points should be points lying on the **junction diode** exponential curve (after all, it is **this curve** that we are **attempting to approximate**!).

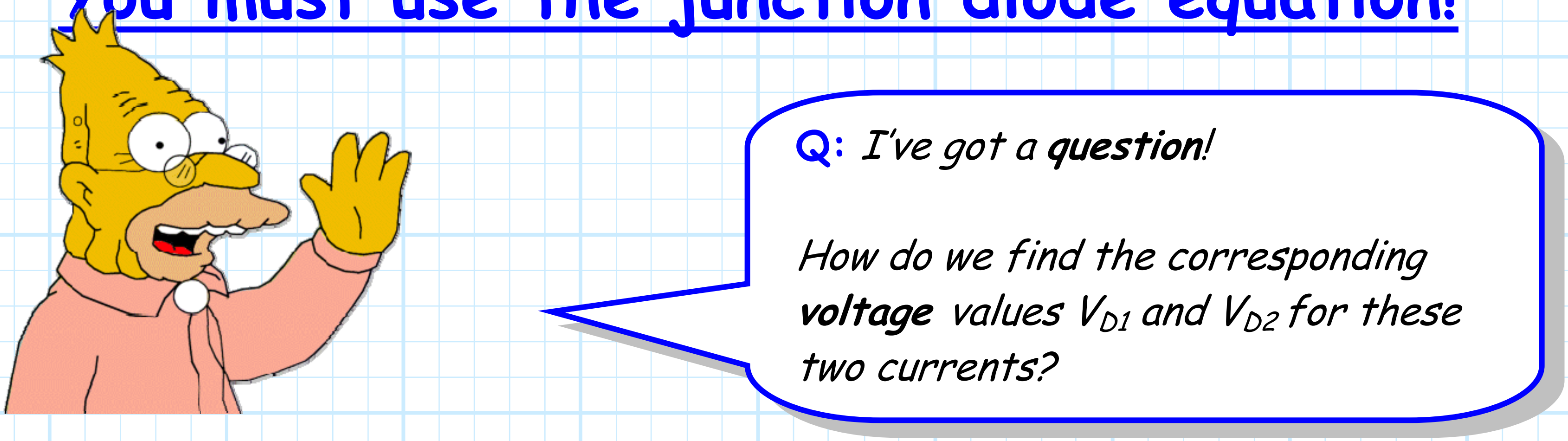
Typically, we pick **two current values** separated by about a **decade** (i.e., 10 times).

For **example**, we might select I_{D1}=10 mA and I_{D2} =100 mA.

We will find that the resulting PWL model will be **fairly accurate** over this region.



You must use the junction diode equation!



A: Remember, we are selecting two points **on** the exponential junction diode curve.

Thus, we can use the **junction diode equation** to determine the corresponding voltages:

$$v_{D1} = nV_T \ln\left[\frac{I_{D1}}{I_s}\right] \quad \text{and} \quad v_{D2} = nV_T \ln\left[\frac{I_{D2}}{I_s}\right]$$

Or, if the diode manufacturer provides us with a **test point** instead of scale current *Is* :

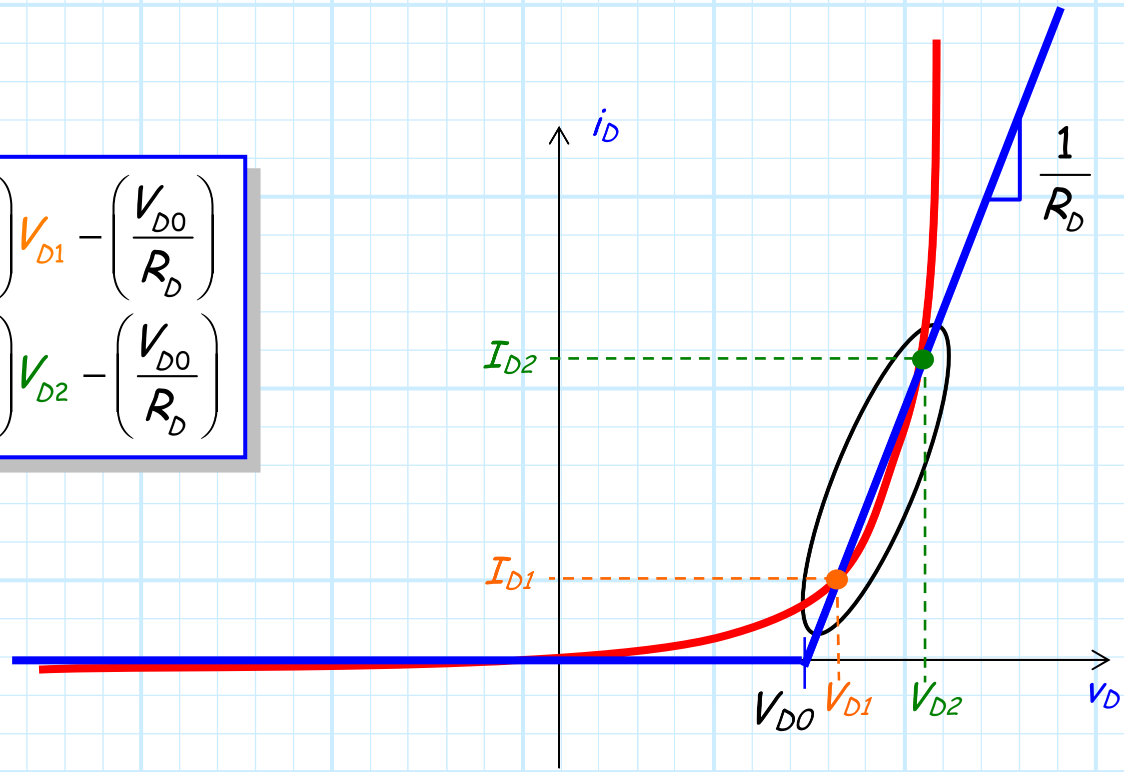
$$V_{D1} = V_{test} + nV_T \ln\left(\frac{I_{D1}}{I_{test}}\right) \quad \text{and} \quad V_{D2} = V_{test} + nV_T \ln\left(\frac{I_{D2}}{I_{test}}\right)$$

This should bring back fond memories

Now, the rest is simply **Middle School mathematics**. If our PWL "line" intersects these two points, then:

$$I_{D1} = \left(\frac{1}{R_D}\right) V_{D1} - \left(\frac{V_{D0}}{R_D}\right)$$

$$I_{D2} = \left(\frac{1}{R_D}\right) V_{D2} - \left(\frac{V_{D0}}{R_D}\right)$$



Thus, we can solve the above **two equations** to determine the **two unknown** values of V_{D0} and R_D, such that our PWL "line" will intersect the two specified points on the junction diode curve.

Middle school math

The **slope** of the line is:

$$m = \frac{1}{R_D} = \frac{I_{D2} - I_{D1}}{V_{D2} - V_{D1}}$$

$$\therefore \quad R_D = \frac{V_{D2} - V_{D1}}{I_{D2} - I_{D1}}$$

And then we use our PWL "line" equation to find V_{D0}:

$$V_{D0} = v_{D1} - i_{D1} R_D r_d \qquad or \qquad V_{D0} = v_{D2} - i_{D2} R_D r_d$$

(note these two equations are **KVL**!).

Method 2: specify one point and the slope he PWL circuit model

Now let's examine **another** way of constructing our PWL model.

We first specify just **one** point that the PWL "line" must intersect.

Let's denote this point as (I_D, V_D) and call this point our **bias point**.

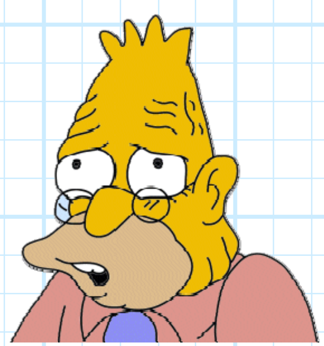
Of course, we want our bias point to **lie on** the exponential junction diode curve, i.e.:

$$I_D = I_s e^{V_D / nV_T} \quad \text{or equivalently} \quad V_D = nV_T \ln\left[\frac{I_D}{I_s}\right]$$

Now, **instead** of specifying a **second** intersection point, we merely **specify directly** the PWL line **slope** (i.e., directly specify the value of R_D!):

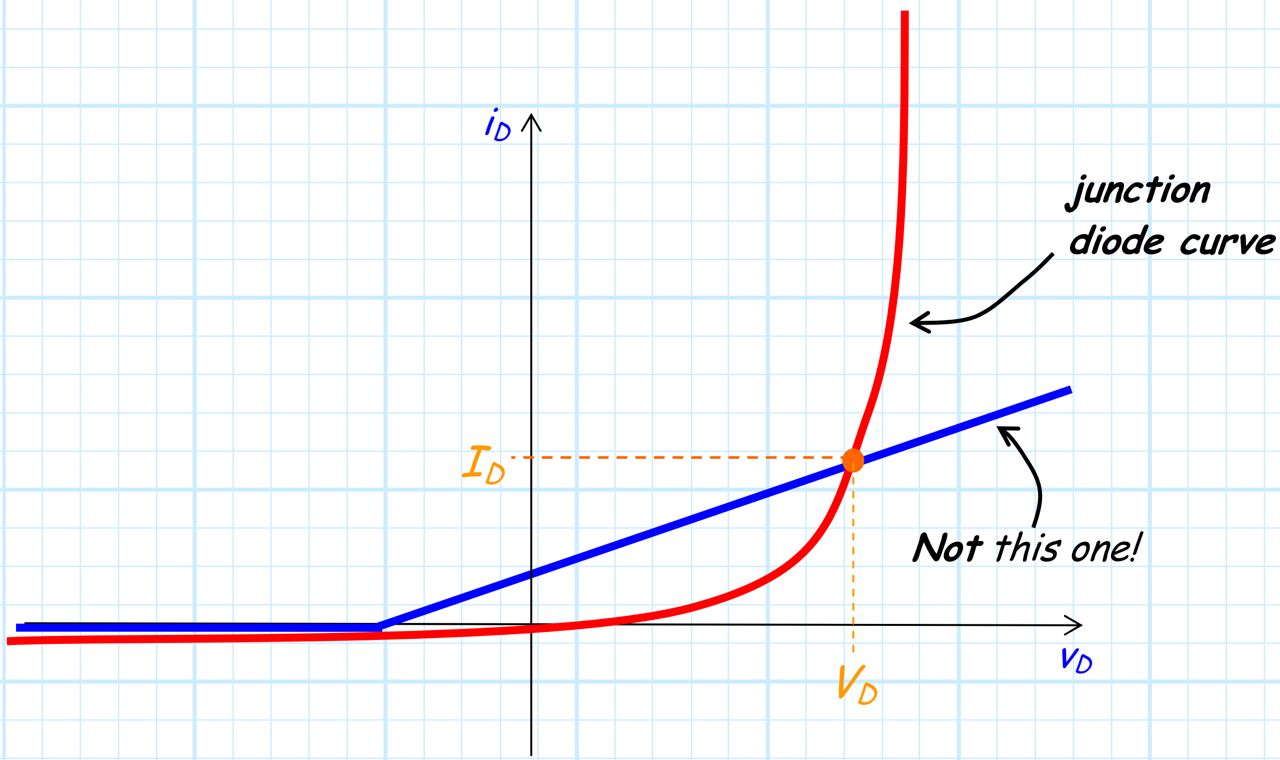
$$m = \frac{1}{R_D}$$

Q: *But I have **no idea** what the value of this slope should be!?!*



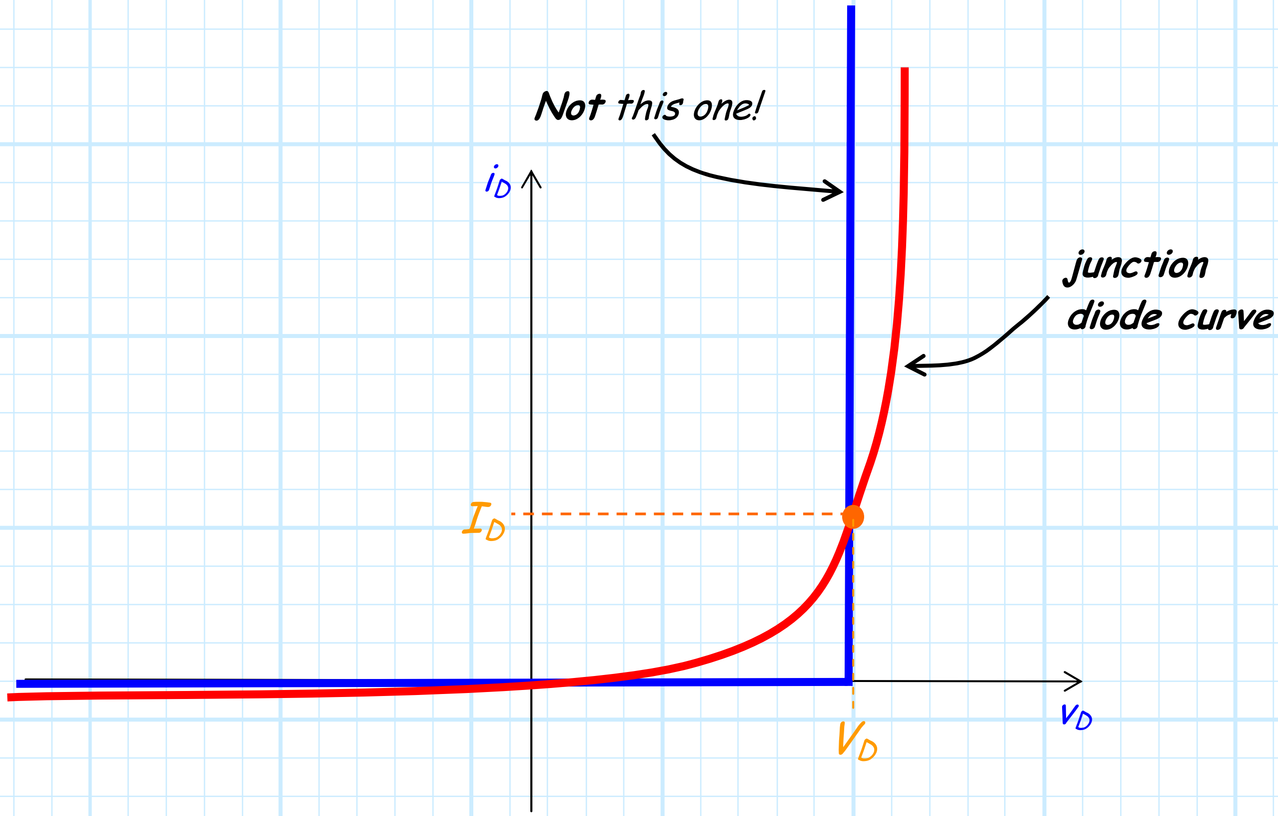
This slope is too low

A1: Not **this** PWL model!



This slope is too high

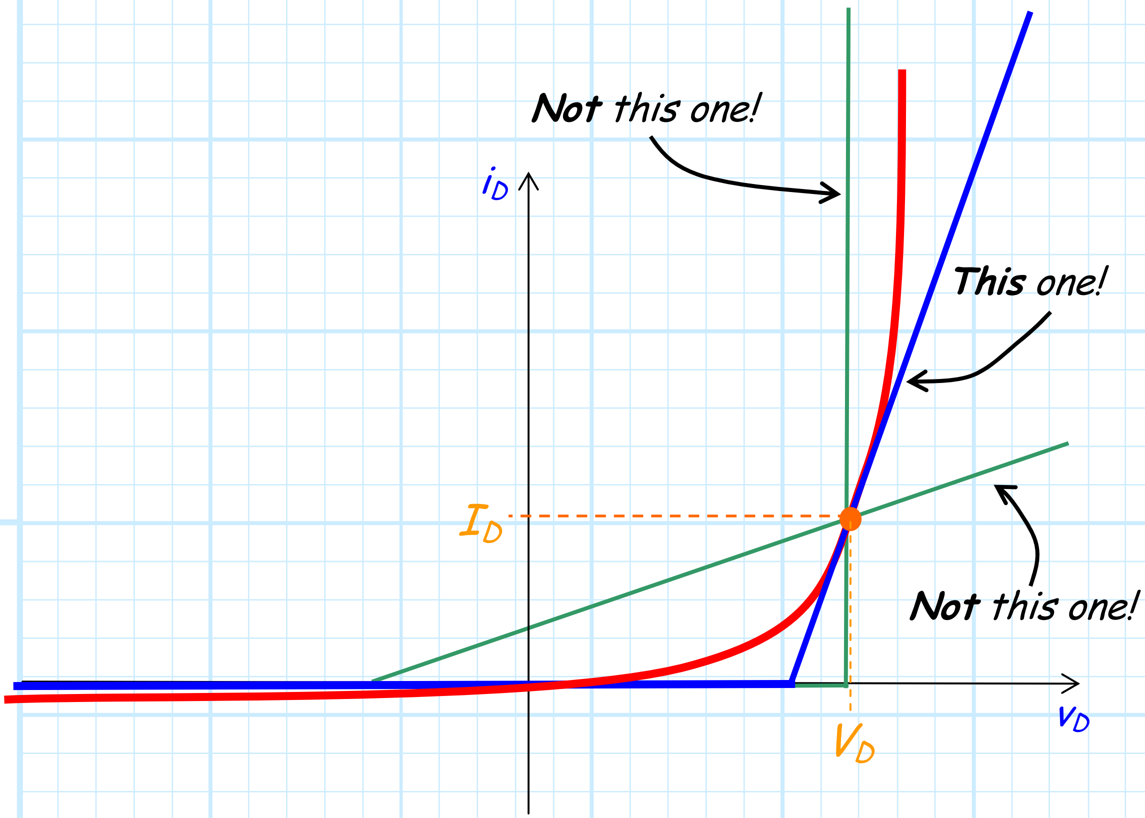
A2: Not **this** PWL model either.

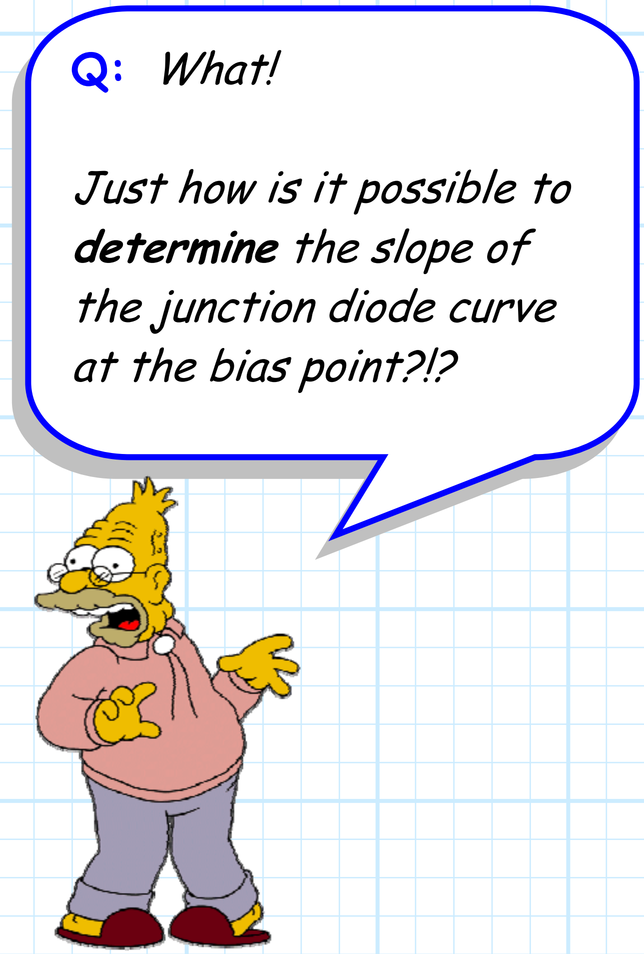


This slope is just right!

A3: Think about it.

Of all possible PWL models that intersect the bias point, the one that is most accurate is the one that has a slope **equal** to the slope of the exponential junction diode curve (that is, **at** the bias point)!





Nutin' funner than calculus!

A: Easy! We simply take the **first derivative** of the junction diode equation:

$$\frac{d\,i_D}{d\,v_D} = \frac{d}{d\,v_D}\left(I_s e^{v_D / nV_T} \right)$$

$$= \frac{I_s e^{v_D / nV_T}}{nV_T}$$

Q: *Of course!*

Isn't this ***equation*** *is the slope of the junction diode curve at the bias point?*

A: Actually **no**. The above equation is **not** the slope of the junction diode curve at the bias point.

This equation provides the slope of the curve **as a function diode voltage** v_D.

The slope of the junction diode curve is in fact different at **every** point on the junction diode curve.

Number—we need a number

In fact, as the equation above clearly states, the slope of the junction diode curve **exponential increases** with increasing v_D!

Q: *Yikes! So* ***what*** *is the derivate equation* ***good*** *for?*

A: Remember, we are interested in the value of the slope of the curve at **one** particular point—the **bias point**.

Thus, we simply **evaluate** the derivative function at that point.

The result is a numeric value of the slope **at our bias point**!

$$m = \frac{d}{d\,v_D}\left(I_s e^{v_D / nV_T} \right)\Bigg|_{v_D = V_D}$$

$$= \frac{I_s e^{v_D / nV_T}}{nV_T}\Bigg|_{v_D = V_D}$$

$$= \frac{I_s e^{V_D / nV_T}}{nV_T}$$

Pretty darn simple

Note the **numerator** of this result!

We recognize this numerator as simply the value of the **bias current** I_D:

$$I_D = I_s e^{V_D / nV_T}$$

Therefore, we find that the **slope** at the bias point is:

$$m = \frac{I_s e^{V_D / nV_T}}{nV_T} = \frac{I_D}{nV_T}$$

Now, we want the slope of our **PWL model** line to be **equal** to the slope of the **junction diode curve** at our bias point.

Therefore, we desire:

$$\frac{1}{R_D} = m = \frac{I_D}{nV_T}$$

The small-signal PWL model

Thus, **rearranging** this equation, we find that the PWL model **resistor value** should be:

$$R_D = \frac{nV_T}{I_D}$$

We likewise can rearrange the PWL "line" equation to determine the value of the **model voltage source** V_{D0}:

$$V_{D0} = V_D - I_D R_D \qquad \textbf{(KVL !)}$$

Now, combining the previous two equations, we find:

$$\begin{aligned} V_{D0} &= V_D - I_D R_D \\ &= V_D - I_D \left(\frac{nV_T}{I_D} \right) \\ &= V_D - nV_T \end{aligned}$$

In summary

So, let's **recap** what we have learned about constructing a PWL model using this particular approach.

1. We first select a single **bias point** (I_D, V_D), a point that lies on the junction diode curve, i.e.:

$$I_D = I_s e^{V_D / nV_T}$$

2. Using the current and voltage values of this bias point, we can then determine **directly** the PWL model **resistor value**:

$$\boxed{R_D = \frac{nV_T}{I_D}}$$

We'll use this later

3. We can also directly determine the **value** of the model **voltage source**:

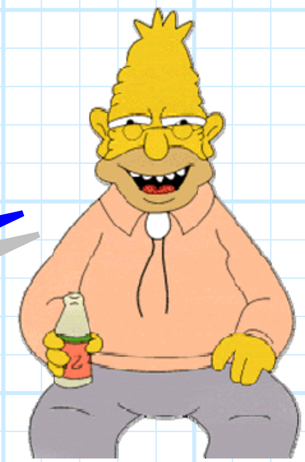
$$V_{D0} = V_D - nV_T$$

This method for constructing a ***PWL model*** produces a very ***precise*** match over a relatively ***small region*** of the junction diode curve.

*We will find that this is **very useful** for many practical diode circuit problems and analysis!*

*This PWL model produced by this last method (as described by the equations of the previous page) is called the junction diode **small-signal model**.*

*We will use the **small-signal model** again—make sure that **you** know **what** it is and **how** we construct it!*



Example: Constructing a PWL Model

We **measured** a certain **junction** diode in our lab, and determined that the current through this diode is:

$$i_D = 10 \text{ mA} \quad \text{when} \quad v_D = 0.7 \text{ V}$$

and

$$i_D = 1 \text{ mA} \quad \text{when} \quad v_D = 0.6 \text{ V}$$

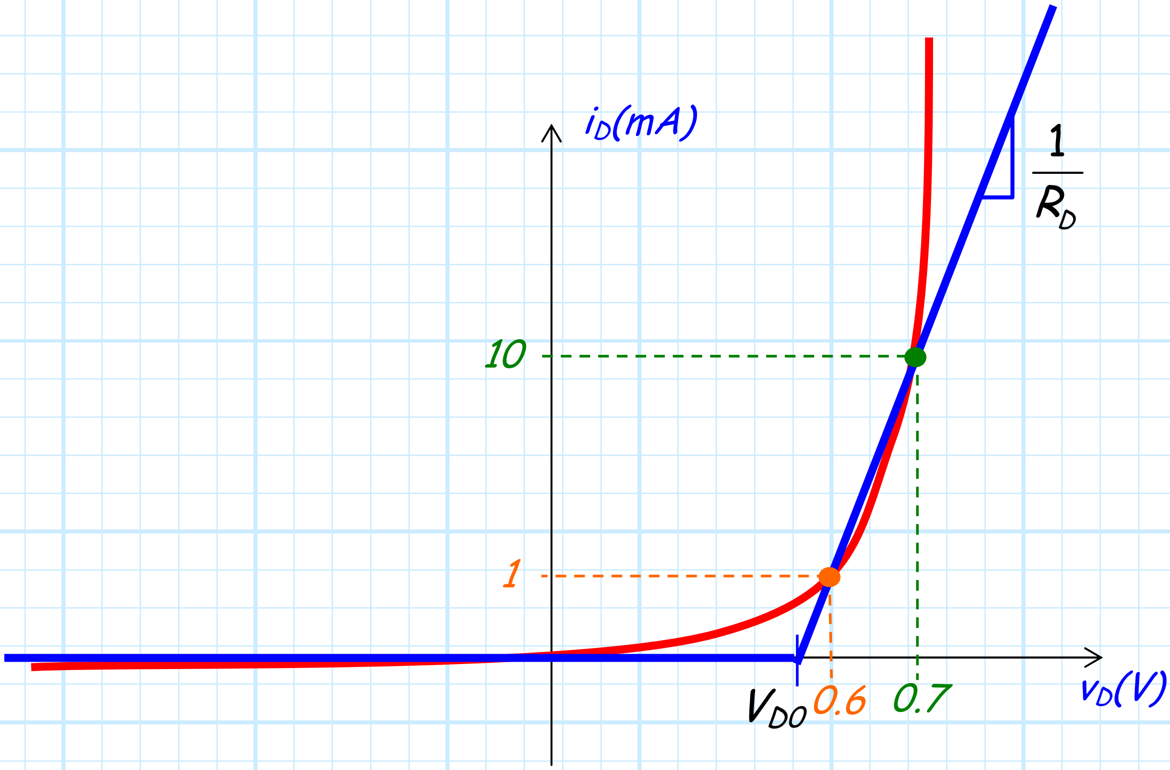
Say we wish to **construct a PWL model** that will approximate this particular **junction** diode.

We want this PWL mode to be particularly accurate for diode currents from, say, approximately **1 mA** to about **10 mA**.

Recall that the resulting model will relate **junction** diode voltage v_D to **junction** diode current i_D as a **line** of the form:

$$i_D = \left(\frac{1}{r_d}\right) v_D - \left(\frac{V_{D0}}{r_d}\right)$$

We therefore need to determine the values of V_{D0} and R_D such that this PWL model "line" will **intersect** the two points I_{D1} = 1.0 mA, V_{D1} = 0.6 V and I_{D2} = 10.0 mA, V_{D2} = 0.7 V.



The **slope** of this line must therefore be:

$$m = \frac{I_{D2} - I_{D1}}{V_{D2} - V_{D1}} = \frac{10 - 1}{0.7 - 0.6} = \frac{9}{0.1} = 90 \quad K\,mhos$$

Thus our PWL model **resistor value** R_D must be:

$$R_D = \frac{1}{m} = \frac{0.1}{9} = 0.0111\ K$$

Or in other words, $R_D = 11.1\ \Omega$.

Q: *Wow! That's a **very small** resistance value. Are you **sure** we calculated R_D correctly?*

A: Typically, we find that the resistor value in the PWL model **is** small. In fact, it is frequently **less than 1 Ω** when we attempt to match the junction diode curve in a "high" current region (e.g., from i_D=50 mA to i_D=500 mA).

Now that we have determined R_D, we can insert **either** point into the model **line equation** and solve for V_{D0}. For example, the equations:

$$I_{D1} = \left(\frac{1}{R_D}\right)V_{D1} - \left(\frac{V_{D0}}{R_D}\right) \quad \text{or} \quad I_{D2} = \left(\frac{1}{R_D}\right)V_{D2} - \left(\frac{V_{D0}}{R_D}\right)$$

become either:

$$\begin{aligned} V_{D0} &= V_{D1} - I_{D1} R_D \\ &= 0.6 - 1(0.0111) \\ &= 0.589 \text{ V} \end{aligned}$$

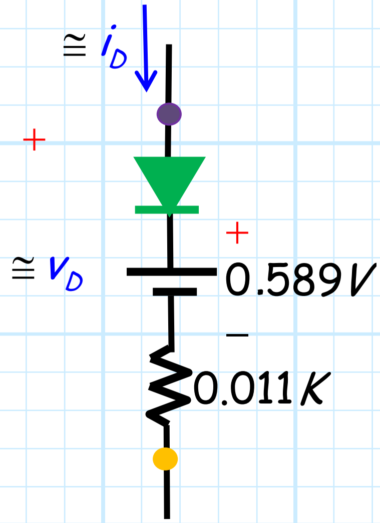
or

$$\begin{aligned} V_{D0} &= V_{D2} - I_{D2} R_D \\ &= 0.7 - 10(0.0111) \\ &= 0.589 \text{ V} \end{aligned}$$

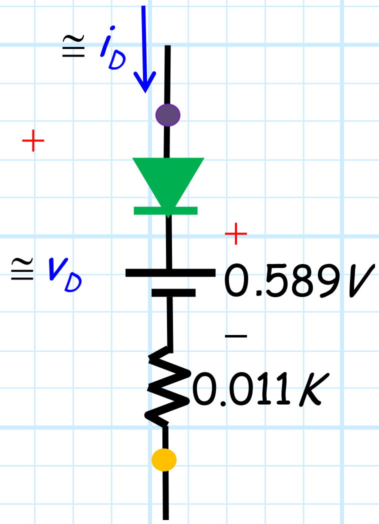
In other words, we can use **either** point to determine V_{D0}.

Our **PWL model** is therefore:

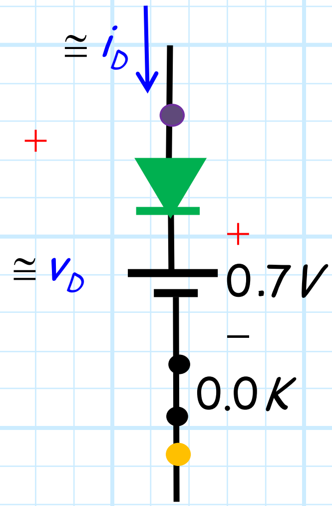
$$i_D = \begin{cases} 0 & \text{for} \quad v_D < 0.589\,V \\ \dfrac{v_D}{0.0111} - \dfrac{0.589}{0.0111} \; mA & \text{for} \quad v_D > 0.589\,V \end{cases}$$



Now, **compare** this PWL model to the CVD model:



PWL



CVD

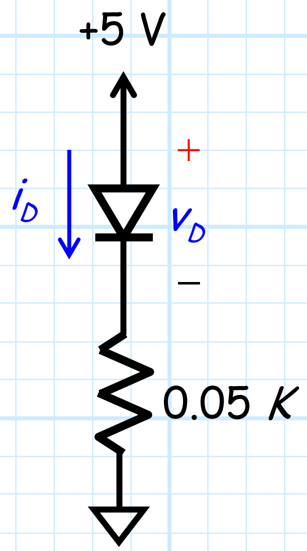
Note that the **CVD** model can be viewed as a PWL model with V_{D0}= 0.7 V and zero resistance $R_D = 0$. **Compare** those values with our model (V_{D0}= 0.589 V and $R_D = 11.1\Omega$)—**not** much difference!

Thus, the PWL model is **not** a radical departure from the CVD model (typically V_{DO} is close to 0.7 V and r_d is **very** small).

Instead, the PWL can be view as **slight improvement** of the CVD model.

Example: Junction Diode Models

Consider the **junction** diode circuit, where the junction diode has device parameters $I_S = 10^{-9}\ mA$, and $n = 1$:



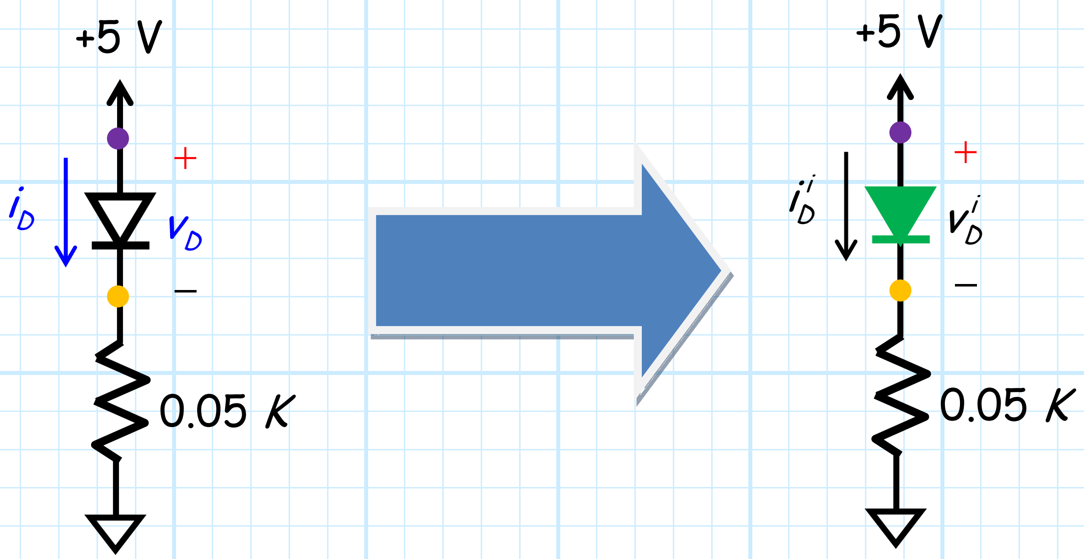
I **numerically** solved the resulting transcendental equation, and determined the **exact** solution:

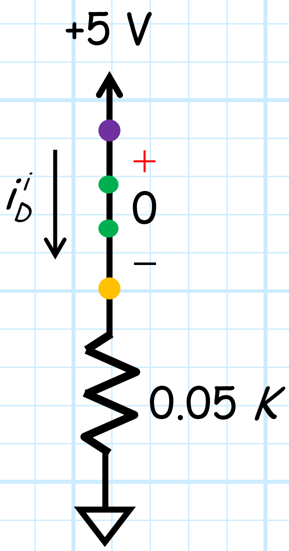
$$i_D = 87.40\ mA$$

$$v_D = 0.630\ V$$

Now, let's determine **approximate** values using diode **models** !

First, let's try the **ideal diode model**.





Assume IDEAL diode is "on".

Enforce $v_D^i = 0$.

Analyze the **IDEAL** diode circuit. From KVL:

$$5.0 - 0 - 0.05\, i_D^i = 0$$

$$\therefore \; i_D^i = \frac{5.0}{0.05} = 100 \; mA$$

Check result:

$$i_D^i = 100 \; mA \overset{?}{>} 0$$

We therefore can **approximate** the **junction diode** current as the current through the ideal diode **model**:

$$i_D \cong i_D^i = 100 \text{ mA}$$

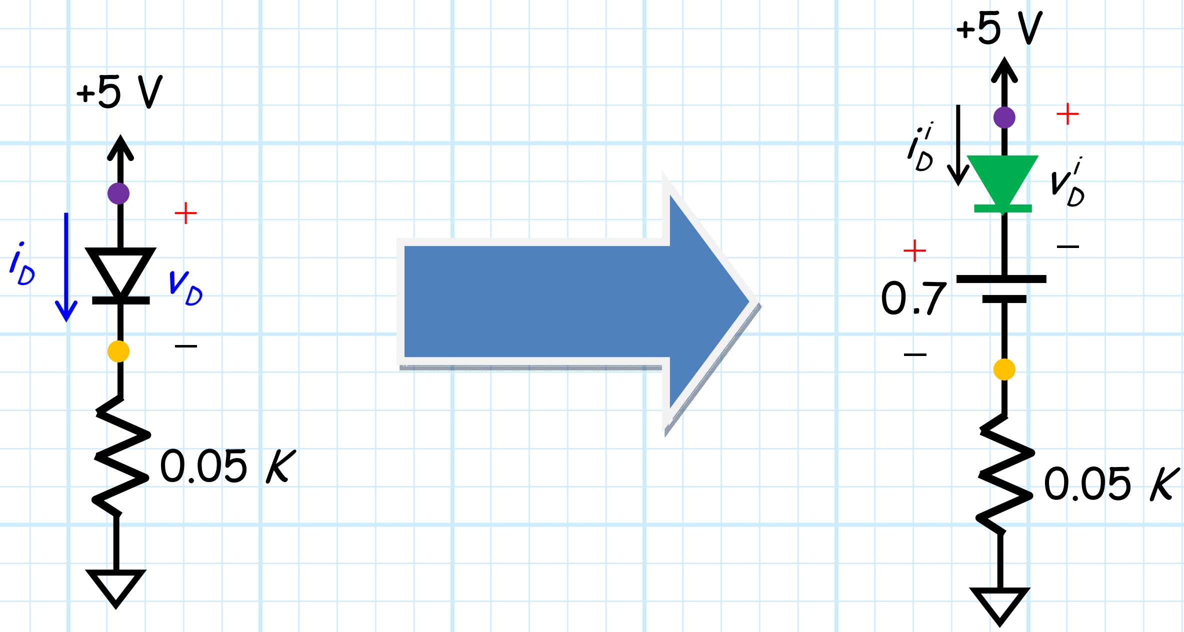
And **approximate** the **junction** diode voltage as the voltage across the ideal diode **model**:

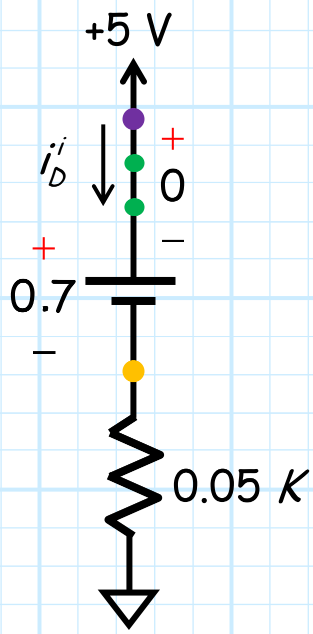
$$v_D \cong v_D^i = 0$$

Compare these approximations to the **exact** solutions:

$$i_D = 87.4 \; mA \text{ and } v_D = 0.630 \; V$$

Close, but we can do better! Let's use the **CVD model**.





Assume IDEAL diode is "on".

Enforce $v_D^i = 0$.

Analyze the **IDEAL** diode circuit. From KVL:

$$5.0 - v_D^i - 0.7 - 0.05\, i_D^i = 0$$

$$\therefore \quad i_D^i = \frac{5.0 - 0.7}{0.05} = 86.0 \; mA$$

Check the result:

$$i_D^i = 86.0 \overset{?}{>} 0$$

We therefore can **approximate** the **junction** diode current as the current through the CVD **model**:

$$i_D \cong i_D^i = 86.0 \; mA$$

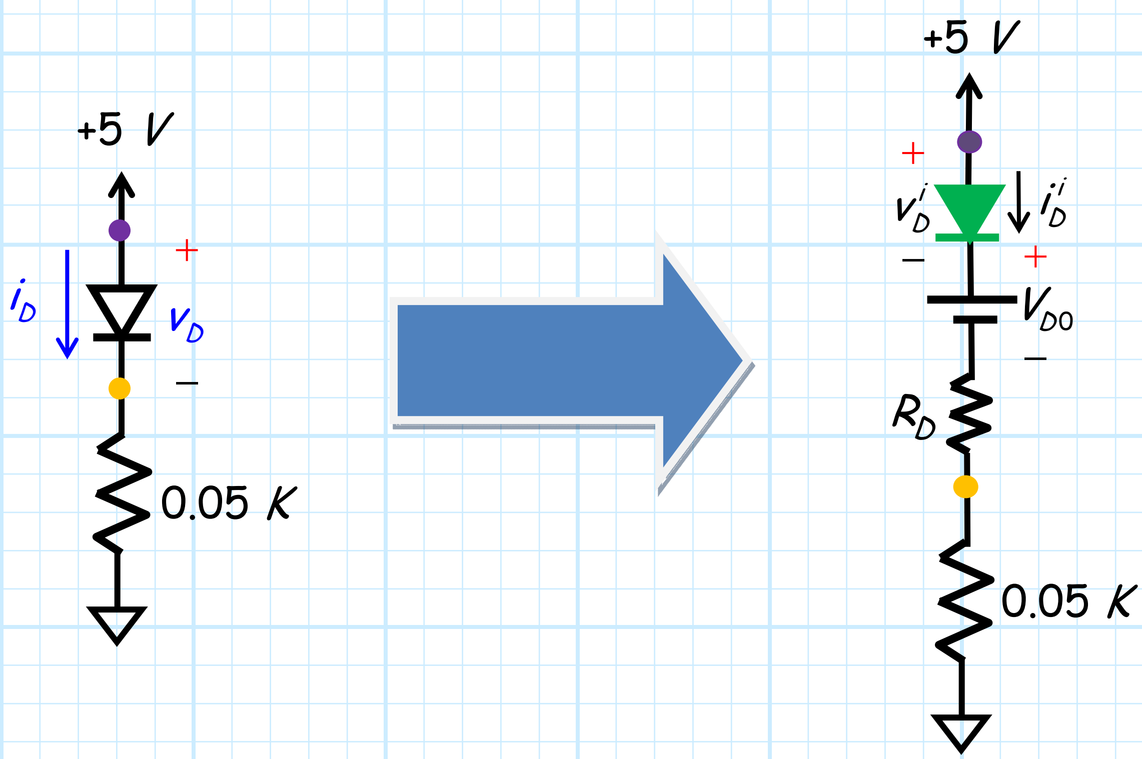
And **approximate** the **junction** diode voltage as the voltage across the CVD **model**:

$$\begin{aligned} v_D &\cong v_D^i + 0.7 \\ &= 0.0 + 0.7 \\ &= 0.7 \; V \end{aligned}$$

Compare these approximations to the **exact** solutions:

$$i_D = 87.4 \; mA \qquad \text{and} \qquad v_D = 0.630 \; V$$

Much better than before, but we can do **even better**! Let's use the **PWL model**.



Q: *But, what **values** should we use for model parameters V_{D0} and R_D ??*

A: From the CVD model, we know that i_D is approximately 86 *mA*. Therefore, let's create a **PWL model** that is accurate in the region between, **say**:

$$50\ mA < i_D < 125\ mA$$

First, we determine v_D at I_1 = 50 mA and I_2 =125 mA.

$$\begin{aligned} V_1 &= nV_T \ln\left(I_1 / I_S\right) \\ &= nV_T \ln\left(50 / I_S\right) \\ &= 0.616\ V \end{aligned} \qquad \begin{aligned} V_2 &= nV_T \ln\left(I_2 / I_S\right) \\ &= nV_T \ln\left(125 / I_S\right) \\ &= 0.639\ V \end{aligned}$$

We now know two points lying on the junction diode curve! Let's construct a PWL model whose "line" **intersects** these two points.

Recall that when the ideal diode is forward biased, applying KVL to the PWL model results in:

$$v_D = V_{D0} + i_D R_D$$

or equivalently:

$$i_D = v_D\left(\frac{1}{R_D}\right) - \frac{V_{D0}}{R_D}$$

Inserting the junction diode values (V_1,I_1) and (V_2,I_2) into this PWL model equation provides:

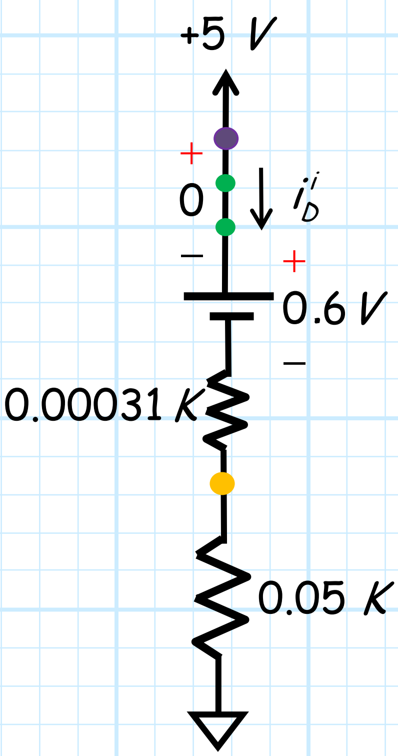
$$0.616 = V_{D0} + (0.05)R_D$$

$$0.639 = V_{D0} + (0.125)R_D$$

Two equations and **two** unknowns !! Solving, we get:

$$V_{D0} = 0.600\ V \text{ and } R_D = 0.00031 \text{ K (small !!)}$$

Therefore, the **ideal** diode circuit is:



Assume the **IDEAL** diode is "on".

Enforce $v_D^i = 0$.

Analyze the **IDEAL** diode circuit.

From KVL:

$$5.0 - v_D^i - 0.6 - (0.05 + 0.00031)\, i_D^i = 0$$

$$\therefore\ i_D^i = \frac{5.0 - 0.6}{0.05031} = 87.5\ mA$$

Check the result:

$$i_D^i = 87.5\ mA \overset{?}{>} 0$$

We can therefore **approximate** the **junction** diode current as the current through the PWL **model**:

$$i_D \approx i_D^i = \mathbf{87.5\ mA}$$

and **approximate** the **junction** diode voltage as the voltage across the PWL model:

$$\begin{aligned} v_D &= v_D^i + V_{D0} + i_D^i R_D \\ &= 0 + 0.600 + (0.087)0.31 \\ &= \mathbf{0.627\ V} \end{aligned}$$

Now, compare these values to the **exact** values v_D = **0.630** V and i_D = **87.4** mA.

The **error** of the PWL model estimates is just **0.003 Volts** and **0.1 mA** !

→ Each model provides **better** estimates than the previous one!

	i_D (mA)	v_D (V)
Ideal	100	0
CVD	86.0	0.700
PWL	87.5	0.627
Exact	87.4	0.630