11.1 Latches and Flip-Flops

Reading Assignment: *pp. 1013-1019*

We can also construct **Flip-Flops** with MOSFETs!

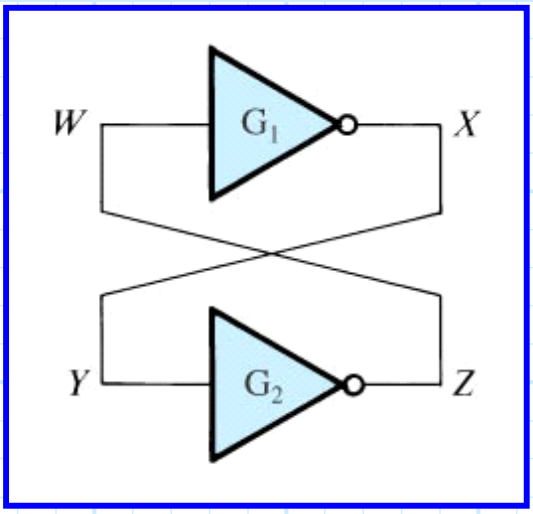
HO: The Digital Latch

By adding **set** and **reset** capabilities to a latch, we form the **S/R flip-flop**.

HO: The S/R Flip-Flop

The Digital "Latch"

Consider two digital inverters that are "**cross coupled**":



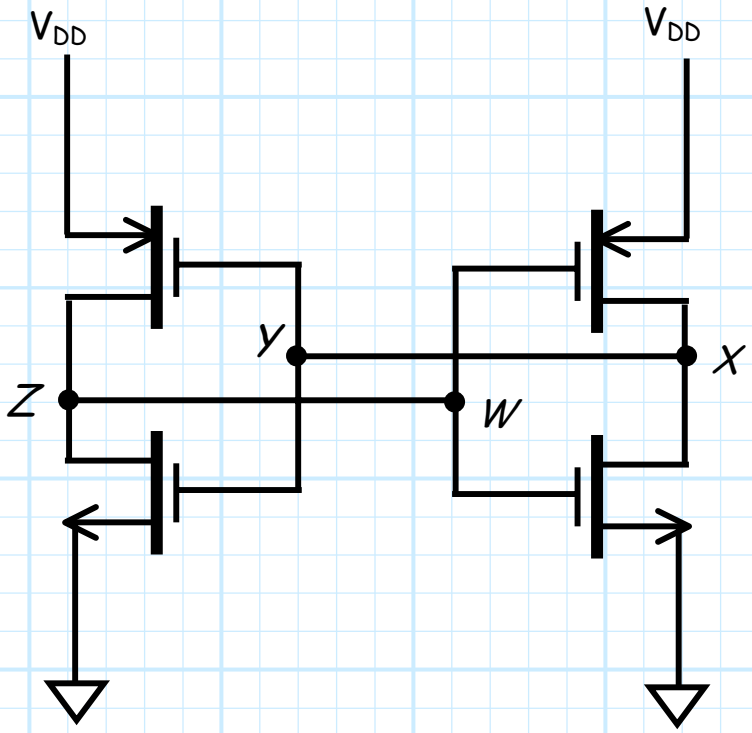
Note that there are **two stable states** for this circuit:

W	X	Y	Z	W
0	1	1	0	0
1	0	0	1	1

Thus, the latch will remain in either state until changed by an external input.

→ A **memory device**!

We of course can use **CMOS inverters** to build this latch:

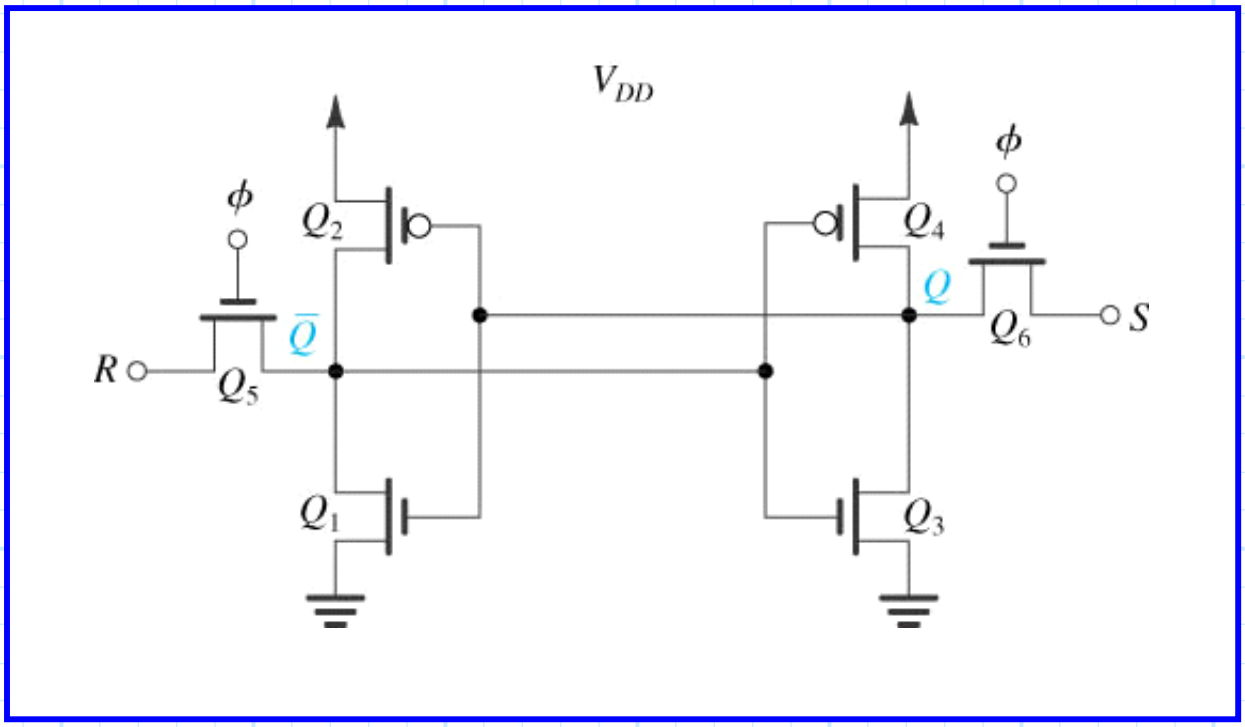


We must add external input in order to **change** the latch state.

→ The result will be a **Set/Reset Flip Flop**!

The S/R Flip-Flop

A **Set/Reset Flip-Flop** can be constructed by attaching **external** inputs to a **CMOS latch**:



Essentially, when S (**Set**) is high, the latch is set such that Q is **high**. Likewise, when R (**Reset**) is high, the latch is set such that Q is **low**.

Of course, if **neither** S nor R are high, then the state of the latch remains **unchanged**. We of course **never** wish to make **both** R and S high at the same time (confusion and ambiguity will result!).

The **truth table** for this circuit is thus that of a Set/Reset Flip Flop:

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	Not used

The value ϕ in the circuit above is an **enable line**, this must likewise be high if the latch is to change state.

The S/R Flip-Flop is thus a great **memory device**, storing the value of a **single bit** (1 or 0). Likewise, we can **write** to this storage device, setting its value to either 1 or 0 by enabling the S or R inputs, respectively.