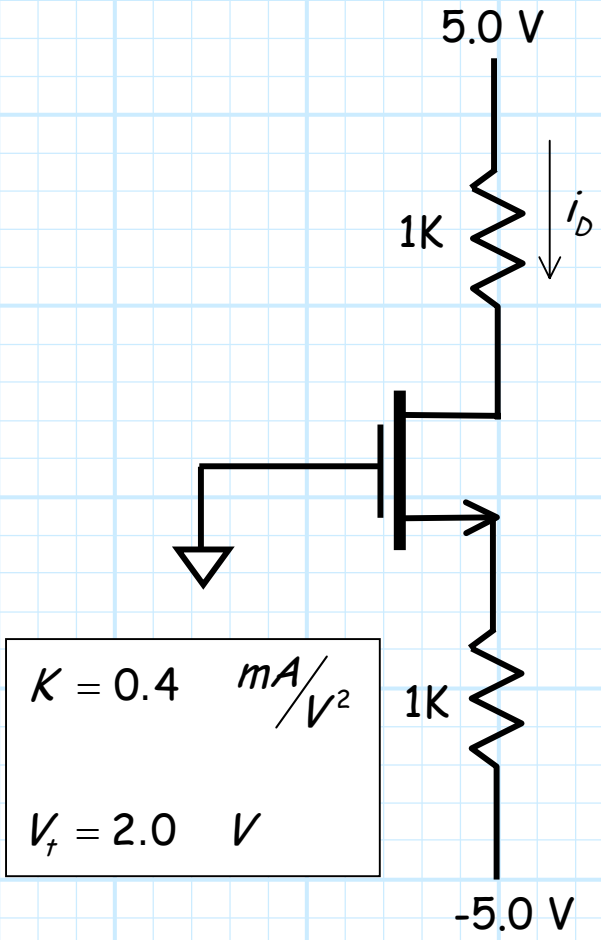
4.3 MOSFET Circuits at DC

Reading Assignment: *pp. 262-270*



Q:

A: HO: Steps for DC Analysis of MOSFET Circuits

Example: NMOS Circuit Analysis

Example: PMOS Circuit Analysis

Example: Another PMOS Circuit Analysis

Steps for D.C Analysis of MOSFET Circuits

To analyze MOSFET circuit with D.C. sources, we **must** follow these **five steps**:

1. *ASSUME* an operating mode

2. *ENFORCE* the equality conditions of that mode.

3. *ANALYZE* the circuit with the enforced conditions.

4. *CHECK* the inequality conditions of the mode for consistency with original assumption. If consistent, the analysis is complete; if inconsistent, go to step 5.

5. *MODIFY* your original assumption and repeat all steps.

Let's specifically look at each step in **detail**.

1. *ASSUME*

Here we have **three** choices—cutoff, triode, or saturation. You can make an "**educated guess**" here, but remember, until you CHECK, it's just a guess!

2. ENFORCE

For all three operating regions, we must ENFORCE just **one equality**.

Cutoff

Since **no** channel is induced, we ENFORCE the equality:

$$I_D = 0$$

Triode

Since the conducting channel **is** induced but **not** in pinch-off, we ENFORCE the equality:

$$I_D = K\left[2(V_{GS} - V_t)V_{DS} - V_{DS}^2\right]$$

Saturation

Since the conducting channel **is** induced and **is** in pinch-off, we ENFORCE the equality:

$$I_D = K(V_{GS} - V_t)^2$$

Note for all cases the constant K is:

$$K \doteq \frac{1}{2} k' \left(\frac{W}{L} \right)$$

and V_t is the MOSFET **threshold voltage**.

3. ANALYZE

The task in D.C. analysis of a MOSFET circuit is to find **one current** and **two voltages**!

a) Since the gate current I_G is zero ($I_G = 0$) for all MOSFETS in all modes, we need **only** to find the **drain current** I_D--this current value must be **positive** (or zero).

b) We also need to find **two** of the three **voltages** associated with the MOSFET. Typically, these two voltages are V_{GS} and V_{DS}, but given any two voltages, we can find the third using KVL:

$$V_{DS} = V_{DG} + V_{GS}$$

Some hints for MOSFET DC analysis:

1) Gate current $I_G = 0$ **always** !!!

2) Equations sometimes have **two** solutions! Choose solution that is **consistent** with the original ASSUMPTION.

4. CHECK

You do not know if your D.C. analysis is correct unless you CHECK to see if it is consistent with your original assumption!

WARNING!-Failure to CHECK the original assumption will result in a SIGNIFICANT REDUCTION in credit on exams, regardless of the accuracy of the analysis !!!

Q: *What exactly do we CHECK?*

A: We ENFORCED the mode **equalities**, we CHECK the mode **inequalities**.

We must CHECK **two** separate inequalities after analyzing a MOSFET circuit. Essentially, we check if we have/have not induced a conducting channel, and then we check if we have/have not pinched-off the channel (if it is conducting).

Cutoff

We must only CHECK to see if the MOSFET has a **conducting channel**. If **not**, the MOSFET is indeed in **cutoff**. We therefore CHECK to see if:

$$V_{GS} < V_t \quad \text{(NMOS)}$$

$$V_{GS} > V_t \quad \text{(PMOS)}$$

Triode

Here we must first CHECK to see **if** a channel has been induced, i.e.:

$$V_{GS} > V_t \quad \text{(NMOS)}$$

$$V_{GS} < V_t \quad \text{(PMOS)}$$

Likewise, we must CHECK to see if the channel has reached **pinchoff**. If **not**, the MOSFET is indeed in the **triode** region. We therefore CHECK to see if:

$$V_{DS} < V_{GS} - V_t \quad \text{(NMOS)}$$

$$V_{DS} > V_{GS} - V_t \quad \text{(PMOS)}$$

Saturation

Here we must first CHECK to see **if** a channel has been induced, i.e.:

$$V_{GS} > V_t \quad \text{(NMOS)}$$

$$V_{GS} < V_t \quad \text{(PMOS)}$$

Likewise, we must CHECK to see if the channel has reached **pinchoff**. If it **has**, the MOSFET is indeed in the **saturation** region. We therefore CHECK to see if:

$$V_{DS} > V_{GS} - V_t \quad \text{(NMOS)}$$

$$V_{DS} < V_{GS} - V_t \quad \text{(PMOS)}$$

If the results of our analysis are consistent with **each** of these inequalities, then we have made the **correct** assumption! The **numeric** results of our analysis are then likewise **correct**. We can **stop** working!

However, if **even one** of the results of our analysis is **inconsistent** with our ASSUMPTION, then we have made the **wrong** assumption! → Time to move to step 5.

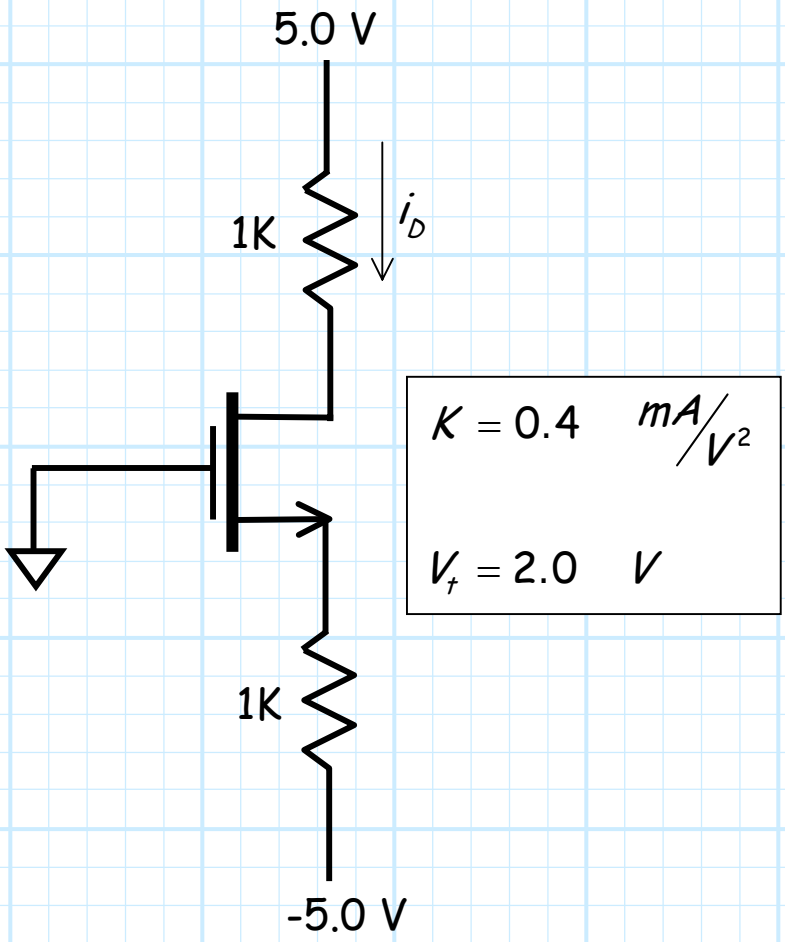
5. MODIFY

If **one or more** of the circuit MOSFETSs are **not** in their ASSUMED mode, we must change our assumptions and start **completely** over!

In general, **all** of the results of our previous analysis are incorrect, and thus must be **completely** scraped!

Example: NMOS Circuit Analysis

Consider this DC MOSFET circuit:



Let's ASSUME the NMOS device is in saturation.

Thus, we must ENFORCE the condition that:

$$I_D = K\left(V_{GS} - V_t\right)^2$$

Now we must ANALYZE the circuit.

Q: *What now? How do we proceed with this analysis?*

A: It's certainly not clear. Let's write the circuit equations and see what happens.

From the Gate-Source loop KVL:

$$0.0 - V_{GS} - (1)I_D = -5.0$$

Therefore, rearranging:

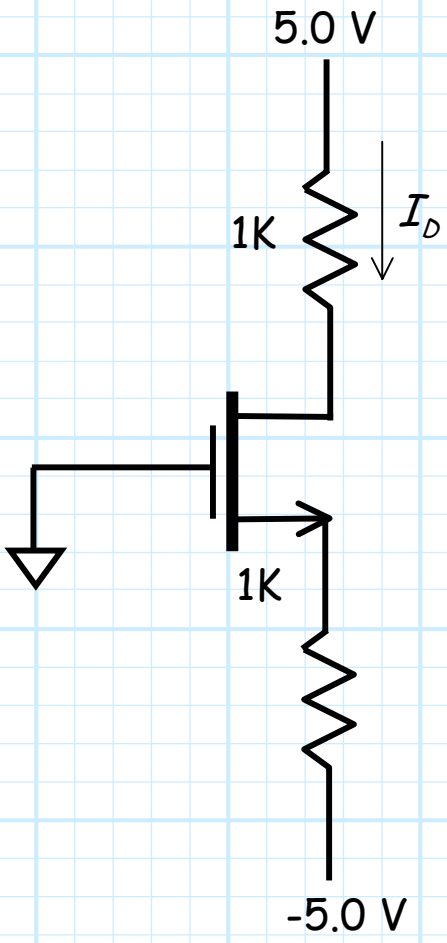
$$I_D = 5.0 - V_{GS}$$

And from the Drain-Source loop KVL:

$$5.0 - (1)I_D - V_{DS} - (1)I_D = -5.0$$

Therefore, rearranging:

$$V_{DS} = 10.0 - 2I_D$$



Look! We can equate the NMOS device equation and G-S equation to find V_{GS}.

$$I_D = K\left(V_{GS} - V_t\right)^2 = 5.0 - V_{GS}$$

$$\therefore 0 = K\,V_{GS}^2 + V_{GS}\left(1 - 2K\,V_t\right) + \left(K\,V_t^2 - 5.0\right)$$

A quadratic equation!

The solutions to this equation are:

$$V_{GS} = 3.76\,V \qquad \text{or} \qquad V_{GS} = -2.26\,V$$

Q: *Yikes! **Two** solutions! Which one is correct?*

A: Note we **assumed** saturation. If the MOSFET is in saturation, we know that:

$$V_{GS} > V_t = 2.0$$

Only one solution of the quadratic satisfies this conidtion, i.e.:

$$V_{GS} = 3.76 > V_t$$

Thus, we use $V_{GS} = 3.76\,V$ --the solution that is consistent with our original assumption.

Inserting this voltage into the Gate-Source KVL equation, we find that the drain current is:

$$\begin{aligned} I_D &= 5.0 - V_{GS} \\ &= 5.0 - 3.76 \\ &= 2.24\ mA \end{aligned}$$

And using the Drain-Source KVL, we find the remaining voltage:

$$\begin{aligned} V_{DS} &= 10.0 - 2.0\, I_D \\ &= 10.0 - 2(2.24) \\ &= 5.52\, V \end{aligned}$$

Even though we have answers (one current and two voltages), we still are not finished, as we now must CHECK our solution to see if it is consistent with the saturation mode inequalities.

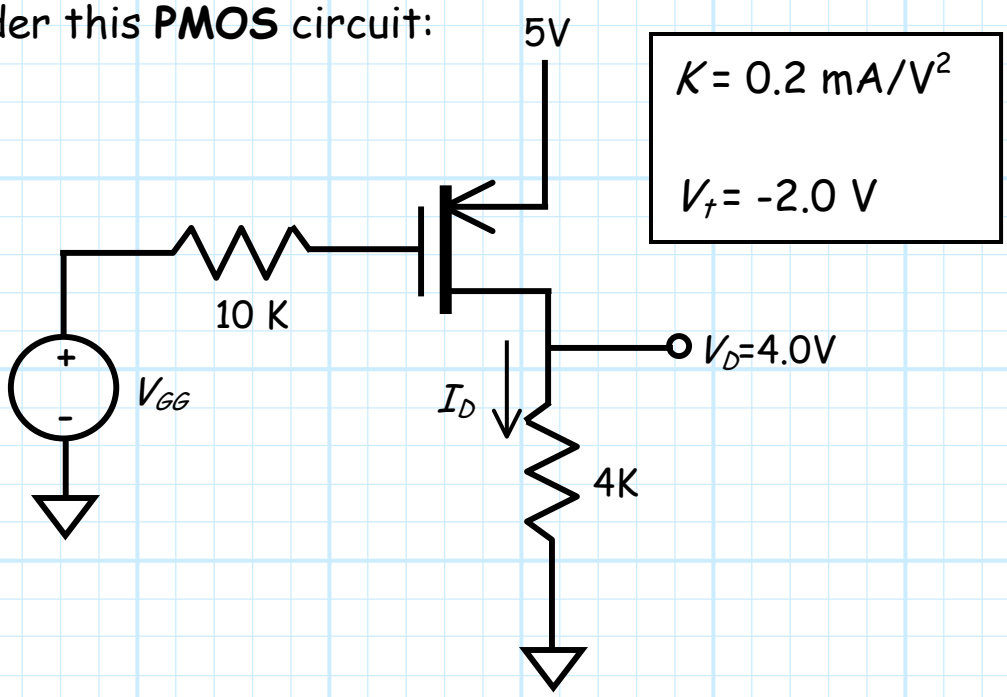
$$3.76 = V_{GS} > V_t = 2.0$$ ✓

$$5.52 = V_{DS} > V_{GS} - V_t = 1.76$$ ✓

Both answers are consistent! Our solutions are correct!

Example: PMOS Circuit Analysis

Consider this **PMOS** circuit:



For this problem, we know that the **drain voltage** V_D = 4.0 V (with respect to ground), but we do **not** know the value of the voltage source V_{GG}.

Let's attempt to **find** this value V_{GG}!

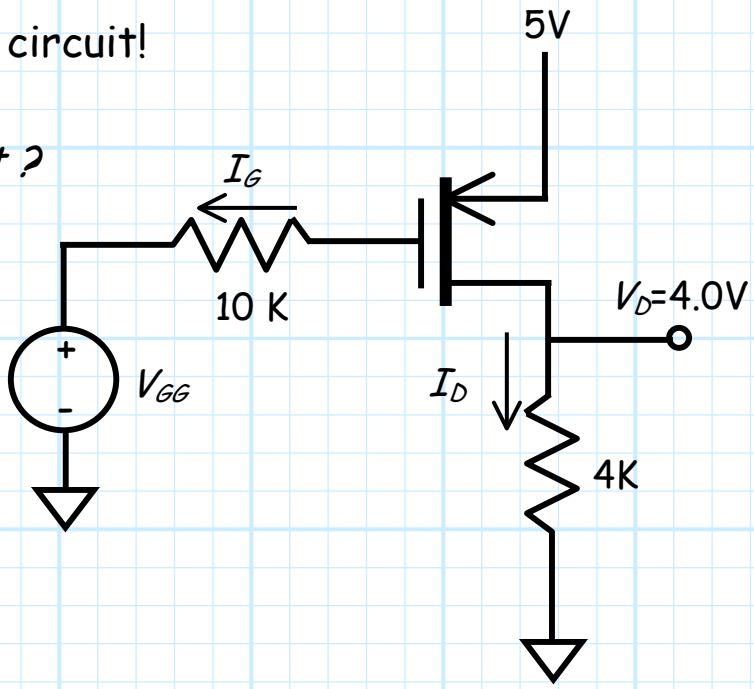
First, let's ASSUME that the PMOS is in **saturation** mode.

Therefore, we ENFORCE the **saturation** drain current equation $I_D = K\left(V_{GS} - V_t\right)^2$.

Now we must ANALYZE this circuit!

Q: *Yikes! Where do we start ?*

A: The best way to start is by "**picking the low-hanging fruit**". In other words, determine the **obvious** and easy values. **Don't** ask, "What is V_{GG}?", but **instead** ask, "What **do** I know?" !



There are **lots** of things that we can **quickly** determine about this circuit!

$$I_G = 0.0 \quad mA$$

$$V_S = 5.0 \quad V$$

$$I_D = \frac{V_D - 0}{4} = \frac{4.0 - 0}{4} = 1\ mA$$

$$V_G = V_{GG} - 10\,I_G = V_{GG} - 10(0) = V_{GG}$$

Therefore, we can likewise determine:

$$V_{DS} = V_D - V_S = 4.0 - 5.0 = -1.0\ V$$

$$V_{GS} = V_G - V_S = V_{GG} - 5.0 \quad V$$

Note what we have **quickly determined**—the **numeric** value of drain current (I_D=1.0 mA) and the voltage drain-to-source (V_{DS}=-1.0) Moreover, we have determined the value V_{GS} in terms of **unknown** voltage V_{GG} ($V_{GS} = V_{GG} - 5.0$).

We've determined all **the important stuff** (i.e., V_{GS}, V_{DS}, I_D)!

We can now relate these values using our PMOS **drain current equation**. Recall that we ASSUMED **saturation**, so **if** this assumption is correct:

$$I_D = K\left(V_{GS} - V_t\right)^2$$

Inserting into this equation our knowledge from above, along with our **PMOS** values K=0.2 mA/V^2 and V_t=-2.0, we get:

$$I_D = K\left(V_{GS} - V_t\right)^2$$
$$1.0 = 0.2\left(V_{GS} - (-2.0)\right)^2$$
$$5.0 = \left(V_{GS} + 2.0\right)^2$$

Be **careful** here! Note in the above equation that threshold voltage V_t is **negative** (since PMOS) and that I_D and K are both written in terms of **milliamps** (mA).

Now, we solve this equation to find the value of V_{GS}!

$$5.0 = (V_{GS} + 2.0)^2$$
$$\pm\sqrt{5} = V_{GS} + 2.0$$
$$\pm\sqrt{5} - 2.0 = V_{GS}$$

Q: *So V_{GS} is **both** $\sqrt{5} - 2.0 = 0.24\,V$ **and** $-\sqrt{5} - 2.0 = -4.23\,V$? How can this be **possible?***

A: It's **not** possible! The solution is **either** V_{GS}=0.24 V **or** V_{GS} = -4.23 V.

Q: *But how can we tell **which** solution is correct?*

A: We must choose a solution that is **consistent** with our original ASSUMPTION. Note that **neither** of the solutions **must** be consistent with the saturation ASSUMPTION, an event meaning that our ASSUMPTION was wrong.

However, **one** (but **only one**!) of the two solutions may be consistent with our saturation ASSUMPTION—**this** is the value that we choose for V_{GS}!

For this example, where we have ASSUMED that the PMOS device is in **saturation**, the voltage gate-to-source V_{GS} must be **less** (remember, it's a **PMOS** device!) than the **threshold voltage**:

$$V_{GS} < V_t$$
$$V_{GS} < -2.0\,V$$

Clearly, one of our solutions **does** satisfy this equation ($V_{GS} = -4.23 < -2.0$), and therefore we choose the **solution** $V_{GS} = -4.23\,V$.

Q: *Does this mean our saturation ASSUMPTION is **correct**?*

A: **NO!** It merely means that our saturation ASSUMPTION **might** be correct! We need to CHECK the other inequalities to know for **sure**.

Now, returning to our circuit **analysis**, we can quickly determine the **unknown** value of V_{GG}. Recall that we **earlier** determined that:

$$V_{GS} = V_{GG} - 5.0$$

And now, since we "know" that the V_{GS}=-4.23 V, we can determine that:

$$\begin{aligned} V_{GG} &= V_{GS} + 5.0 \\ &= -4.23 + 5.0 \\ &= 0.77\,V \end{aligned}$$

This solution (V_{GG}=0.77 V) is of course true **only if** our original ASSUMPTION was correct. Thus, we must CHECK to see if our **inequalities** are valid:

We of course already know that the **first** inequality is true—a p-type channel is induced:

$$V_{GS} = -4.23 < -2.0 = V_t \quad \checkmark$$

And, since the **excess gate voltage** is $V_{GS} - V_t = -2.23\ V$, the **second** inequality:

$$V_{DS} = -1.0 > -2.23 = V_{GS} - V_t$$ ✗

shows us that our ASSUMPTION was **incorrect**!

→ Time to make a **new** ASSUMPTION and **start over**!

So, let's **now** ASSUME the PMOS device is in **triode** region.

Therefore ENFORCE the drain current equation:

$$i_D = K\left[2(V_{GS} - V_t)V_{DS} - V_{DS}^2\right]$$

Now let's ANALYZE our circuit!

Note that most of our **original** analysis was **independent** of our PMOS mode ASSUMPTION. Thus, we **again** conclude that:

$I_G = 0.0\ mA$

$V_S = 5.0\ V$

$$I_D = \frac{V_D - 0}{4} = \frac{4.0 - 0}{4} = 1\ mA$$

$$V_G = V_{GG} - 10\,I_G = V_{GG} - 10(0) = V_{GG}$$

Therefore,

$$V_{DS} = V_D - V_S = 4.0 - 5.0 = -1.0 \ V$$

$$V_{GS} = V_G - V_S = V_{GG} - 5.0 \quad V$$

Now, inserting these values in the **triode drain current equation**:

$$i_D = K\left[2(V_{GS} - V_t)V_{DS} - V_{DS}^2\right]$$

$$1.0 = 0.2\left[2\left(V_{GS} - (-2)\right)(-1) - (-1)^2\right]$$

$$5.0 = \left[-2(V_{GS} + 2) - 1\right]$$

Look! **One** equation and **one** unknown! Solving for V_{GS} we find:

$$5.0 = \left[-2(V_{GS} + 2) - 1\right]$$

$$6.0 = -2(V_{GS} + 2)$$

$$-3.0 = V_{GS} + 2$$

$$-5.0 = V_{GS}$$

Thus, we find that V_{GS} = -5.0 V, so that we can find the **value** of voltage source V_{GG}:

$$V_{GS} = V_{GG} - 5.0$$

$$-5.0 = V_{GG} - 5.0$$

$$0.0 = V_{GG}$$

The voltage source V_{GG} is equal to **zero**—provided that our triode ASSUMPTION was **correct**.

To find out **if** the ASSUMPTION is correct, we must CHECK our **triode inequalities**.

First, we CHECK to see if a channel has indeed been **induced:**

$$V_{GS} = -5.0 < -2.0 = V_t \quad \surd$$

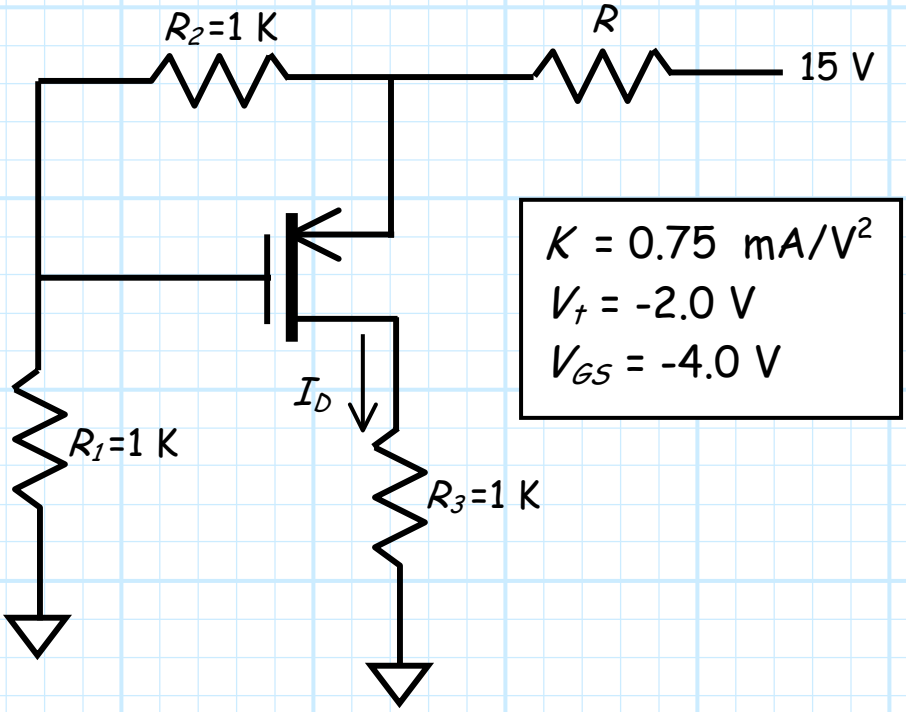
Next, we CHECK to make sure that our channel is **not** in pinch-off. Noting that the **excess gate voltage** is $V_{GS} - V_t = -5.0 - (-2.0) = -3.0\,V$, we find that:

$$V_{DS} = -1.0 > -3.0 = V_{GS} - V_t \quad \surd$$

Our **triode** ASSUMPTION is **correct**! Thus, the voltage source V_{GG} = 0.0 V.

Example: Another PMOS Circuit Analysis

Consider the **PMOS** circuit below, where we know (somehow) that V_{GS} = -4.0 V, but don't know (for some reason) the value of resistor R.

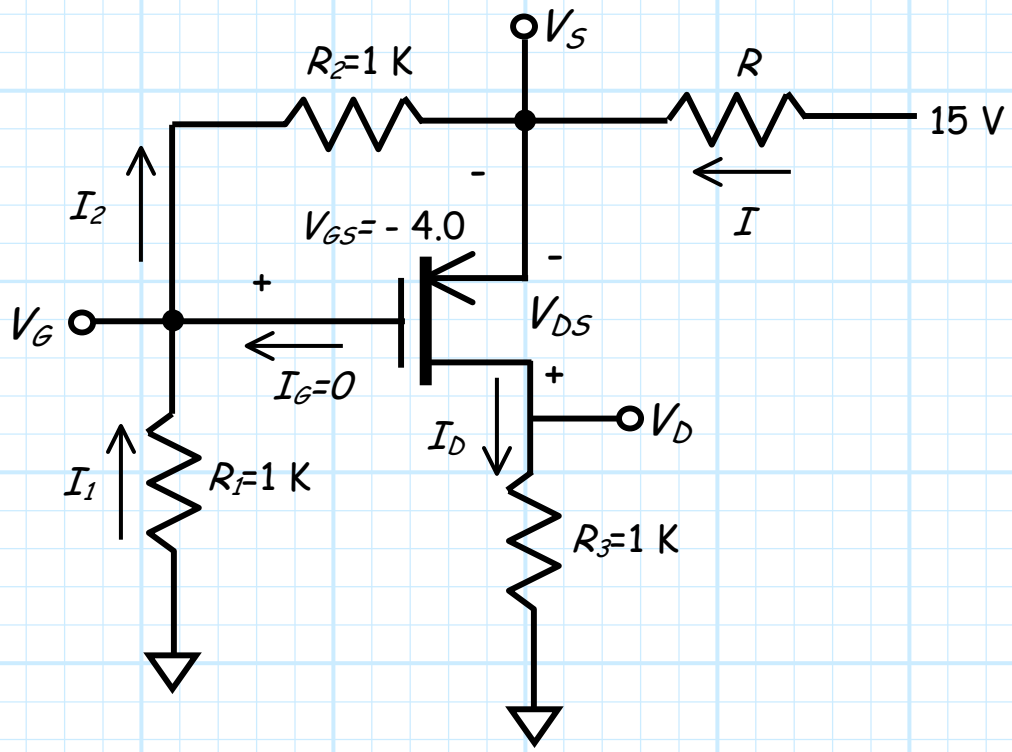


Let's see if we can determine the value of resistor R.

First, let's ASSUME that the MOSFET is in saturation, and therefore ENFORCE the drain current equation:

$$I_D = K\left(V_{GS} - V_t\right)^2$$

Now we ANALYZE the circuit:



Since we know that V_{GS}=-4.0 V, and we ASSUMED that the PMOS device was in saturation, we can directly determine the drain current I_D:

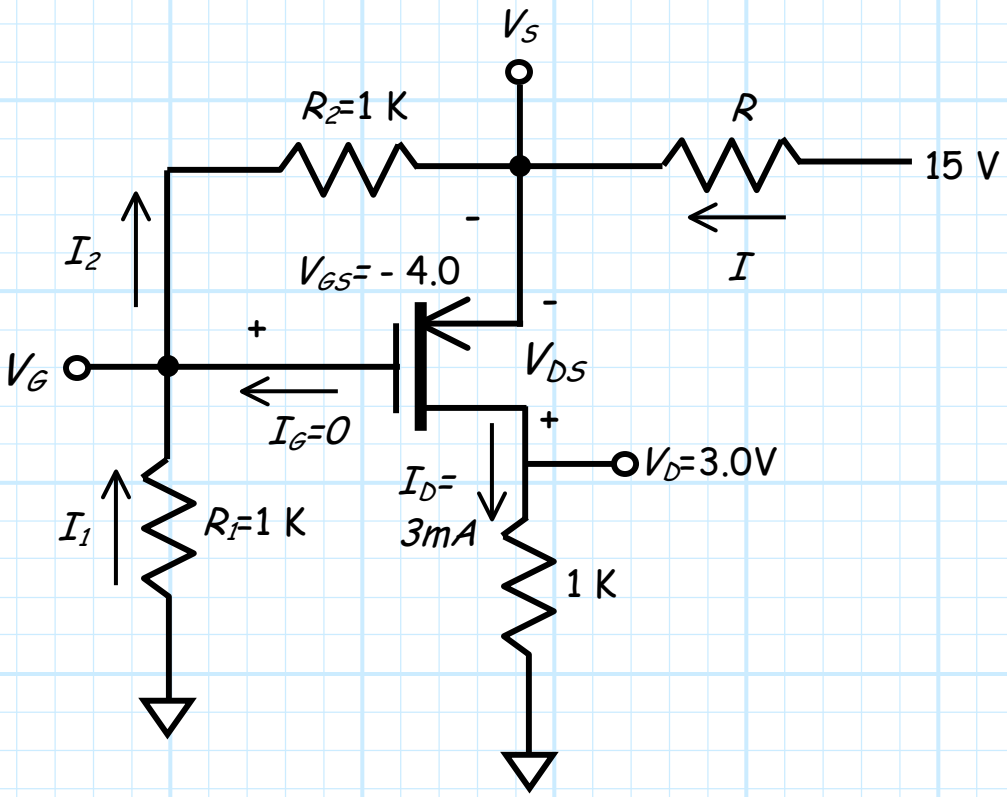
$$\begin{aligned} I_D &= K\left(V_{GS}-V_t\right)^2 \\ &= 0.75\left(-4.0-\left(-2.0\right)\right)^2 \\ &= 0.75\left(-4.0+2.0\right)^2 \\ &= 3\,mA \end{aligned}$$

and thus the drain voltage V_D is:

$$\begin{aligned} V_D &= 0.0 + I_D R_3 \\ &= 0.0 + (3.0)1.0 \\ &= 3.0\ \text{V} \end{aligned}$$

Q: *OK, this first part was easy, but what do we do now? How can we determine the value of resistor R ?*

A: The key to "unlocking" this circuit analysis is recognizing that the potential difference across resistor R_2 is simply the voltage V_{GS}—and we **know** the value of V_{GS} (V_{GS} =-4.0V)!



Thus, we can immediately determine that current I_2 is:

$$I_2 = \frac{V_{GS}}{R_2} = \frac{-4.0}{1} = -4.0\ mA$$

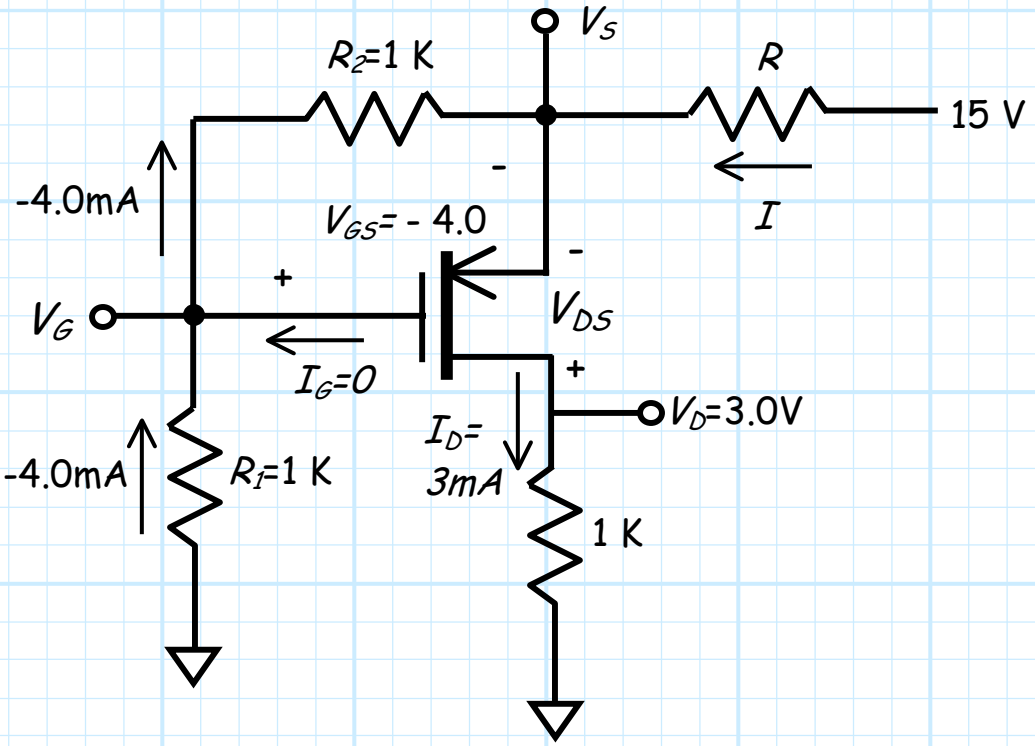
Likewise, from KCL, we find:

$$I_1 + I_G = I_2$$

But since gate current $I_G = 0$, we conclude:

$$I_1 = I_2 = -4.0\ mA$$

Now we can determine much about this circuit!

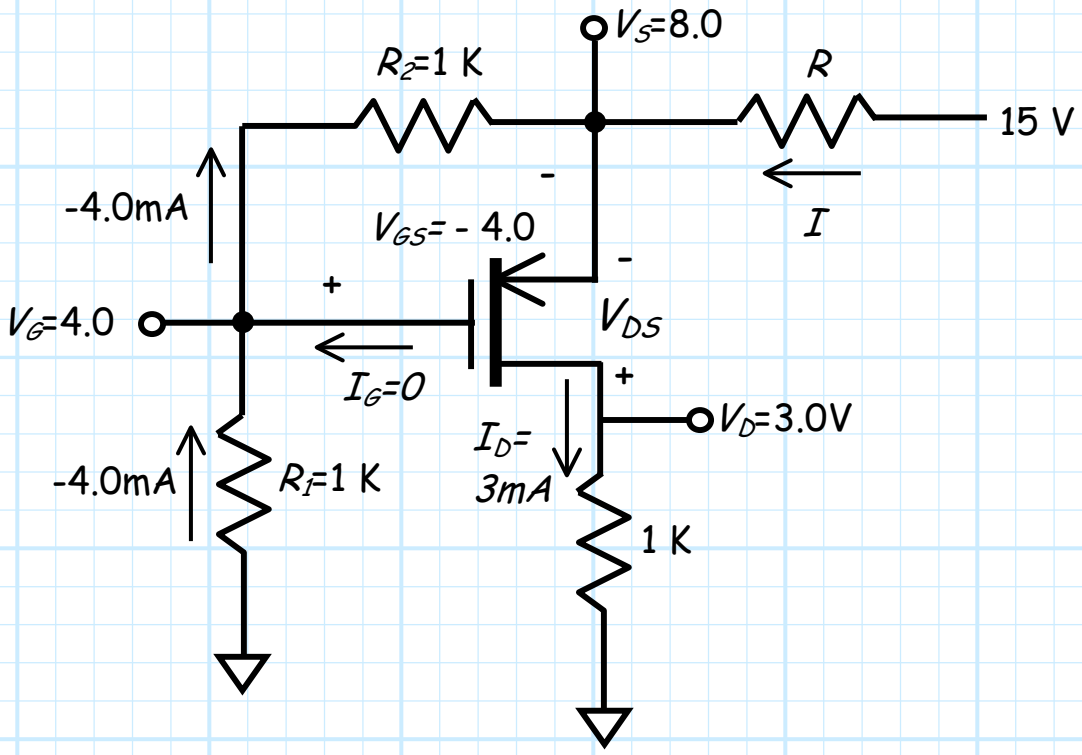


For example, from KVL, we find the gate voltage:

$$\begin{aligned} V_G &= 0.0 - I_1 R_1 \\ &= -(-4.0)1 \\ &= 4.0\ \text{V} \end{aligned}$$

And likewise the source voltage:

$$\begin{aligned} V_S &= V_G - I_2 R_2 \\ &= 4.0 - (-4.0)1 \\ &= 8.0\ \text{V} \end{aligned}$$



Likewise, from KCL, we can determine the current through resistor *R*:

$$\begin{aligned} I &= I_D - I_2 \\ &= 3.0 - (-4.0) \\ &= 7.0\ mA \end{aligned}$$

And thus from Ohm's Law we can find the value of *R*:

$$\begin{aligned} R &= \frac{15.0 - V_S}{I} \\ &= \frac{15.0 - 8.0}{7.0} \\ &= 1\ K \end{aligned}$$

But wait! We're still not done! We must CHECK to see if our original ASSUMPTION was correct.

First, we CHECK to see if the channel is induced:

$$V_{GS} = -4.0 < -2.0 = V_t \quad \checkmark$$

Next, we CHECK to see if the channel is pinched off. Here, we note that $V_{DS} = V_D - V_S = 3.0 - 8.0 = -5.0\,\text{V}$, and excess gate voltage is $V_{GS} - V_t = -4.0 - (-2.0) = -2.0\,\text{V}$. Therefore:

$$V_{DS} = -5.0 < -2.0 = V_{GS} - V_t \quad \checkmark$$

Hence, our ASSUMPTION is correct, and R =1K.