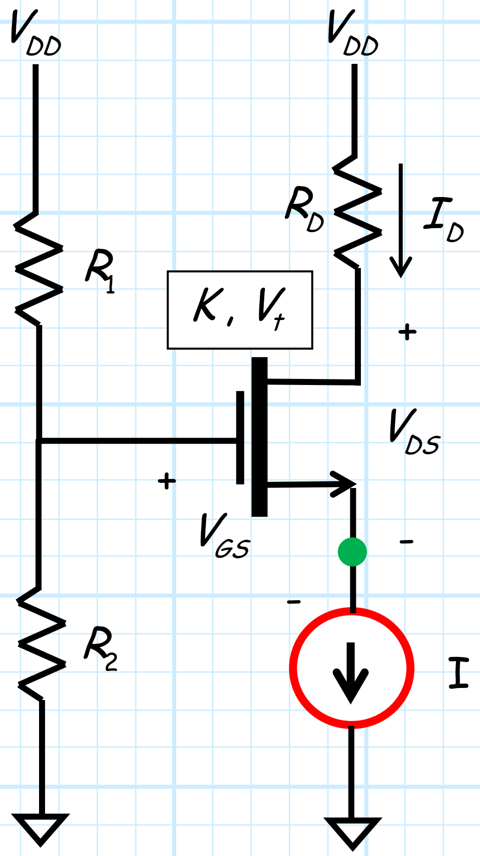
MOSFET Biasing using a Current Mirror

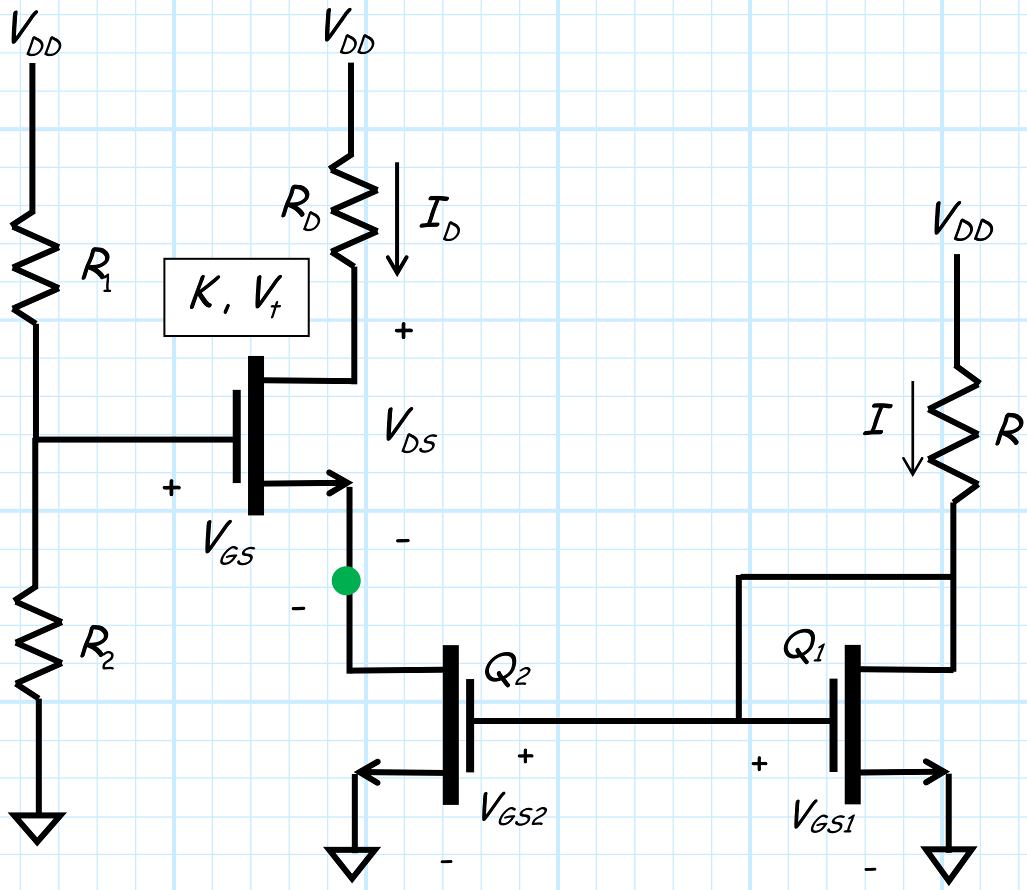
Just as with BJT amplifiers, we can likewise bias a MOSFET amplifier using a **current source**:



It is evident that the DC drain current I_D, is equal to the current source I, **regardless** of the MOSFET values K or V_t!

Thus, this bias design maximizes drain current **stability**!

We now know how to implement this bias design with MOSFETs—we use the **current mirror** to construct the current source!



Since $I_D = I$, it is evident that V_{GS} **must** be equal to:

$$V_{GS} = \sqrt{\frac{I}{K}} + V_t$$

and since the DC **gate** voltage is:

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

It is evident that the DC **source** voltage V_S is thus:

$$
\begin{aligned}
V_S &= V_G - V_{GS} \\
&= V_{DD}\left(\frac{R_2}{R_1+R_2}\right) - \left(\sqrt{\frac{I}{K}} + V_t\right)
\end{aligned}
$$

Since we are biasing with a current source, we do **not** need to worry about drain current **stability**—the current source will determine the DC drain current for **all** conditions (i.e., $I_D = I$).

We might conclude therefore, that we should make DC source voltage V_S as **small** as possible. After all, this would allow us to **maximize** the output voltage swing (i.e., maximize $I_D R_D$ and V_{DS}).

Note however, that the **source** voltage V_S of the MOSFET is numerically equal to the **drain** voltage V_{D2} (and thus V_{DS2}) of the second MOSFET of the **current mirror**.

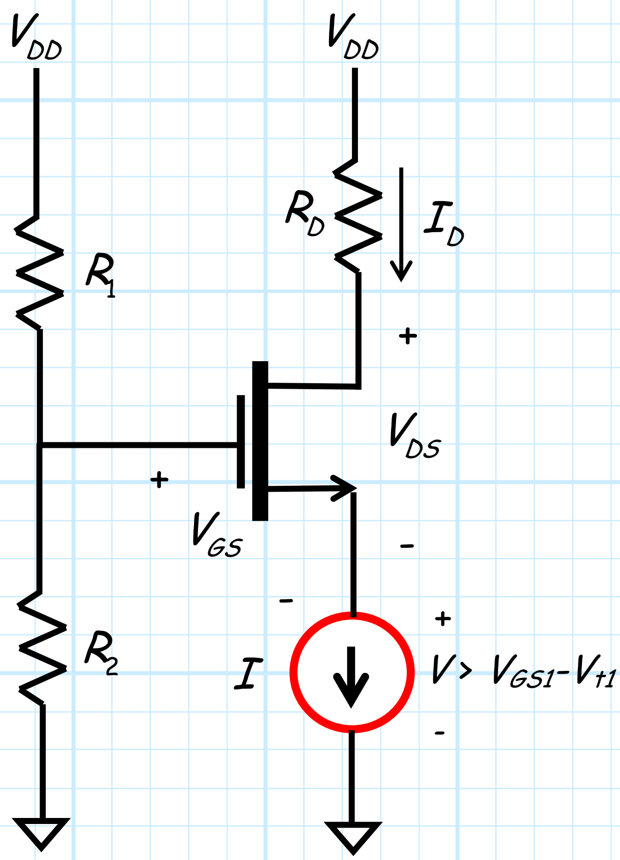
Q: *So what?!*

A: The voltage $V_{DS2} = V_S$ must be **greater** than:

$$
\begin{aligned}
V_{GS2} - V_{t2} &= V_{GS1} - V_{t1} \\
&= \left(V_{DD} - I_{ref}R\right) - V_{t1}
\end{aligned}
$$

in order for the **second** MOSFET to remain in **saturation**.

There is a **minimum voltage** across the current source in order for the current source to properly operate!



Thus, to maximize output swing, we **might** wish to set:

$$V_S = V_{GS1} - V_{t1}$$

(although to be practical, we should make V_S **slightly greater** than this to allow for some design **margin**).

Q: *How do we "set" the DC **source** voltage V_S ??*

A: By setting the DC **gate** voltage V_G !!

Recall that the DC voltage V_{GS} is determined by the DC current source value I:

$$V_{GS} = \sqrt{\frac{I}{K}} + V_t$$

and the DC gate voltage is determined by the **two** resistors R_1 and R_2:

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

Thus, we should **select** these resistors such that:

$$\begin{aligned} V_G &= V_{GS} + V_S \\ &= \left(\sqrt{\frac{I}{K}} + V_t \right) + \left(V_{GS1} - V_{t1} \right) \end{aligned}$$

Q: *So what should the value of resistor R_D be?*

A: Recall that we should set the DC **drain** voltage V_D:

a) much **less** than V_{DD} to avoid **cutoff**.

b) much **greater** than $V_G - V_t$ to avoid **triode**.

Thus, we **compromise** by setting the DC drain voltage to a point **halfway** in between!

$$V_D = \frac{V_{DD} + \left(V_G - V_t \right)}{2}$$

To achieve this, we must select the drain **resistor** R_D so that:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{V_{DD} - \left(V_G - V_t \right)}{I_D}$$