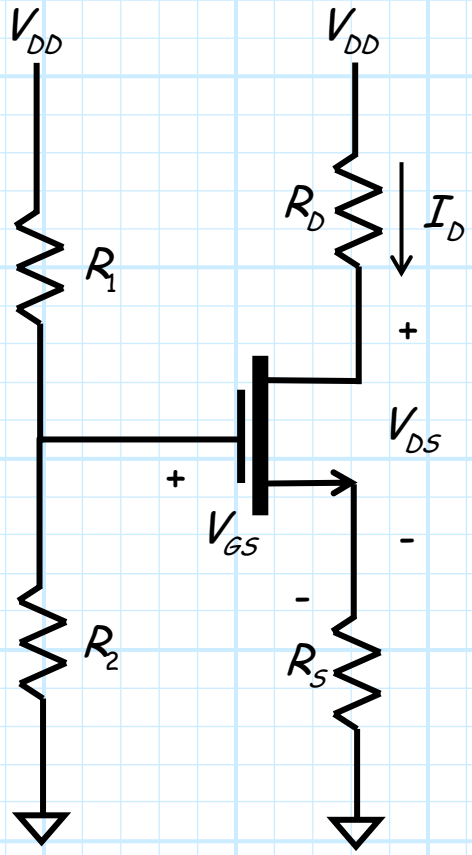
MOSFET Biasing using a Single Power Supply

The general form of a **single**-supply MOSFET amplifier biasing circuit is:



Just like BJT biasing, we typically attempt to satisfy three main bias design goals:

1) Maximize Gain

Typically, the small-signal **voltage gain** of a MOSFET amplifier will be proportional to transconductance g_m:

$$A_{vo} \propto g_m$$

Thus, to maximize the amplifier voltage gain, we must **maximize** the MOSFET transconductance.

Q: *What does this have to do with **D.C. biasing?***

A: Recall that the transconductance depends on the **DC excess gate voltage**:

$$g_m = 2K\left(V_{GS} - V_t\right)$$

Another way to consider transconductance is to express it in terms of DC drain current I_D. Recall this DC current is related to the DC excess gate voltage (in satureation!) as:

$$I_D = K\left(V_{GS} - V_t\right)^2 \qquad \Rightarrow \qquad \left(V_{GS} - V_t\right) = \sqrt{\frac{I_D}{K}}$$

And so transconductance can be alternatively expressed as:

$$g_m = 2K\left(V_{GS} - V_t\right) = 2K\sqrt{\frac{I_D}{K}} = 2\sqrt{KI_D}$$

Therefore, the amplifier voltage gain is typically **proportional** to the square-root of the DC drain current:

$$A_{vo} \propto \sqrt{I_D}$$

To maximize A_{vo}, maximize I_D

2) Maximize Voltage Swing

Recall that if the DC drain voltage V_D is biased too close to V_{DD}, then even a small small-signal drain voltage $v_d(t)$ can result in a **total** drain voltage that is too **large**, i.e.:

$$v_D(t) = V_D + v_d(t) \geq V_{DD}$$

In other words, the MOSFET enters **cutoff**, and the result is a **distorted** signal!

To avoid this (to allow $v_d(t)$ to be as large as possible without MOSFET entering cutoff), we need to bias our MOSFET such that the DC drain voltage V_D is as **small** as possible.

Note that the drain voltage is:

$$V_D = V_{DD} - R_D I_D$$

Therefore V_D is minimized by designing the bias circuit such that the DC drain current I_D is as **large** as possible.

However, we must **also** consider the signal distortion that occurs when the MOSFET enters **triod**. This of course is avoided if the total voltage drain-to-source remains greater than the excess gate voltage, i.e.:

$$v_{DS}(t) = V_{DS} + v_{ds}(t) > (V_{GS} - V_t)$$

Thus, to avoid the MOSFET triode mode—and the resulting signal distortion—we need to bias our MOSFET such that the DC voltage V_{DS} is as **large** as possible.

To minimize signal distortion, maximize V_{DS}

3) Minimize Sensitivity to changes in K, V_t

We find that MOSFETs are **sensitive** to temperature—specifically, the value of K is a function of temperature.

Likewise, the values of K and threshold voltage V_t are not particularly constant with regard to the manufacturing process.

Both of these facts lead to the requirement that our bias design be **insensitive** to the values of K and V_t. Specifically, we want to design the bias network such that the DC bias current does **not** change values when K and/or V_t does.

Mathematically, we can express this requirement as minimizing the value:

$$\frac{d\,I_D}{dK} \quad \text{and} \quad \frac{d\,I_D}{dV_t}$$

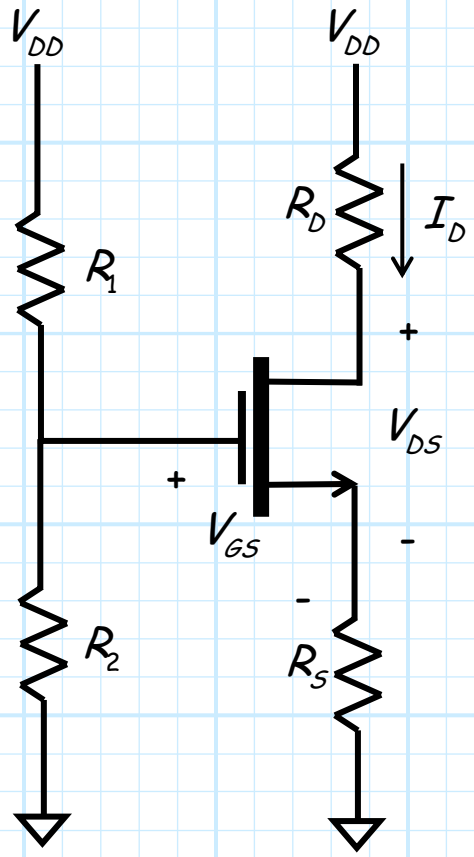
Similar to the BJT, we find that these derivatives are minimized by maximizing the value of **source resistor** R_S.

To minimize $d\,I_D/dK$, maximize R_S

So, let's **recap** what we have learned about designing our bias network:

1. Make I_D as large as possible.
2. Make V_{DS} as large as possible.
3. Make R_S as large as possible.

Again analogous to BJT biasing, we find that these three goals are conflicting, as they are constrained by the KVL equation of the bias circuit:



$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

or

$$I_D R_D + V_{DS} + I_D R_S = V_{DD}$$

Maximize A_{vo} by **maximizing** this term.

Minimize distortion by **maximizing** this term.

Minimize sensitivity by **maximizing** this term.

But the **total** of the three terms must equal this!

Resolving this conflict is a subject choice of the amplifier designer. However, here is a "rule-of-thumb" procedure.

However, verify that these results satisfy your design requirements (or the requirements assigned to you by your boss and/or professor!).

1. Given the **desired value** of I_D, make **source voltage** $V_S = V_{DD}/4$, i.e. set the source resistor R_S to:

$$R_S = \frac{V_s}{I_D} = \frac{V_{DD}}{4I_D} \qquad (1)$$

This value reduces the sensitivity $d\,I_D/dK$!

2. Now determine the required value of V_{GS}. Since $I_D = K(V_{GS} - V_t)^2$, we find that V_{GS} should be:

$$V_{GS} = \sqrt{\frac{I_D}{K}} + V_t$$

3. Set the required value of **gate voltage** V_G.

Note that:

$$V_G = V_{GS} + V_S$$

Thus, we can **add** the results of the previous **two** steps to find the required value of the gate voltage V_G.

To set the gate voltage to this value, we must select the proper values of **resistors** R_1 and R_2.

Since the gate current is **zero** ($i_G = 0$), we find from voltage division that:

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right) = \frac{V_{DD}}{\left(\frac{R_1}{R_2}\right) + 1} \qquad (2)$$

Note this equation determines the **ratio** of resistors R_1 and R_2, but not the resistors themselves.

We need a **second** equation to explicitly determine the resistors values—the **sum** of the two resistances, for example.

We find that making the resistances R_1 and R_2 as **large** as possible is **very desirable**! This will typically maximize the amplifier input resistance, as well as result in minimum power dissipation.

As a result, we make the resistors as **large a practicable**. For **example**:

$$R_1 + R_2 = 250 \text{ K} \qquad (3)$$

4. Set the required value of DC **drain voltage** V_D.

Recall that:

a) we require $V_D \ll V_{DD} = L_+$ to avoid **cutoff** mode.

b) and, we require that $V_D \gg V_G - V_t = L$ to avoid **triode** mode.

Solution: set the drain voltage V_D to a value **half-way** between V_{DD} and $V_G - V_t$!

In other words, set the DC **drain voltage** to be:

$$V_D = \frac{V_{DD} + (V_G - V_t)}{2}$$

To achieve this, we must select the drain **resistor** R_D so that:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{V_{DD} - (V_G - V_t)}{2 I_D} \qquad (4)$$

Thus, use equations (1), (2), (3), and (4) to determine the **standard** DC bias design (i.e., R_1, R_2, R_S, and R_D) for MOSFET amplifiers.

*If I were you, I'd make sure I understood this material well enough that I could also bias a **non-standard** MOSFET amplifier problem.*

*It's not enough to simply know how, you must also know **why**!*