4.5 Biasing in BJT Amplifier Circuits

Reading **Assignment**: 280-286

Now let's examine how we DC bias MOSFETs **amplifiers**!

If we don't bias properly, distortion can result!

EXAMPLE: MOSFET AMPLIFIER DISTORTION

There is a classic bias circuit for **MOSFET amplifiers**; let's see what it is!

HO: MOSFET BIASING USING A SINGLE POWER SUPPLY

Let's do an **example** DC bias design.

EXAMPLE: BIASING OF DISCRETE MOSFET AMPLIFIERS

We can also use a DC current source to bias the Amplifier.

Q: *Yes, but just how do we construct a current source?*

A: HO:THE MOSFET CURRENT MIRROR

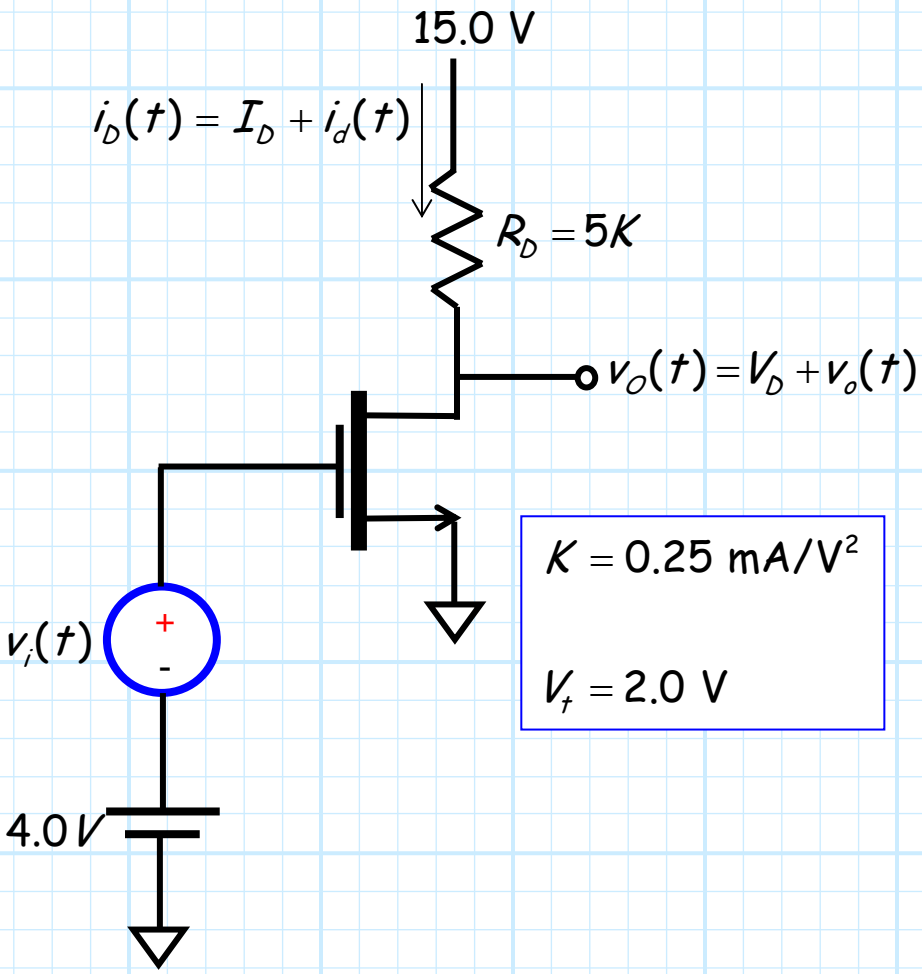
HO: CURRENT STEERING CIRCUITS

HO: MOSFET Biasing Using Current Mirrors

Example: MOSFET Biasing Using Current Mirrors

Example: MOSFET Amplifier Distortion

Recall this circuit from a **previous** handout:



We found that the small-signal **voltage gain** is:

$$A_{vo} = \frac{v_o(t)}{v_i(t)} = -5.0$$

Say the **input** voltage to this amplifier is:

$$v_i(t) = V_i \cos\omega t$$

Q: *What is the **largest** value that V_i can take without producing a **distorted** output?*

A: Well, we know that the **small-signal output** is:

$$\begin{aligned} v_o(t) &= A_{vo}\, v_i(t) \\ &= -5.0\, V_i \cos\omega t \end{aligned}$$

BUT, this is **not** the output voltage!

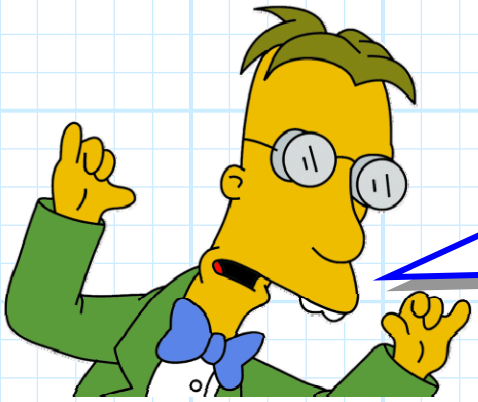
The **total** output voltage is the **sum** of the **small-signal** output voltage and the **DC** output voltage!

Note for this example, the **DC output** voltage is the **DC drain** voltage, and we recall we determined in an earlier handout that its value is:

$$V_O = V_D = 10 \text{ V}$$

Thus, the **total output voltage** is :

$$\begin{aligned} v_O(t) &= V_D + v_o(t) \\ &= 10.0 - 5.0\, V_i \cos\omega t \end{aligned}$$



*It is very important that you realize there is a **limit** on both how high and how low the **total** output voltage $v_o(t)$ can go!*

*That's right! If the **total** output voltage $v_o(t)$ tries to exceed these limits—even for a moment—theMOSFET will leave **saturation** mode.*

*And leaving saturation mode results in **signal distortion**!*

Let's break the problem down into **two** separate problems:

1) If **total** output voltage $v_O(t)$ becomes too **small**, the MOSFET will enter the **triode** mode.

2) If **total** output voltage $v_O(t)$ becomes too **large**, the MOSFET will enter **cutoff**.

We'll first consider **problem 1**.

For a MOSFET to remain in saturation, $v_{DS}(t)$ must remain **greater than** the excess gate voltage $(V_{GS} - V_t)$ for all time t.

$$v_{DS}(t) > V_{GS} - V_t$$

Since the source terminal of the MOSFET in **this** circuit is connected to ground, we know that $V_S = 0\ \text{V}$. Therefore:

$$v_{DS}(t) = v_D(t) = v_O(t) \qquad \text{and} \qquad V_{GS} = V_G$$

And so the MOSFET will remain in saturation **only** if the total output voltage remains **larger** than $V_{GS} - V_t = V_G - V_t$!

$$v_O(t) > V_G - V_t$$

Thus, we conclude for this amplifier that the output "floor" is:

$$L_- = V_G - V_t$$

And since $V_G = 4.0\,V$ and $V_t = 2.0\,V$, we find:

$$L_- = V_G - V_t = 4 - 2 = 2.0\,V$$

Thus, to remain in saturation, the **total** output voltage must remain larger than the "floor" voltage L_- for all time t:

$$v_O(t) > L_- = 2.0\,V$$

Since this **total** voltage is:

$$v_O(t) = 10.0 - 5.0\,V_i \cos\omega t$$

we can determine the **maximum** value of small-signal **input** magnitude V_i:

$$10.0 - 5.0\,V_i \cos\omega t > 2.0$$

$$\Rightarrow 8.0 > 5.0\,V_i \cos\omega t$$

$$\Rightarrow V_i \cos\omega t < 1.6$$

Since $\cos\omega t$ can be as large as 1.0, we find that the **magnitude** of the **input** voltage can be **no larger** than 1.6 V, i.e.,

$$V_i < 1.6 \text{ V}$$

If the **input** magnitude exceeds this value, the MOSFET will (momentarily) leave the saturation region and enter the dreaded **triode** mode!

Now let's consider **problem 2**

For the MOSFET to remain in saturation, the **drain** current must be **greater** than zero (i.e., $i_D > 0$). Otherwise, the MOSFET will enter **cutoff** mode.

Applying **Ohm's Law** to the drain resistor, we find the **drain current** is:

$$i_D = \frac{V_{DD} - v_O}{R_C} = \frac{15 - v_O}{5}$$

it is evident that drain current is **positive** only if $v_O < 15$ V.

In other words, the **upper** limit (i.e., the "ceiling") on the **total** output voltage is:

$$L_+ = V_{DD} = 15.0\,V$$

Since:

$$v_O(t) = 10.0 - 5.0\,V_i \cos\omega t$$

we can conclude that in order for the MOSFET to remain in **saturation** mode:

$$10 - 5.0\,V_i \cos\omega t > 15.0$$

Therefore, we find:

$$V_s \cos\omega t > \frac{-5.0}{5.0} = -1.0$$

Since $\cos\omega t \geq -1$, the above equation means that the **input** signal **magnitude** V_i can be **no larger** than:

$$V_i < 1.0 \text{ V}$$

If the input magnitude **exceeds** 1.0 V, the MOSFET will (momentarily) leave the saturation and enter the **cutoff** region!

In **summary**:

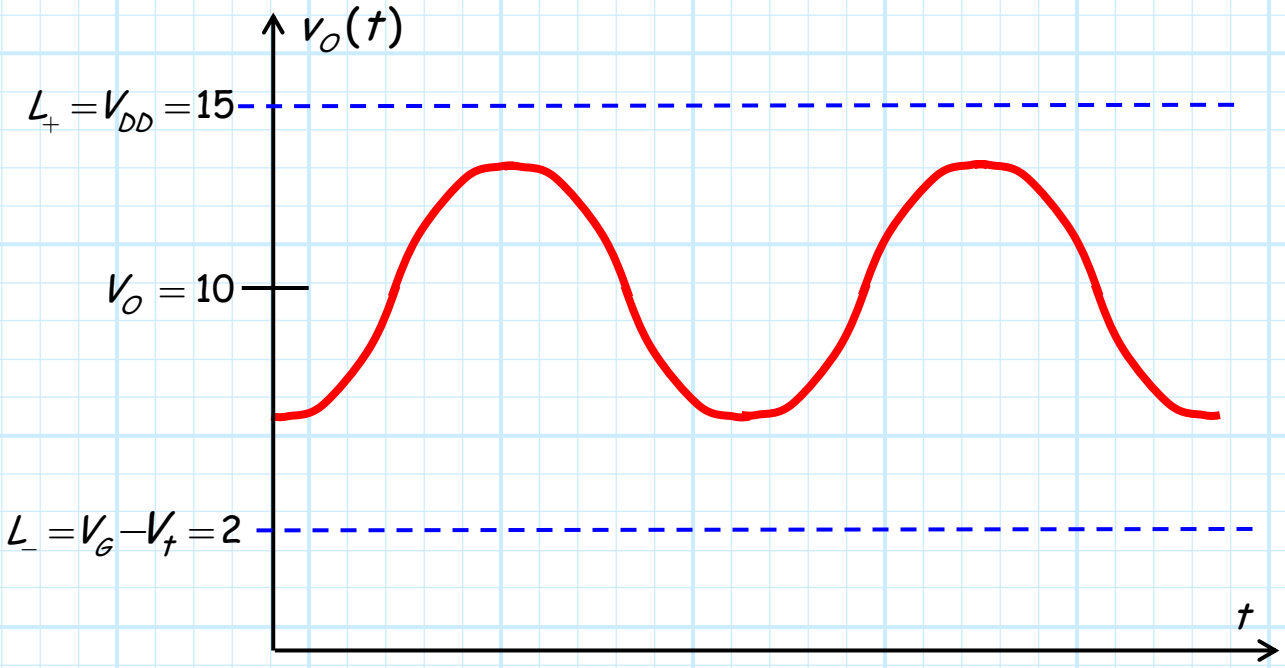
1) If $V_i > 1.6$ V, the MOSFET will at times enter **triode**, and **distortion** will occur!

2) If $V_i > 1.0$ V, the MOSFET will at times enter **cutoff**, and **even more** distortion will occur!

To demonstrate this, let's consider **three** examples:

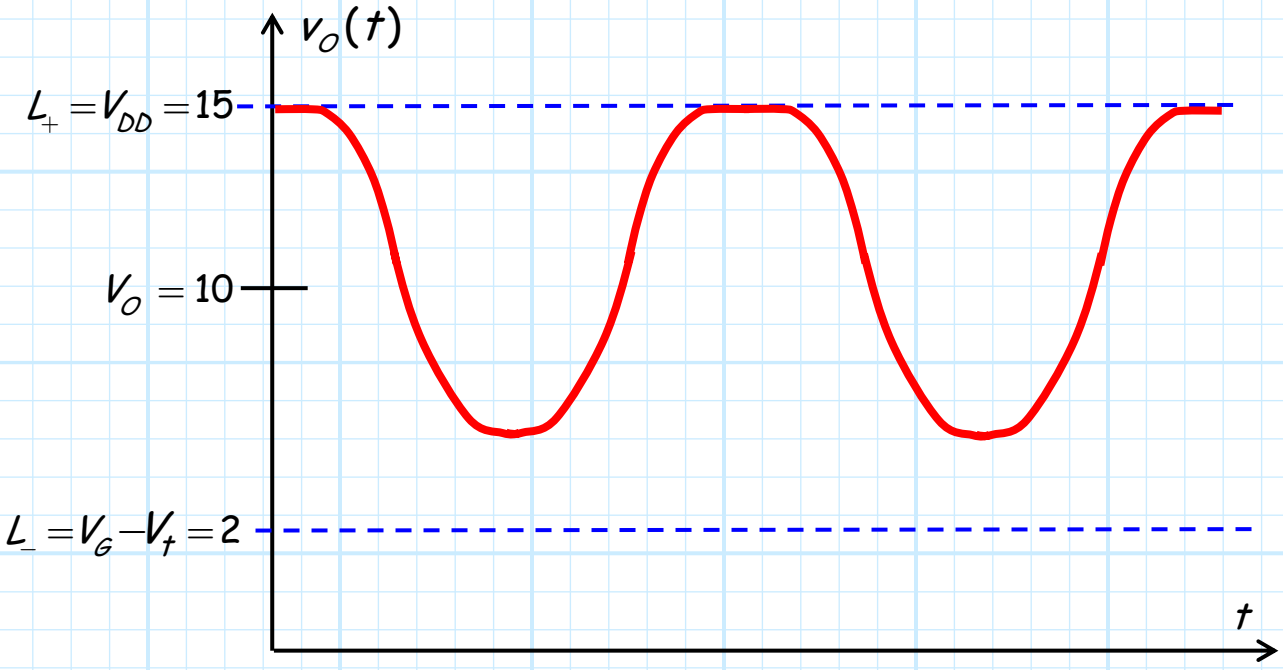
1. $V_i < 1.0$ V

The output signal in this case remains between $V_{DD} = 15.0$ and $V_G - V_t = 2.0$ V for **all** time t. Therefore, the output signal is **not distorted**.



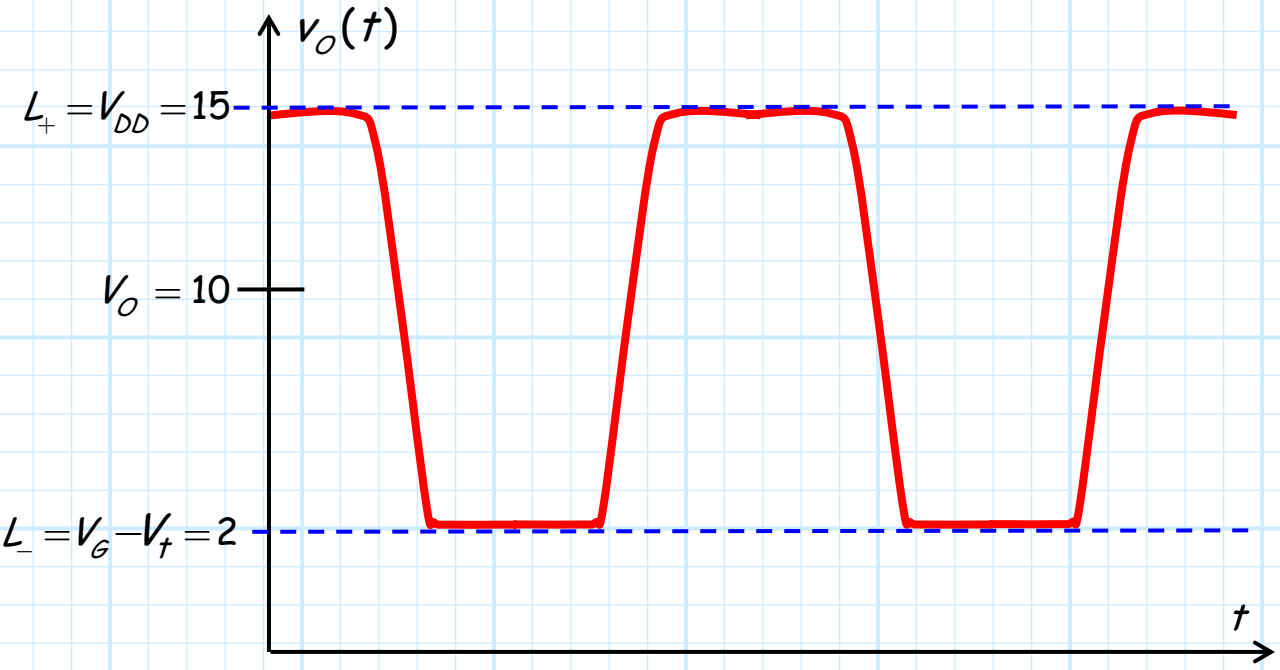
2. 1.6 V $> V_i >$ 1.0 V

The output signal in this case remains greater than $L_- = V_G - V_t = 2$ for all time t. However, the small-signal output is now large enough so that the total output voltage at times tries to **exceed** $L_+ = V_{DD} = 15$. For these times, the MOSFET will enter **cutoff**, and the output signal will be **distorted**.



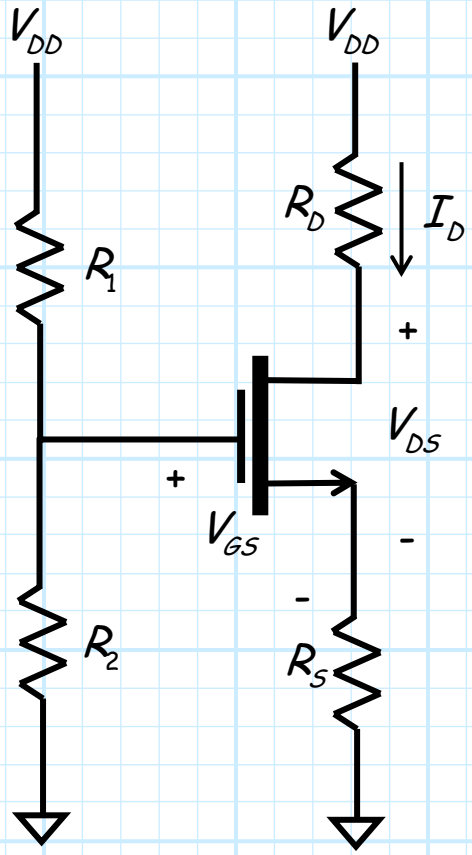
3. $V_i > 1.6\,V$

In this case, the small-signal input signal is sufficiently **large** so that the total output will attempt to exceed **both** limits (i.e., $V_{DD} = 15.0\,V$ and $V_G - V_t = 2.0\,V$). Therefore, there are periods of time when the MOSFE will be in **cutoff**, and periods when the MOSFET will be in **saturation**.



MOSFET Biasing using a Single Power Supply

The general form of a **single**-supply MOSFET amplifier biasing circuit is:



Just like BJT biasing, we typically attempt to satisfy three main bias design goals:

1) Maximize Gain

Typically, the small-signal **voltage gain** of a MOSFET amplifier will be proportional to transconductance g_m:

$$A_{vo} \propto g_m$$

Thus, to maximize the amplifier voltage gain, we must **maximize** the MOSFET transconductance.

Q: *What does this have to do with **D.C. biasing?***

A: Recall that the transconductance depends on the **DC excess gate voltage**:

$$g_m = 2K\left(V_{GS} - V_t\right)$$

Another way to consider transconductance is to express it in terms of DC drain current I_D. Recall this DC current is related to the DC excess gate voltage (in satureation!) as:

$$I_D = K\left(V_{GS} - V_t\right)^2 \qquad \Rightarrow \qquad \left(V_{GS} - V_t\right) = \sqrt{\frac{I_D}{K}}$$

And so transconductance can be alternatively expressed as:

$$g_m = 2K\left(V_{GS} - V_t\right) = 2K\sqrt{\frac{I_D}{K}} = 2\sqrt{KI_D}$$

Therefore, the amplifier voltage gain is typically **proportional** to the square-root of the DC drain current:

$$A_{vo} \propto \sqrt{I_D}$$

To maximize A_{vo}, maximize I_D

2) Maximize Voltage Swing

Recall that if the DC drain voltage V_D is biased too close to V_{DD}, then even a small small-signal drain voltage $v_d(t)$ can result in a **total** drain voltage that is too **large**, i.e.:

$$v_D(t) = V_D + v_d(t) \geq V_{DD}$$

In other words, the MOSFET enters **cutoff**, and the result is a **distorted** signal!

To avoid this (to allow $v_d(t)$ to be as large as possible without MOSFET entering cutoff), we need to bias our MOSFET such that the DC drain voltage V_D is as **small** as possible.

Note that the drain voltage is:

$$V_D = V_{DD} - R_D I_D$$

Therefore V_D is minimized by designing the bias circuit such that the DC drain current I_D is as **large** as possible.

However, we must **also** consider the signal distortion that occurs when the MOSFET enters **triod**. This of course is avoided if the total voltage drain-to-source remains greater than the excess gate voltage, i.e.:

$$v_{DS}(t) = V_{DS} + v_{ds}(t) > (V_{GS} - V_t)$$

Thus, to avoid the MOSFET triode mode—and the resulting signal distortion—we need to bias our MOSFET such that the DC voltage V_{DS} is as **large** as possible.

To minimize signal distortion, maximize V_{DS}

3) Minimize Sensitivity to changes in K, V_t

We find that MOSFETs are **sensitive** to temperature—specifically, the value of K is a function of temperature.

Likewise, the values of K and threshold voltage V_t are not particularly constant with regard to the manufacturing process.

Both of these facts lead to the requirement that our bias design be **insensitive** to the values of K and V_t. Specifically, we want to design the bias network such that the DC bias current does **not** change values when K and/or V_t does.

Mathematically, we can express this requirement as minimizing the value:

$$\frac{d\,I_D}{dK} \quad \text{and} \quad \frac{d\,I_D}{dV_t}$$

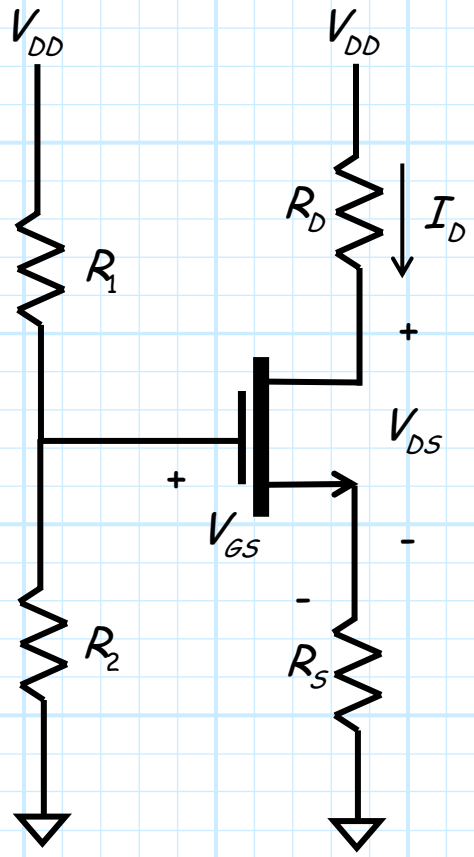
Similar to the BJT, we find that these derivatives are minimized by maximizing the value of **source resistor** R_S.

To minimize $d\,I_D/dK$, maximize R_S

So, let's **recap** what we have learned about designing our bias network:

1. Make I_D as large as possible.
2. Make V_{DS} as large as possible.
3. Make R_S as large as possible.

Again analogous to BJT biasing, we find that these three goals are conflicting, as they are constrained by the KVL equation of the bias circuit:



$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

or

$$I_D R_D + V_{DS} + I_D R_S = V_{DD}$$

Maximize A_{vo} by **maximizing** this term.

Minimize distortion by **maximizing** this term.

Minimize sensitivity by **maximizing** this term.

But the **total** of the three terms must equal this!

Resolving this conflict is a subject choice of the amplifier designer. However, here is a "rule-of-thumb" procedure.

However, verify that these results satisfy your design requirements (or the requirements assigned to you by your boss and/or professor!).

1. Given the **desired value** of I_D, make **source voltage** $V_S = V_{DD}/4$, i.e. set the source resistor R_S to:

$$R_S = \frac{V_s}{I_D} = \frac{V_{DD}}{4I_D} \qquad (1)$$

This value reduces the sensitivity $d\,I_D/dK$!

2. Now determine the required value of V_{GS}. Since $I_D = K(V_{GS} - V_t)^2$, we find that V_{GS} should be:

$$V_{GS} = \sqrt{\frac{I_D}{K}} + V_t$$

3. Set the required value of **gate voltage** V_G.

Note that:

$$V_G = V_{GS} + V_S$$

Thus, we can **add** the results of the previous **two** steps to find the required value of the gate voltage V_G.

To set the gate voltage to this value, we must select the proper values of **resistors** R_1 and R_2.

Since the gate current is **zero** ($i_G = 0$), we find from voltage division that:

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right) = \frac{V_{DD}}{\left(\frac{R_1}{R_2}\right) + 1} \qquad (2)$$

Note this equation determines the **ratio** of resistors R_1 and R_2, but not the resistors themselves.

We need a **second** equation to explicitly determine the resistors values—the **sum** of the two resistances, for example.

We find that making the resistances R_1 and R_2 as **large** as possible is **very desirable**! This will typically maximize the amplifier input resistance, as well as result in minimum power dissipation.

As a result, we make the resistors as **large a practicable**. For **example**:

$$R_1 + R_2 = 250 \text{ K} \qquad (3)$$

4. Set the required value of DC **drain voltage** V_D.

Recall that:

a) we require $V_D \ll V_{DD} = L_+$ to avoid **cutoff** mode.

b) and, we require that $V_D \gg V_G - V_t = L$ to avoid **triode** mode.

Solution: set the drain voltage V_D to a value **half-way** between V_{DD} and $V_G - V_t$!

In other words, set the DC **drain voltage** to be:

$$V_D = \frac{V_{DD} + (V_G - V_t)}{2}$$

To achieve this, we must select the drain **resistor** R_D so that:

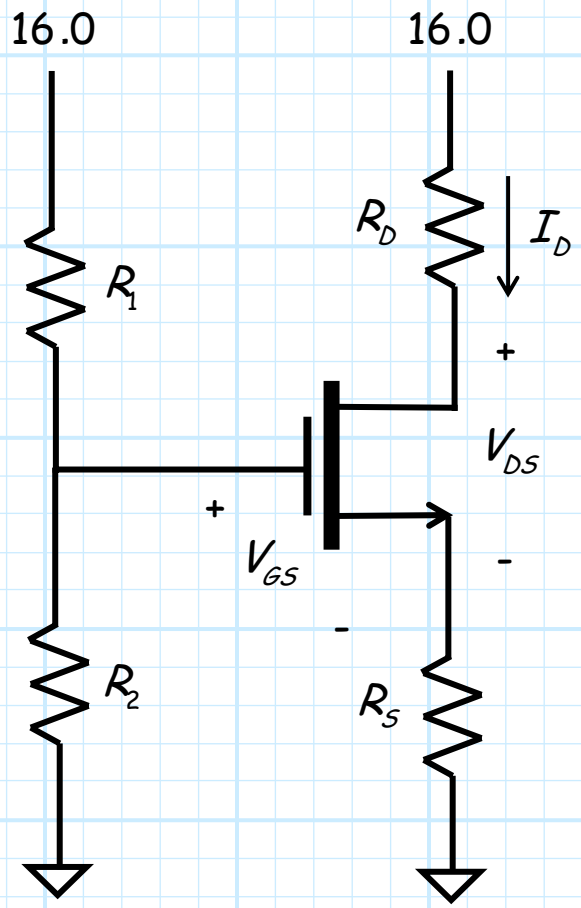
$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{V_{DD} - (V_G - V_t)}{2 I_D} \qquad (4)$$

Thus, use equations (1), (2), (3), and (4) to determine the **standard** DC bias design (i.e., R_1, R_2, R_S, and R_D) for MOSFET amplifiers.

*If I were you, I'd make sure I understood this material well enough that I could also bias a **non-standard** MOSFET amplifier problem.*

*It's not enough to simply know how, you must also know **why**!*

Example: Biasing of Discrete MOSFET Amplifiers



If the MOSFET has device values $K = 1.0\ mA/V^2$ and $V_t = 1.0\ V$, determine the resistor values to bias this MOSFET with a DC drain current of:

$$I_D = 4\ mA$$

1. Given the desired value of I_D, make **source voltage** $V_s = V_{DD}/4 = 4.0\ V$, i.e. set the source resistor R_S to:

$$R_S = \frac{V_s}{I_D} = \frac{4.0}{4.0} = 1\ K\Omega$$

2. Now determine the required value of V_{GS}. Since $I_D = K(V_{GS} - V_t)^2$, we find that V_{GS} should be:

$$\begin{aligned} V_{GS} &= \sqrt{\frac{I_D}{K}} + V_t \\ &= \sqrt{\frac{4.0}{1.0}} + 1.0 \\ &= 3.0 \text{ V} \end{aligned}$$

3. Set the required value of **gate voltage** V_G.

$$\begin{aligned} V_G &= V_{GS} + V_S \\ &= 3.0 + 4.0 \\ &= 7.0 \text{ V} \end{aligned}$$

Since the gate current is **zero** ($i_G = 0$), we find from voltage division that:

$$V_G = \frac{V_{DD}}{\left(R_1 \middle/ R_2\right) + 1}$$

Therefore:

$$\begin{aligned} R_1/R_2 &= \frac{V_{DD}}{V_G} - 1 \\ &= \frac{16.0}{7.0} - 1 \\ &= \frac{9}{7} \end{aligned}$$

We need a **second** equation to explicitly determine the resistors values—the **sum** of the two resistances, for example.

We make the resistors as large a practicable. For **example**:

$$R_1 + R_2 = 240 \text{ K}$$

Therefore:

$$\frac{9}{7} R_2 + R_2 = 240$$

$$\frac{16}{7} R_2 = 240$$

and thus:

$$R_1 = 135 \text{ K}\Omega \qquad \text{and} \qquad R_2 = 105 \text{ K}\Omega$$

4. Set the required value of DC **drain voltage** V_D.

Set the drain voltage V_D to a value **half-way** between V_{DD} and $V_G - V_t$!

In other words, set the DC **drain voltage** to be:

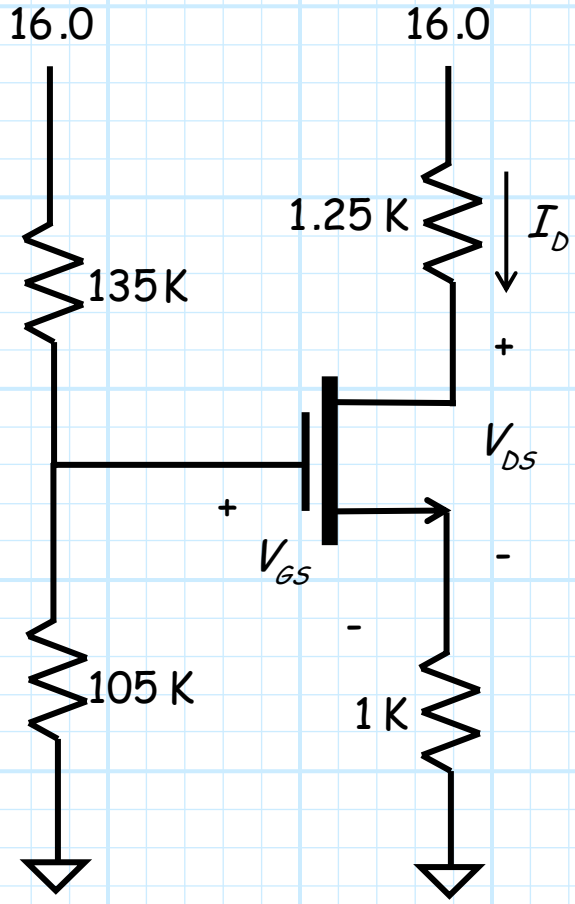
$$V_D = \frac{V_{DD} + (V_G - V_t)}{2}$$

$$= \frac{16 + (7.0 - 1.0)}{2}$$

$$= 11.0 \text{ V}$$

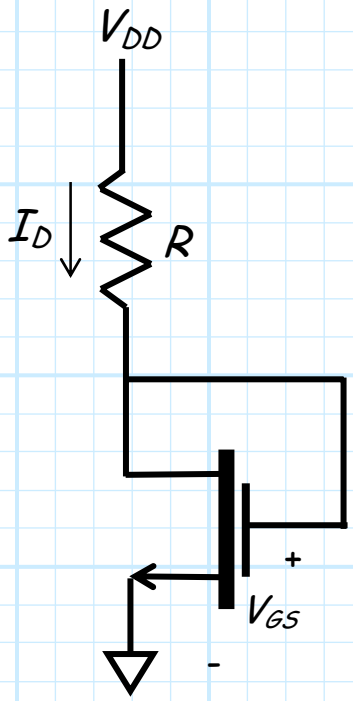
To achieve this, we must select the drain **resistor** R_D so that:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$
$$= \frac{16.0 - 11.0}{4.0}$$
$$= 1.25\ \text{K}\Omega$$



The MOSFET Current Mirror

Consider the following MOSFET circuit:



Note $V_D = V_G$, therefore:

$$V_{DS} = V_{GS}$$

and thus:

$$V_{DS} > V_{GS} - V_t$$

So, **if** $V_{GS} > V_t$, then the MOSFET is in **saturation**!

We know that for a MOSFET in saturation, the drain current is equal to:

$$I_D = K\left(V_{GS} - V_t\right)^2$$

Say we want this current I_D to be a **specific** value—call it I_{ref}.

Since $V_s = 0$, we find that from the above equation, the drain voltage must be:

$$V_D = \sqrt{\frac{I_{ref}}{K}} + V_t$$

Likewise, from KVL we find that:

$$I_{ref} = \frac{V_{DD} - V_D}{R}$$

And thus the **resistor** value to achieve the desired drain current I_{ref} is:

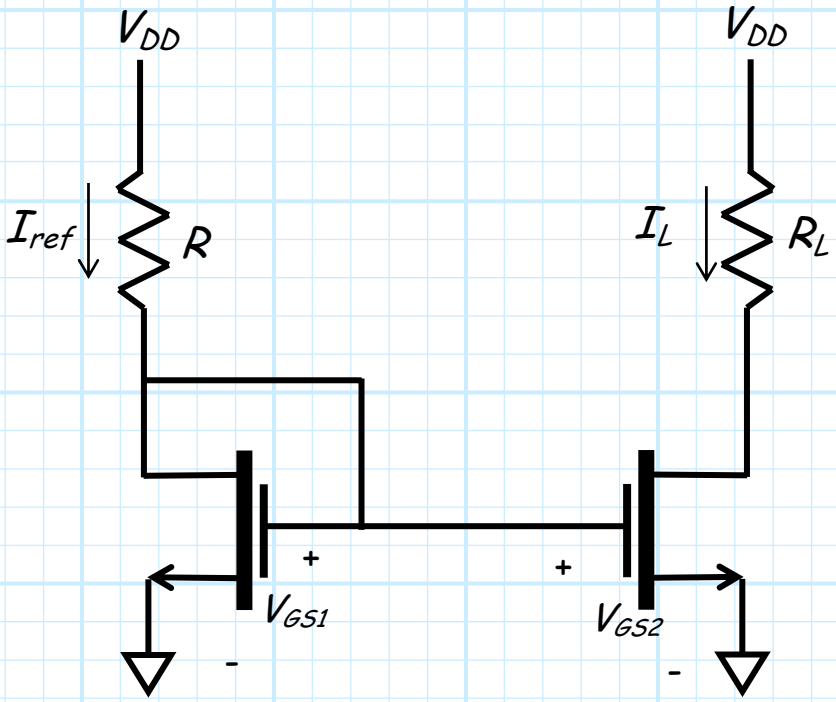
$$R = \frac{V_{DD} - V_D}{I_{ref}}$$

where:

$$V_D = \sqrt{\frac{I_{ref}}{K}} + V_t$$

Q: *Why are we doing this?*

A: Say we now add another component to the circuit, with a second MOSFET that is **identical** to the first :



Q: *So what is current I_L ?*

A: Note that the gate voltage of each MOSFET is the **same** (i.e., $V_{GS1} = V_{GS2}$), and if the MOSFETS are the **same** (i.e., $K_1 = K_2$, $V_{t1} = V_{t2}$), and if the second MOSFET is likewise in **saturation**, its drain current I_L is:

$$I_L = K_2 \left(V_{GS2} - V_{t2}\right)^2$$
$$= K_1 \left(V_{GS1} - V_{t1}\right)^2 = I_{ref}$$

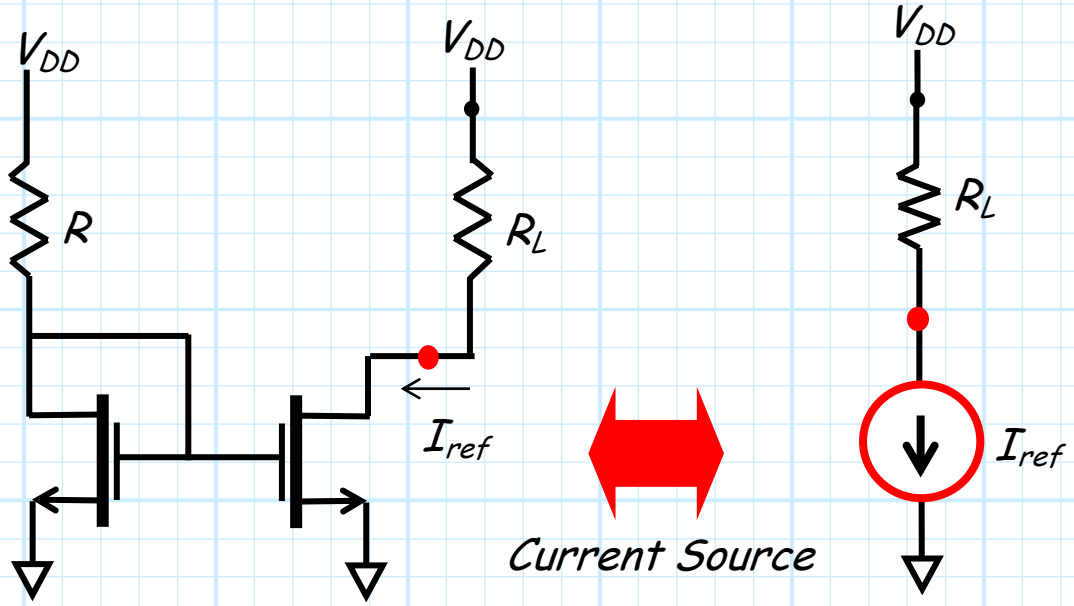
Therefore, the drain current of the **second** MOSFET is **equal** to the current of the **first**!

$$I_{ref} = I_L$$

Q: *Wait a minute! You mean to say that the current through the resistor R_L is **independent** of the value of resistor R_L ?*

A: Absolutely! As long as the second MOSFET is in **saturation**, the current through R_L is equal to I_{ref}—**period**.

The current through R_L is independent on the value of R_L (provided that the MOSFET remains in saturation). Think about what this means—this device is a **current source** !



Remember, the second MOSFET **must** be in saturation for the current through R_L to be a constant value I_{ref}. As a result, we find that:

$$V_{DS2} > V_{GS2} - V_{t2}$$

or for this example, since $V_s = 0$:

$$V_{D2} > V_{G2} - V_{t2}$$

Since $V_{D2} = V_{DD} - R_L I_{ref}$, we find that in order for the MOSFET to be in saturation:

$$V_{DD} - R_L I_{ref} > V_{G2} - V_{t2} = V_{G1} - V_{t1}$$

Or, sated another way, we find that the load resistor R_L can be **no larger** than:

$$R_L < \frac{V_{DD} - V_{G1} + V_{t1}}{I_{ref}}$$

Where we know that:

$$V_{G1} = V_{DD} - R\,I_{ref}$$

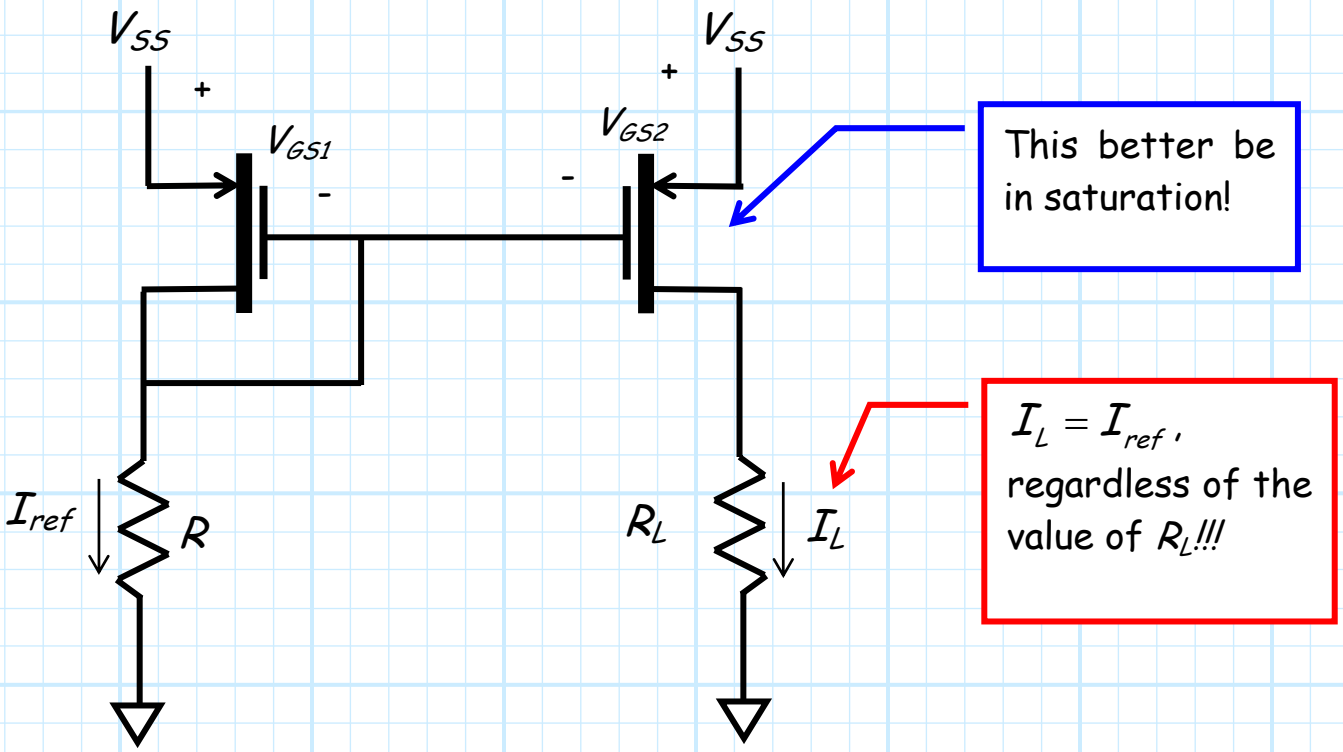
and thus we can alternatively write the above equation as:

$$R_L < R + \frac{V_{t1}}{I_{ref}}$$

If the **load** resistor becomes **larger** than $R + V_{t1}/I_{ref}$, the voltage V_{DS2} will drop **below** the excess gate voltage $V_{GS2} - V_{t2}$, and thus the second MOSFET will enter the **triode** region. As a result, the drain current will **not** equal I_{ref}—the current source will **stop working**!

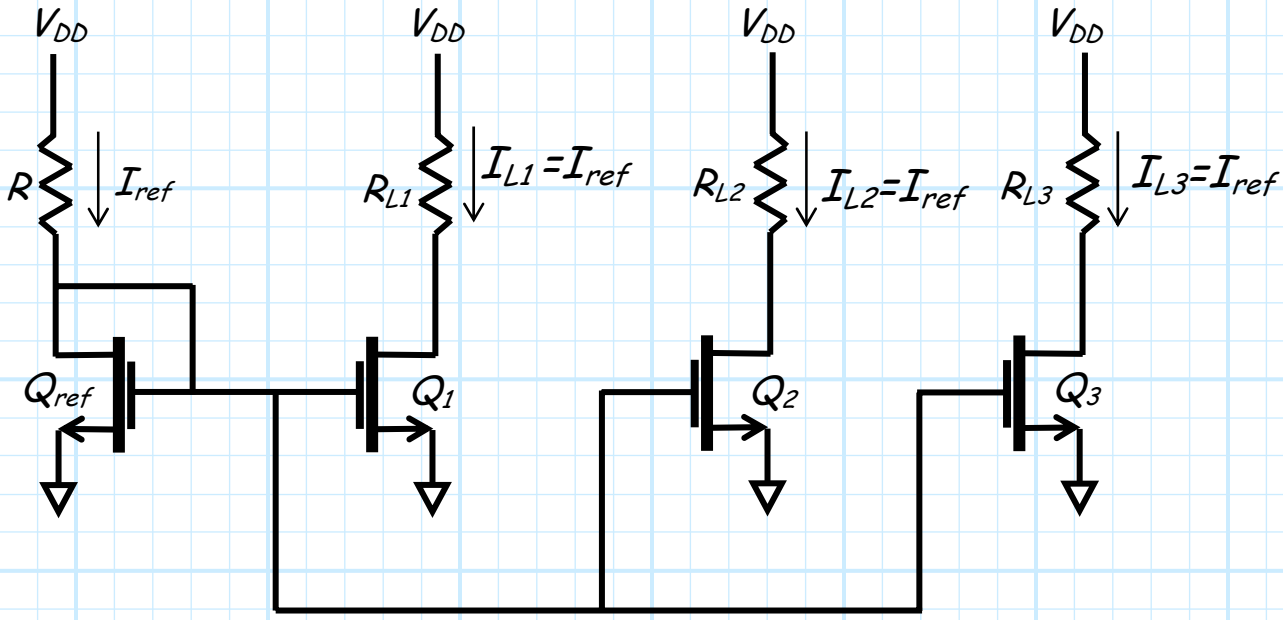
Although the circuit presented here is sometimes referred to as a current **sink**, understand that the circuit is clearly a way of designing a **current source**.

We can also use **PMOS** devices to construct a current mirror!



Current Steering Circuits

A current mirror may consist of **many** MOSFET current sources!



This circuit is particularly useful in integrated circuit design, where **one** resistor *R* is used to make **multiple** current sources.

Q: *What if we want to make the sources have **different** current values? Do we need to make **additional** current mirrors?*

A: NO!!

Recall that the current mirror simply ensures that the gate to source voltages of **each** transistor is **equal** to the gate to source voltage of the **reference**:

$$V_{GS}^{ref} = V_{GS1} = V_{GS2} = V_{GS3} = \cdots$$

Therefore, **if** each transistor is identical (i.e., $K_{ref} = K_1 = \cdots$, and $V_t^{ref} = V_{t1} = V_{t2} = \cdots$) then:

$$\begin{aligned} I_{ref} &= K_{ref}\left(V_{GS}^{ref} - V_t^{ref}\right)^2 \\ &= K_n\left(V_{GSn} - V_{tn}\right)^2 = I_{Dn} \end{aligned}$$

In other words, **if** each transistor Q_n is **identical** to Q_{ref}, then each current I_{Dn} will **equal** reference current I_{ref}.

But, consider what happens if the MOSFETS are not identical. Specifically, consider the case where $K_n \neq K_{ref}$ (but $V_{tn} = V_t^{ref}$).

Remember, we know that $V_{GSn} = V_{GS}^{ref}$ still, even when $K_n \neq K_{ref}$. Thus, the drain current I_{Dn} will now be:

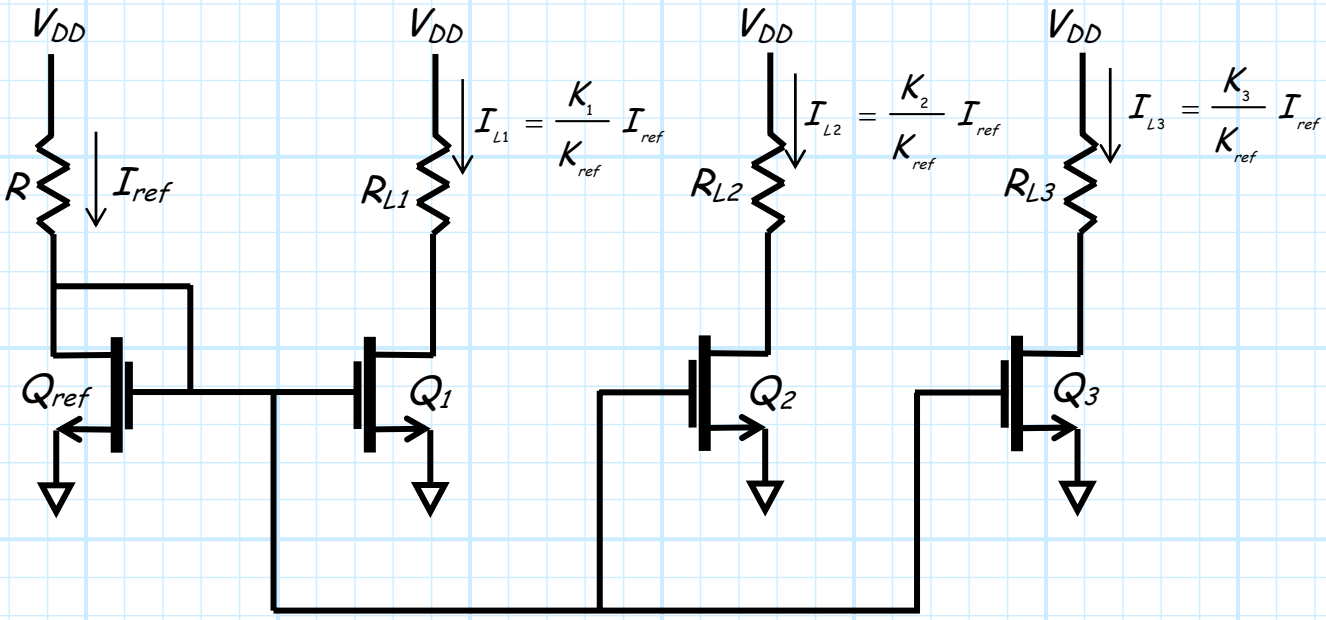
$$\begin{aligned} I_{Dn} &= K_n\left(V_{GSn} - V_{tn}\right)^2 \\ &= K_n\left(V_{GS}^{ref} - V_t^{ref}\right)^2 \\ &= K_n\left(\frac{I_{ref}}{K_{ref}}\right) \\ &= \left(\frac{K_n}{K_{ref}}\right) I_{ref} \end{aligned}$$

The drain current is a scaled value of I_{ref}!

For example, if K_1 is twice that of K_{ref} (i.e., $K_1 = 2K_{ref}$), then I_{D1} will be twice as large as I_{ref} (i.e., $I_1 = 2I_{ref}$).

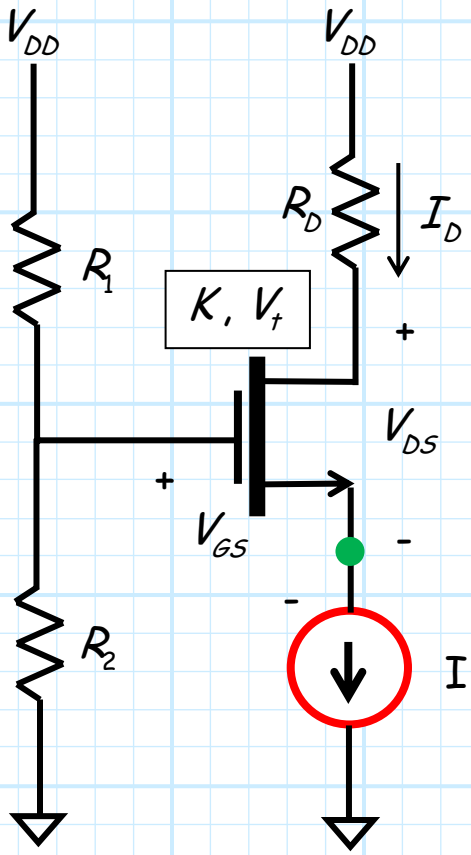
From the standpoint of integrated circuit design, we can change the value of K by modifying the MOSFET channel **width-to-length ratio** (W/L) for each transistor.

$$\frac{K_n}{K_{ref}} = \frac{\frac{1}{2}k'\left(W/L\right)_n}{\frac{1}{2}k'\left(W/L\right)_{ref}} = \frac{\left(W/L\right)_n}{\left(W/L\right)_{ref}}$$



MOSFET Biasing using a Current Mirror

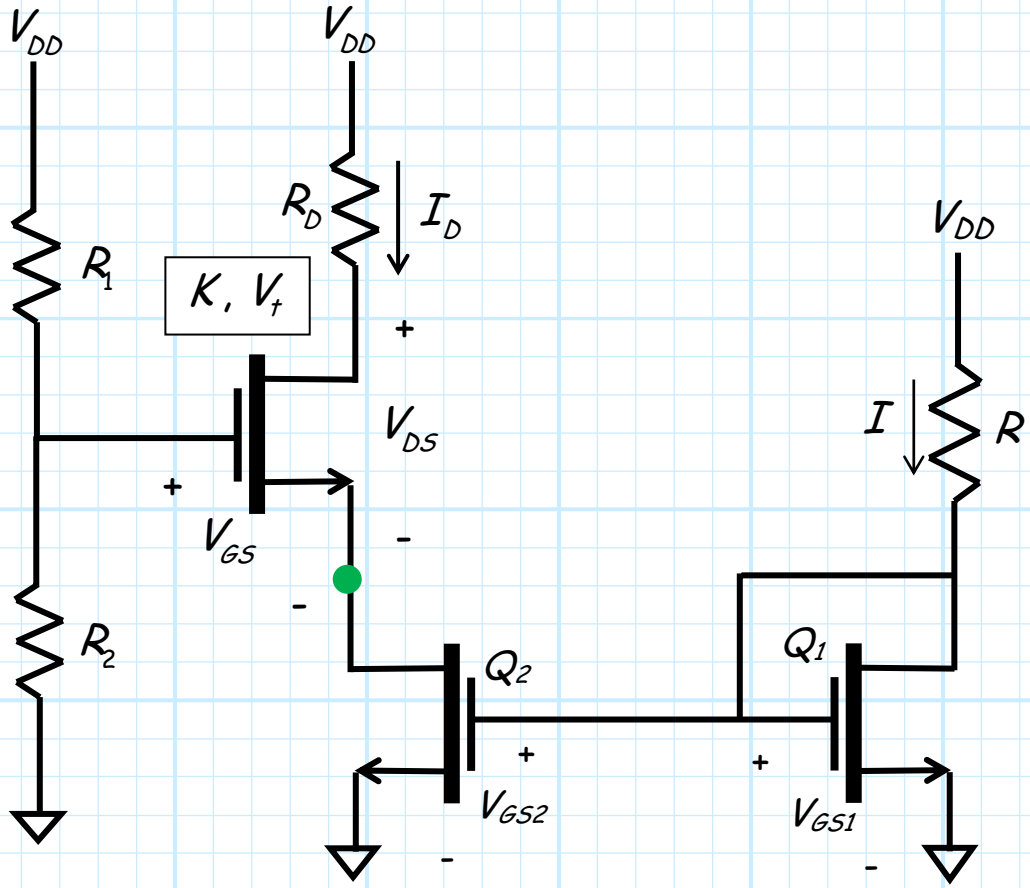
Just as with BJT amplifiers, we can likewise bias a MOSFET amplifier using a **current source**:



It is evident that the DC drain current I_D, is equal to the current source I, **regardless** of the MOSFET values K or V_t!

Thus, this bias design maximizes drain current **stability**!

We now know how to implement this bias design with MOSFETs—we use the **current mirror** to construct the current source!



Since $I_D = I$, it is evident that V_{GS} **must** be equal to:

$$V_{GS} = \sqrt{\frac{I}{K}} + V_t$$

and since the DC **gate** voltage is:

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

It is evident that the DC **source** voltage V_S is thus:

$$V_S = V_G - V_{GS}$$
$$= V_{DD}\left(\frac{R_2}{R_1 + R_2}\right) - \left(\sqrt{\frac{I}{K}} + V_t\right)$$

Since we are biasing with a current source, we do **not** need to worry about drain current **stability**—the current source will determine the DC drain current for **all** conditions (i.e., $I_D = I$).

We might conclude therefore, that we should make DC source voltage V_S as **small** as possible. After all, this would allow us to **maximize** the output voltage swing (i.e., maximize $I_D R_D$ and V_{DS}).

Note however, that the **source** voltage V_S of the MOSFET is numerically equal to the **drain** voltage V_{D2} (and thus V_{DS2}) of the second MOSFET of the **current mirror**.

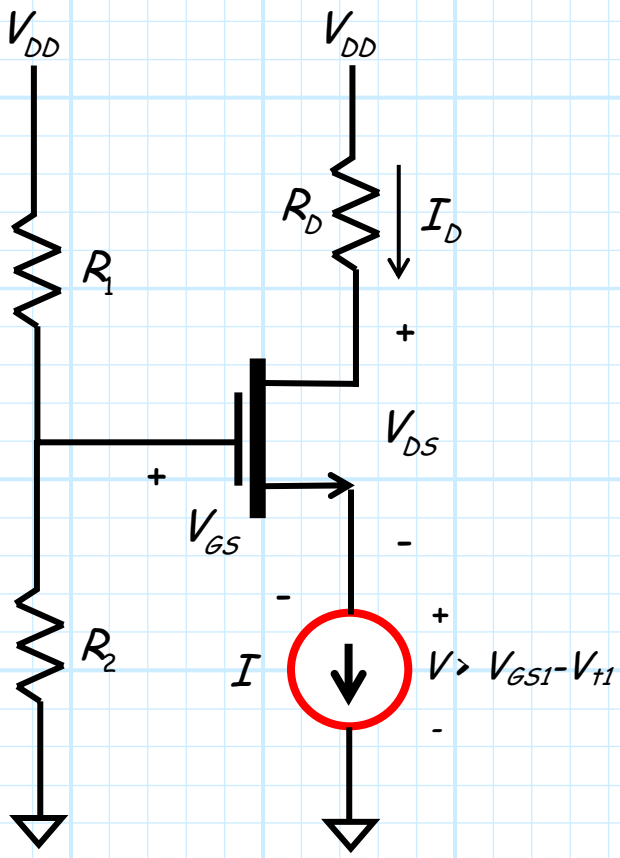
Q: *So what?!*

A: The voltage $V_{DS2} = V_S$ must be **greater** than:

$$V_{GS2} - V_{t2} = V_{GS1} - V_{t1}$$
$$= \left(V_{DD} - I_{ref} R\right) - V_{t1}$$

in order for the **second** MOSFET to remain in **saturation**.

There is a **minimum voltage** across the current source in order for the current source to properly operate!



Thus, to maximize output swing, we **might** wish to set:

$$V_S = V_{GS1} - V_{t1}$$

(although to be practical, we should make V_S **slightly greater** than this to allow for some design **margin**).

Q: *How do we "set" the DC* ***source*** *voltage V_S ??*

A: By setting the DC **gate** voltage V_G !!

Recall that the DC voltage V_{GS} is determined by the DC current source value I:

$$V_{GS} = \sqrt{\frac{I}{K}} + V_t$$

and the DC gate voltage is determined by the **two** resistors R_1 and R_2:

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

Thus, we should **select** these resistors such that:

$$V_G = V_{GS} + V_S$$
$$= \left(\sqrt{\frac{I}{K}} + V_t\right) + \left(V_{GS1} - V_{t1}\right)$$

Q: *So what should the value of resistor R_D be?*

A: Recall that we should set the DC **drain** voltage V_D:

a) much **less** than V_{DD} to avoid **cutoff**.

b) much **greater** than $V_G - V_t$ to avoid **triode**.

Thus, we **compromise** by setting the DC drain voltage to a point **halfway** in between!

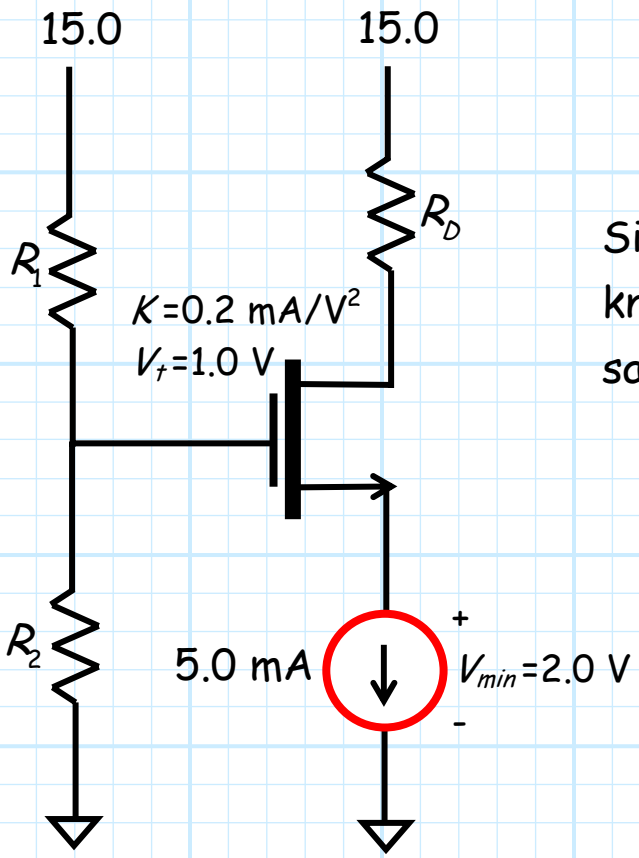
$$V_D = \frac{V_{DD} + \left(V_G - V_t\right)}{2}$$

To achieve this, we must select the drain **resistor** R_D so that:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{V_{DD} - \left(V_G - V_t\right)}{I_D}$$

Example: MOSFET Biasing using a Current Mirror

Let's determine the proper resistor values to DC bias this MOSFET. The current source is 5.0 mA and has a minimum voltage of 2.0 Volts in order to operate properly



Since $I = I_D = 5.0\,\text{mA}$, we know that V_{GS} will be (if in saturation):

$$V_{GS} = \sqrt{\frac{I}{K}} + V_t$$
$$= \sqrt{\frac{5.0}{0.2}} + 1.0$$
$$= 6.0\,\text{V}$$

Assuming that we want the DC source voltage to be the minimum value of $V_S = 2.0$, we nee for the DC gate voltage to be:

$$V_G = V_{GS} + V_S$$
$$= 6.0 + 2.0$$
$$= 8.0\,\text{V}$$

Thus, we need to select resistors R_1 and R_2 so that:

$$V_G = 8.0 = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

or in other words, we want:

$$\left(\frac{R_2}{R_1 + R_2}\right) = \frac{8.0}{15.0}$$

Since we can make R_1 and R_2 large, let's assume that we want:

$$R_1 + R_2 = 300\,\text{K}$$

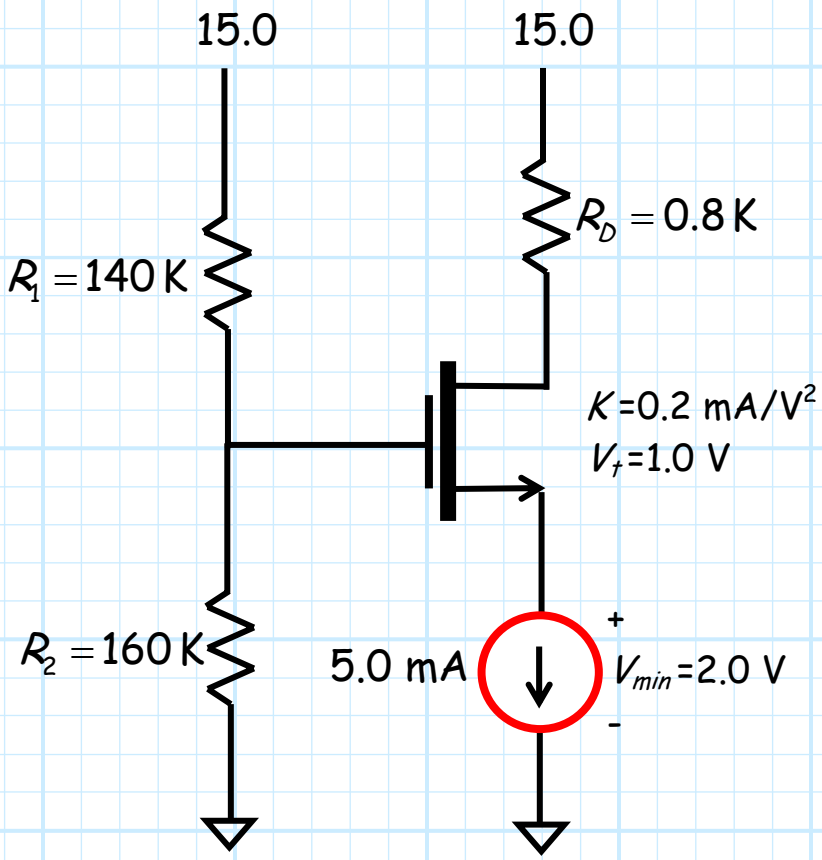
So that $R_1 = 140\ \text{K}\Omega$ and $R_2 = 160\ \text{K}\Omega$.

Finally, we want the DC drain voltage to be:

$$\begin{aligned} V_D &= \frac{V_{DD} + (V_G - V_t)}{2} \\ &= \frac{15.0 + (8.0 - 1.0)}{2} \\ &= 11.0\,\text{V} \end{aligned}$$

So that the resistor R_D is:

$$\begin{aligned} R_D &= \frac{V_{DD} - V_D}{I_D} \\ &= \frac{15.0 - 11.0}{5.0} \\ &= 0.8\,\text{K}\Omega \end{aligned}$$


15.0
15.0
$R_D = 0.8\,K$
$R_1 = 140\,K$
$K = 0.2\ mA/V^2$
$V_t = 1.0\ V$
$R_2 = 160\,K$
5.0 mA
+
$V_{min} = 2.0\ V$
-