D.C Biasing using a Single Power Supply

The general form of a single-supply BJT amplifier biasing circuit is:

\[ V_{cc} \]
\[ R_1 \]
\[ \downarrow \]
\[ R_2 \]
\[ \downarrow \]
\[ R_E \]
\[ \downarrow \]
\[ I_C \]
\[ V_{CE} \]

\[ V_{ee} \]
\[ R_2 \]
\[ \downarrow \]
\[ R_E \]
\[ \downarrow \]
\[ + \]
\[ V_{EC} \]

\[ V_{cc} \]
\[ R_C \]
\[ \downarrow \]
\[ - \]
\[ V_{CE} \]

\[ V_{ee} \]
\[ R_1 \]
\[ \downarrow \]
\[ R_C \]
\[ \downarrow \]
\[ I_C \]

\[ V_{ee} \]
\[ R_E \]
\[ \downarrow \]
\[ + \]
\[ V_{EC} \]
Just three goals

Generally, we have three goals in designing a biasing network:

1) Maximize Gain

Typically, we seek to set the operating point of the BJT amplifier such that the resulting small signal voltage gain is maximized.

However, we sometimes seek to set the bias point such that the output resistance is minimized, or the input resistance is maximized.

2) Maximize Voltage Swing

We seek to set the operating point of the BJT amplifier such that the maximum small signal output can be as large as possible.

If we make $V_{CE}$ too small, then the BJT will easily saturate, whereas if $V_{CE}$ is too large, the BJT will easily cutoff.
This suddenly seems like a lot of goals

3) Minimize Sensitivity to changes in $\beta$

Manufacturing and temperature variances will result in significant changes in the value $\beta$.

We seek to design the bias network such that the amplifier parameters will be insensitive to these changes.

Q: You're kidding me right?

We're supposed to achieve all these goals with just four resistors?

A: Actually, the three design goals listed above are often in conflict.

We typically have to settle for a compromise DC bias design.
How we maximize gain

Let’s take a closer look at each of the three design goals:

1) **Maximize Gain**

Typically, the small-signal voltage gain of a BJT amplifier will be proportional to transconductance $g_m$:

$$A_v \propto g_m$$

Thus, to maximize the amplifier voltage gain, we must maximize the BJT transconductance.

**Q:** What does this have to do with D.C. biasing?

**A:** Recall that the transconductance depends on the DC collector current $I_C$:

$$g_m = \frac{I_C}{V_T}$$
Maximize that darn bias current!

Therefore the amplifier voltage gain is typically proportional to the DC collector current:

\[ A_v \propto \frac{I_c}{V_T} \]

We of course can't decrease the thermal voltage \( V_T \), but we can design the bias circuit such that \( I_c \) is maximized.

To maximize \( A_v \), maximize \( I_c \)
We don’t want distortion!

2) Maximize Voltage Swing

Recall that if the DC collector voltage $V_C$ is biased too close to $V_{cc}$, then even a small small-signal collector voltage $v_c(t)$ can result in a total collector voltage that is too large, i.e.:

$$v_c(t) = V_C + v_c(t) \geq V_{cc}$$

In other words, the BJT enters cutoff, and the result is a distorted signal!

To avoid this (to allow $v_c(t)$ to be as large as possible without BJT entering cutoff), we need to bias our BJT such that the DC collector voltage $V_C$ is as small as possible.
How to avoid cutoff

Note that the collector voltage is:

\[ V_c = V_{cc} - R_c I_c \]

Therefore \( V_c \) is minimized by designing the bias circuit such that the DC collector current \( I_c \) is as large as possible.

Q: Hey hey! It looks like amplifier bias design is going to be easy. We can both maximize transconductance \( g_m \) and minimize the DC collector voltage \( V_c \) by maximizing the DC collector current \( I_c \)!

A: Just a second! We must also consider the signal distortion that occurs when the BJT enters saturation.
But also avoid saturation

Saturation of course is avoided if the total voltage collector to emitter remains greater than 0.7 V, i.e.:

\[ v_{ce}(t) = V_{ce} + v_{ce}(t) > 0.7 \text{ V} \]

Thus, to avoid BJT saturation—and the resulting signal distortion—we need to bias our BJT such that the DC voltage \( V_{CE} \) is as large as possible.

To minimize signal distortion, maximize \( V_{CE} \)
BJTs are pretty sensitive

3) Minimize Sensitivity to changes in $\beta$

We find that BJTs are very sensitive to temperature—specifically, the value of $\beta$ is a function of temperature.

Likewise, the value of $\beta$ is not particularly constant with regard to the manufacturing process.

We find that 100 otherwise “identical” BJTs will result have 100 different values of $\beta$!

Both of these facts lead to the requirement that our bias design be insensitive to the value of $\beta$.

Specifically, we want to design the bias network such that the DC bias currents (e.g., $I_C$) do not change values when $\beta$ does.

Mathematically, we can express this requirement as minimizing the value:

$$\frac{d I_C}{d \beta}$$
How do we determine this derivative?

Let’s determine this derivative value for our standard bias network:

Q: Yuck! This looks like a disturbingly difficult circuit to analyze.

A: One way to simplify the analysis is to use a Thevenin’s equivalent circuit.

Specifically, replace this portion of the bias circuit with its Thevenin’s equivalent:
Good ol’ Thevenin’s!

We find that this equivalent circuit is:

\[ V_{cc} \left( \frac{R_2}{R_1 + R_2} \right) \]

The bias network can therefore be equivalently represented as:
You’re always having fun
if you’re doing calculus

If we ASSUME that the BJT is in active mode, then we ENFORCE the proper
equalities and ANALYZE this circuit to find collector current $I_C$:

$$I_C = \frac{\beta (V_{BB} - 0.7)}{(\beta + 1)R_E + R_B}$$

We find therefore that:

$$\frac{d I_C}{d \beta} = -\left(\frac{V_{BB} - 0.7}{\left(\frac{\beta}{R_E} + 1\right)^2}\right)$$

Note then that:

$$\lim_{R_E/R_B \to \infty} \frac{d I_C}{d \beta} = 0$$
Maximize that darn resistor!

In other words, if we wish to make the DC collector current insensitive to changes in $\beta$, we need to make:

$$R_E \gg R_B$$

We of course could accomplish this by making the base resistance $R_B = R_1 \parallel R_2$ small, but we will find out later that there are problems with doing this.

Instead, we can minimize the circuit sensitivity to changes in $\beta$ by maximizing the emitter resistor $R_E$.

To minimize $d I_C/d \beta$, maximize $R_E$
This seems so simple...

So, let’s recap what we have learned about designing our bias network:

1. Make $I_C$ as large as possible.
2. Make $V_{CE}$ as large as possible.
3. Make $R_E$ as large as possible.

Q: Seems easy enough! Let’s get started biasing BJT amplifiers!

A: Not so fast! We still have a serious problem.
...NOT!

To see what this problem is, write the KVL equation for the Collector-Emitter Leg of the Bias Network:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

or

$$I_C R_C + V_{CE} + I_E R_E = V_{CC}$$

Maximize $A_v$ by maximizing this term.

Minimize distortion by maximizing this term.

Minimize $\beta$ sensitivity by maximizing this term.

But the total of the three terms must equal this!
A logical compromise

**Q:** Yikes! It's like owing 3 really big guys $15 each, but having only $15 in your pocket.

What do we do?

**A:** Split the total voltage 3 ways (give each guy $5).

\[
I_C R_C = \frac{V_{CC}}{3}
\]

\[
V_{CE} = \frac{V_{CC}}{3}
\]

\[
I_E R_E = \frac{V_{CC}}{3}
\]

\[
I_C R_C + V_{CE} + I_E R_E = V_{CC}
\]
The result of this compromise

In other words, for an \textit{n}pn BJT, set:

\[
V_c = \frac{2}{3} V_{cc} \quad \text{and} \quad V_E = \frac{1}{3} V_{cc}
\]
Don’t forget $pnp$

Likewise, for a $pnp$ BJT, set:

\[ V_E = \frac{2}{3} V_{EE} \quad \text{and} \quad V_C = \frac{1}{3} V_{EE} \]
What should $I_C$ be?

**Q:** We have determined that the product $I_C R_C$ should be equal to $V_{cc}/3$.

We can of course accomplish this with a larger resistor $R_C$ and a smaller current $I_C$, or a larger current $I_C$ and a smaller resistor $R_C$. What should the value of $I_C$ be?

**A:** Generally speaking, the value of the DC collector current $I_C$ affects:

1) Voltage Gain ($g_m \rightarrow \infty$ as $I_C \rightarrow \infty$).

2) Input Resistance ($r_i \rightarrow 0$ as $I_C \rightarrow \infty$).

3) BJT Output Resistance ($r_o \rightarrow 0$ as $I_C \rightarrow \infty$).

4) Power Consumption ($P \rightarrow \infty$ as $I_C \rightarrow \infty$).

5) Amplifier Bandwidth ($BW \rightarrow \infty$ as $I_C \rightarrow \infty$).

The “best” value of collector current $I_C$ is a trade between these parameters.
There are two resistors left

Q: OK, we now have enough information to set $I_C, V_C,$ and $V_E,$ and thus
resistors $R_C$ and $R_E.$

But we still have two bias resistors left—$R_1$ and $R_2.$ How do we determine their
values?

A: Well, we have found that reducing $R_B = R_1 \parallel R_2$ decreases the circuit
sensitivity to $\beta \Rightarrow \text{This is good!}$

But, we will find that reducing $R_B = R_1 \parallel R_2$ will often decrease the amplifier input
resistance $R_i \Rightarrow \text{This is bad!}$

Also, we find that reducing $R_B = R_1 \parallel R_2$ will increase the power dissipation $\Rightarrow$
This is also bad!
A “rule of thumb”

\[ I_1 \approx \frac{V_{cc}}{R_1 + R_2} \quad \text{if} \quad I_1 \gg I_B \]

\[ P = V_{cc} I_1 \approx \frac{V_{cc}^2}{R_1 + R_2} \]

A general “rule of thumb” is to select the values of \( R_1 \) and \( R_2 \) so that \( I_C \) is:

\[ 0.1 I_C < I_1 < I_C \]

Remember, the resistors \( R_1 \) and \( R_2 \) also determine the base voltage \( V_B \), which should approximately be:

\[ V_B = V_{BE} + V_E = 0.7 + \frac{V_{cc}}{3} \]