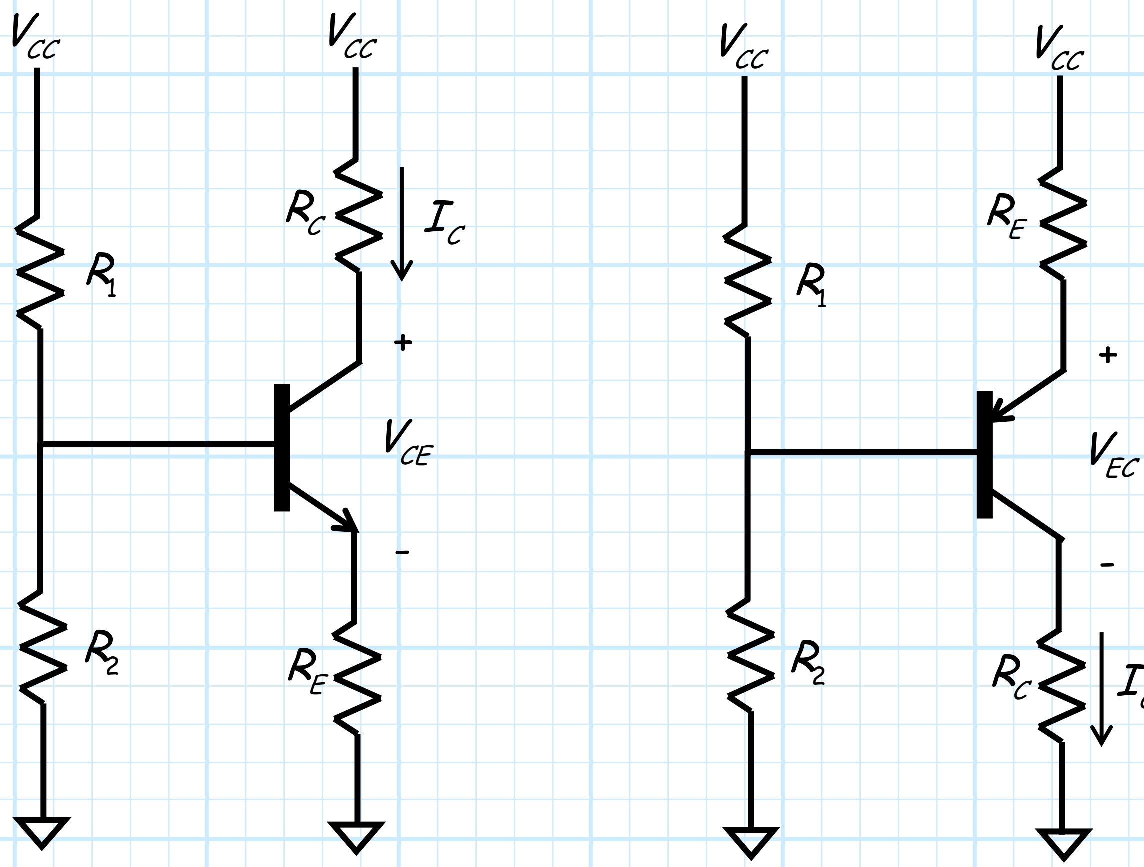
D.C Biasing using a Single Power Supply

The general form of a **single**-supply BJT amplifier biasing circuit is:



Generally, we have three goals in designing a biasing network:

1) Maximize Gain

Typically, we seek to set the operating point of the BJT amplifier such that the resulting small signal voltage gain is **maximized**.

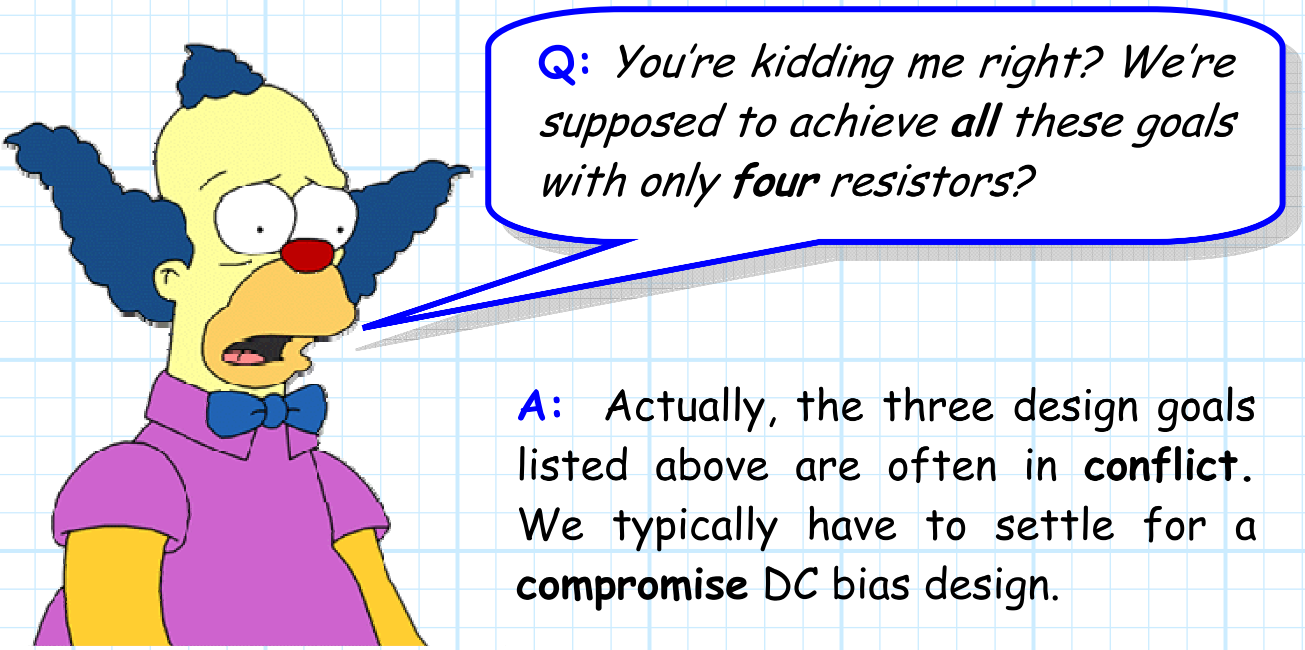
However, we sometimes seek to set the bias point such that the **output resistance** is minimized, or the **input resistance** is maximized.

2) Maximize Voltage Swing

We seek to set the operating point of the BJT amplifier such that the maximum small signal output can a **large** as possible. If we make V_{CE} too small, then the BJT will easily **saturate**, whereas if V_{CE} is too large, the BJT will easily **cutoff**.

3) Minimize Sensitivity to changes in β

Manufacturing and temperature variances will result in significant changes in the value β. We seek to design the bias network such that the amplifier parameters will be **insensitive** to these changes.



A: Actually, the three design goals listed above are often in **conflict.** We typically have to settle for a **compromise** DC bias design.

Let's take a closer look at each of the **three** design goals:

1) Maximize Gain

Typically, the small-signal **voltage gain** of a BJT amplifier will be proportional to transconductance g_m:

$$A_{vo} \propto g_m$$

Thus, to maximize the amplifier voltage gain, we must **maximize** the BJT transconductance.

Q: *What does this have to do with* ***D.C. biasing?***

A: Recall that the transconductance depends on the DC **collector current** I_C:

$$g_m = \frac{I_C}{V_T}$$

Therefore the amplifier voltage gain is typically **proportional** to the DC collector current:

$$A_{vo} \propto \frac{I_C}{V_T}$$

We of course can't decrease the thermal voltage V_T, but we can design the bias circuit such that I_C is **maximized**.

To maximize A_{vo}, maximize I_C

2) Maximize Voltage Swing

Recall that if the DC collector voltage V_C is biased too close to V_{CC}, then even a small small-signal collector voltage $v_c(t)$ can result in a **total** collector voltage that is too **large**, i.e.:

$$v_C(t) = V_C + v_c(t) \geq V_{CC}$$

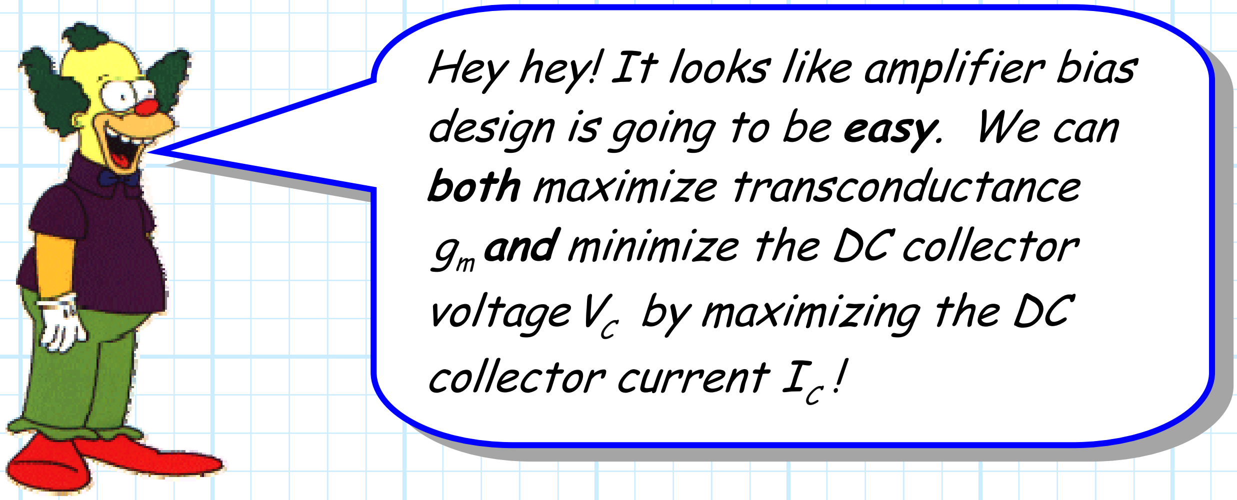
In other words, the BJT enters **cutoff**, and the result is a **distorted** signal!

To avoid this (to allow $v_c(t)$ to be as large as possible without BJT entering cutoff), we need to bias our BJT such that the DC collector voltage V_C is as **small** as possible.

Note that the collector voltage is:

$$V_C = V_{CC} - R_C I_C$$

Therefore V_C is minimized by designing the bias circuit such that the DC collector current I_C is as **large** as possible.



Just a second! We must **also** consider the signal distortion that occurs when the BJT enters **saturation**. This of course is avoided if the total voltage collector to emitter remains greater than 0.7 V, i.e.:

$$v_{CE}(t) = V_{CE} + v_{ce}(t) > 0.7 \text{ V}$$

Thus, to avoid BJT saturation—and the resulting signal distortion—we need to bias our BJT such that the DC voltage V_{CE} is as **large** as possible.

To minimize signal distortion, maximize V_{CE}

3) Minimize Sensitivity to changes in β

We find that BJTs are very **sensitive** to temperature—specifically, the value of β is a function of temperature.

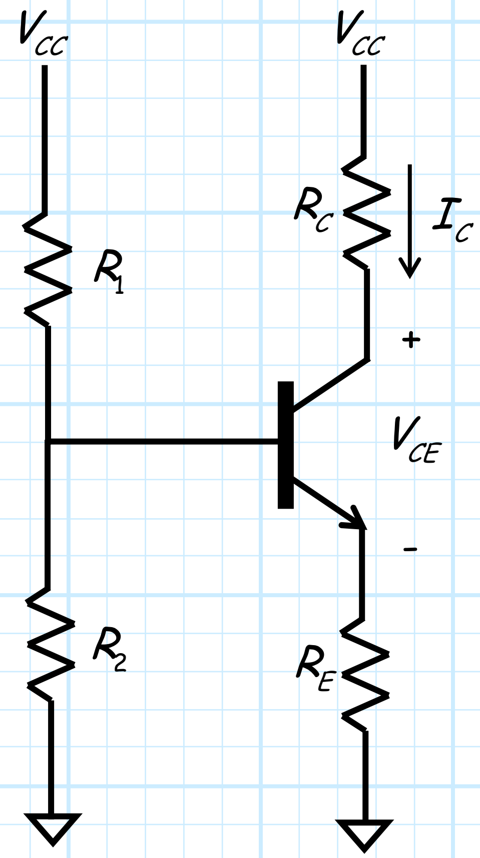
Likewise, the value of β is not particularly constant with regard to the manufacturing process. We find that 100 otherwise "identical" BJTs will result have 100 **different** values of β!

Both of these facts lead to the requirement that our bias design be **insensitive** to the value of β. Specifically, we want to design the bias network such that the DC bias currents (e.g., I_C) do **not** change values when β does.

Mathematically, we can express this requirement as minimizing the value:

$$\frac{d\,I_C}{d\,\beta}$$

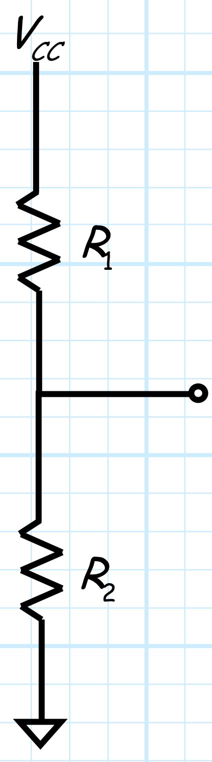
Let's determine this value for our **standard** bias network:



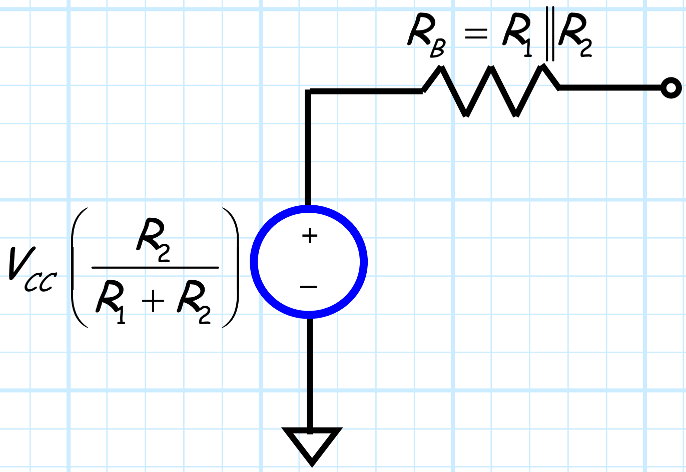
Q: *Yuck! This looks like a disturbingly difficult circuit to analyze.*

A: One way to **simplify** the analysis it to use a **Thevenin's** equivalent circuit.

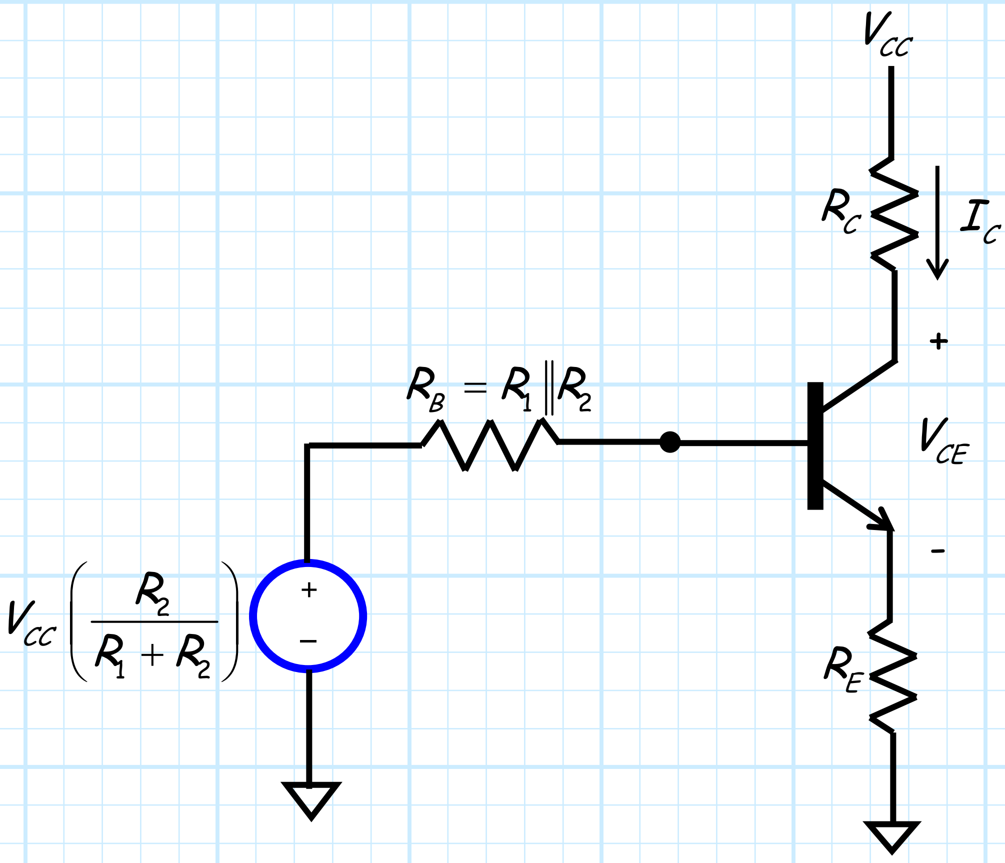
Specifically, replace this portion of the bias circuit with its Thevenin's equivalent:



We find that this equivalent circuit is:



The bias network can therefore be equivalently represented as:



If we **ASSUME** that the BJT is in active mode, then we **ENFORCE** the proper equalities and **ANALYZE** this circuit to find collector current I_C:

$$I_C = \frac{\beta\left(V_{BB} - 0.7\right)}{\left(\beta + 1\right) R_E + R_B}$$

We find therefore that:

$$\frac{d\, I_C}{d\beta} = \frac{-\left(V_{BB} - 0.7\right)}{\left(\beta \dfrac{R_E}{R_B} + 1\right)^2}$$

Note then that:

$$\lim_{R_E/R_B \to \infty} \frac{d\, I_C}{d\beta} = 0$$

In other words, if we wish to make the DC collector current **insensitive** to changes in β, we need to make:

$$R_E \gg R_B$$

We of course could accomplish this by making the **base resistance** $R_B = R_1 \| R_2$ small, but we will find out later that there are problems with doing this.

Instead, we can minimize the circuit sensitivity to changes in β by maximizing the **emitter resistor** R_E.

> To minimize $d\, I_C / d\,\beta$, maximize R_E

So, let's **recap** what we have learned about designing our bias network:

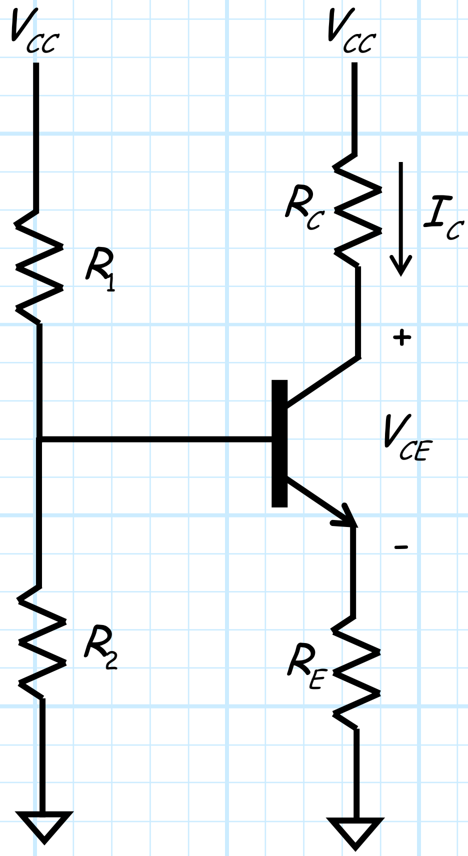
1. Make I_C as large as possible.

2. Make V_{CE} as large as possible.

3. Make R_E as large as possible.

Seems easy enough! Let's get started biasing BJT amplifiers!

Not so fast! We have a **serious problem**. To see what this problem is, write the KVL equation for the Collector-Emitter Leg of the Bias Network:



$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

or

$$I_C R_C + V_{CE} + I_E R_E = V_{CC}$$

Maximize A_{vo} by **maximizing** this term.

Minimize distortion by **maximizing** this term.

Minimize β sensitivity by **maximizing** this term.

But the **total** of the three terms must equal this!

Q: ***Yikes!*** *It's like owing 3 really big guys \$15 each, but having only \$15 in your pocket.*

What do we do?

A: Split the total voltage **3 ways** (give each guy \$5).

I.E., set:

$$I_C\,R_C = \frac{V_{CC}}{3}$$

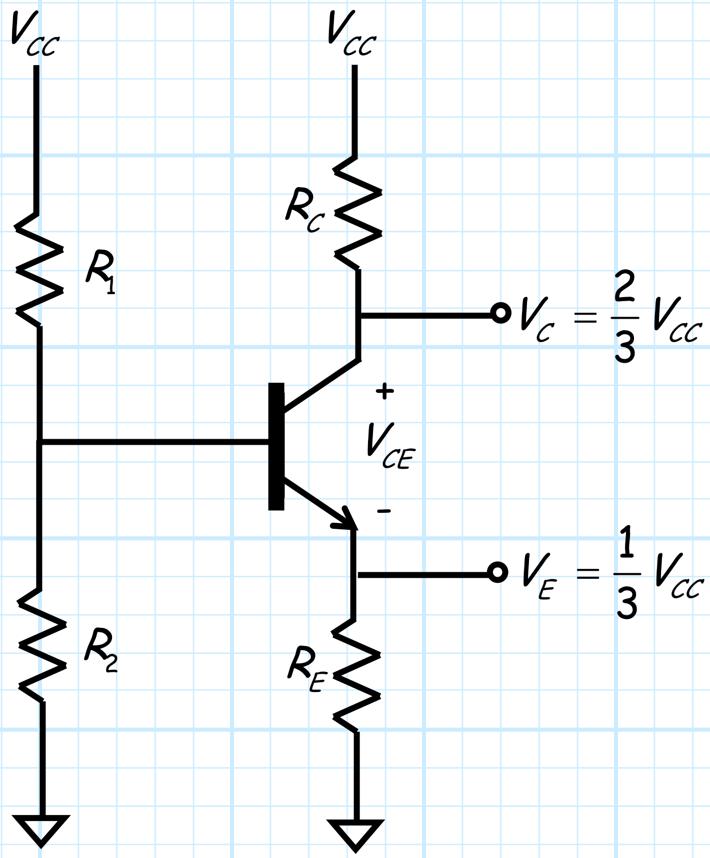
$$V_{CE} = \frac{V_{CC}}{3}$$

$$+ \qquad I_E\,R_E = \frac{V_{CC}}{3}$$

$$I_C R_C + V_{CE} + I_E R_E = V_{CC}$$

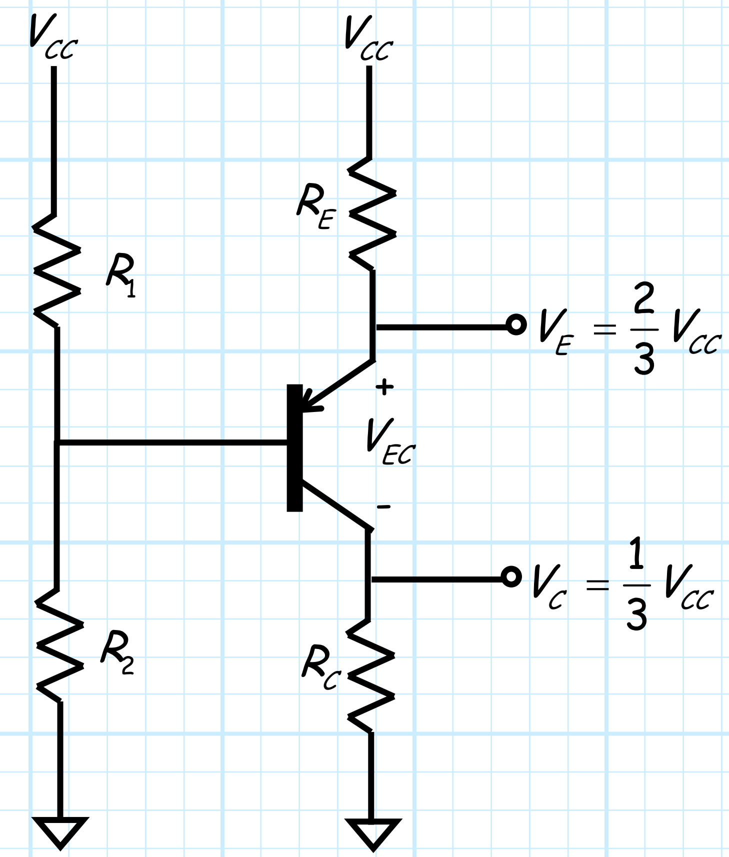
In other words, for an *npn* BJT, set:

$$V_C = \frac{2}{3} V_{CC} \qquad \text{and} \qquad V_E = \frac{1}{3} V_{CC}$$



Likewise, for a *pnp* BJT, set:

$$V_E = \frac{2}{3} V_{CC} \qquad \text{and} \qquad V_C = \frac{1}{3} V_{CC}$$



Q: *We have determined that the **product** $I_C R_C$ should be equal to $V_{CC}/3$. We can of course accomplish this with a larger resistor R_C and a smaller current I_C, **or** a larger current I_C and a smaller resistor R_C. What **should** the value of I_C be?*

A: Generally speaking, the value of the **DC collector current** I_C affects:

1) Voltage Gain ($g_m \rightarrow \infty$ as $I_C \rightarrow \infty$).

2) Input Resistance ($r_\pi \rightarrow 0$ as $I_C \rightarrow \infty$).

3) BJT Output Resistance ($r_o \rightarrow 0$ as $I_C \rightarrow \infty$).

4) Power Consumption ($P \rightarrow \infty$ as $I_C \rightarrow \infty$).

5) Amplifier Bandwidth ($BW \rightarrow$ "∞" as $I_C \rightarrow \infty$).

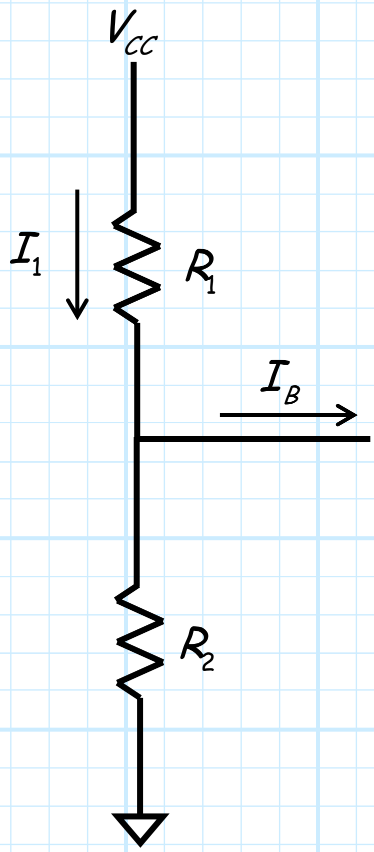
The "best" value of collector current I_C is a **trade** between these parameters.

Q: *OK, we now have enough information to set I_C, V_C, and V_E, and thus resistors R_C and R_E. But we still have **two** bias resistors left--R_1 and R_2. How do we determine there values?*

A: Well, we have found that reducing $R_B = R_1 \| R_2$ decreases the circuit sensitivity to $\beta \Rightarrow$ This is **good**!

But, we will find that reducing $R_B = R_1 \| R_2$ will often decrease the amplifier input resistance $R_i \Rightarrow$ This is **bad**!

Also, we find that reducing $R_B = R_1 \| R_2$ will increase the power dissipation $\Rightarrow$ This is also **bad**!



$$I_1 \approx \frac{V_{CC}}{R_1 + R_2} \qquad \text{if } I_1 \gg I_B$$

$$\therefore \; P = V_{CC}\, I_1 \approx \frac{V_{CC}^2}{R_1 + R_2}$$

A general "**rule of thumb**" is to select the values of R_1 and R_2 so that I_C is:

$$0.1 I_C < I_1 < I_C$$

Remember, the resistors R_1 and R_2 also determine **the base voltage** V_B, which should approximately be:

$$\begin{aligned} V_B &= V_{BE} + V_E \\ &= 0.7 + \frac{V_{CC}}{3} \end{aligned}$$