5.5 Biasing in BJT Amplifier Circuits

Reading **Assignment**: 436-442

Now let's examine how we DC bias BJTs **amplifiers**!

HO: A GRAPHICAL ANALYSIS OF BJT AMPLIFIERS

If we don't bias properly, distortion can result!

EXAMPLE: AMPLIFIER DISTORTION

There is a classic bias circuit for BJT amplifiers; let's see what it is!

HO:DC BIASING USING A SINGLE POWER SUPPLY

We can also use a DC current source to bias the BJT.

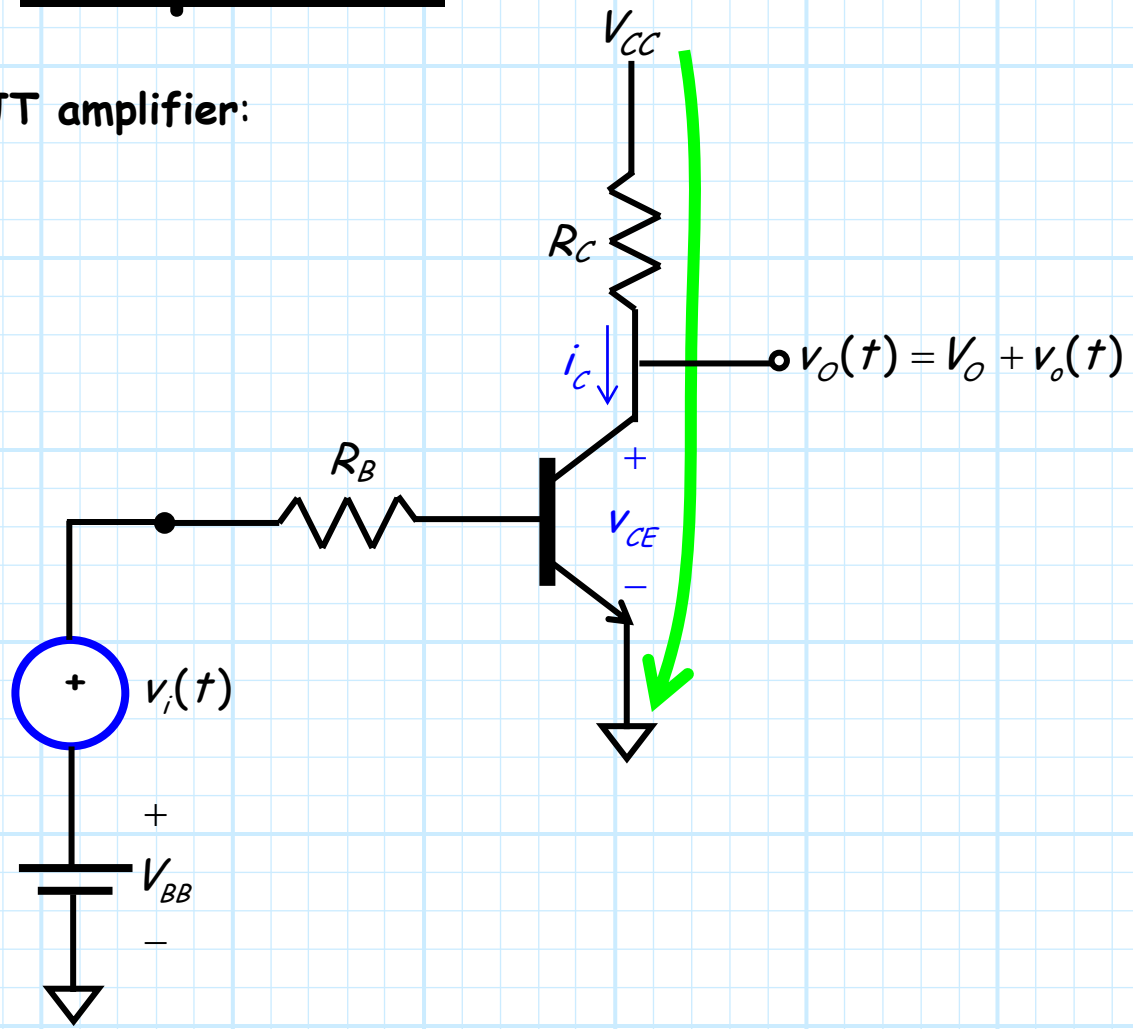
HO:BJT BIASING USING A CURRENT SOURCE

Let's do an example DC bias design.

EXAMPLE: SINGLE-SUPPLY DC BIAS

Graphical Analysis of a BJT Amplifier

Consider again this simple **BJT amplifier**:



We note that for this amplifier, the **output** voltage is equal to the **collector-to-emitter** voltage ($v_O(t) = v_{CE}(t)$).

y = m x + b

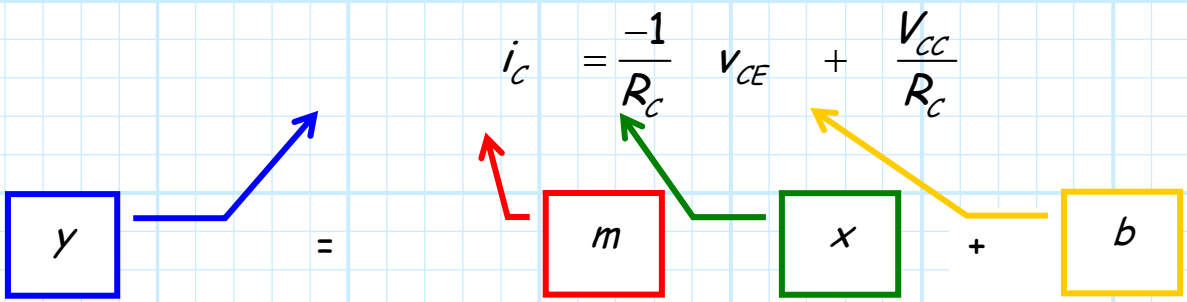
If we apply **KVL** to the collector-emitter leg, we find:

$$V_{CC} - i_C R_C - v_{CE} = 0$$

We can rearrange this to get an expression for the **collector current** i_C in terms of voltage v_{CE} (i.e., $i_C = f(v_{CE})$):

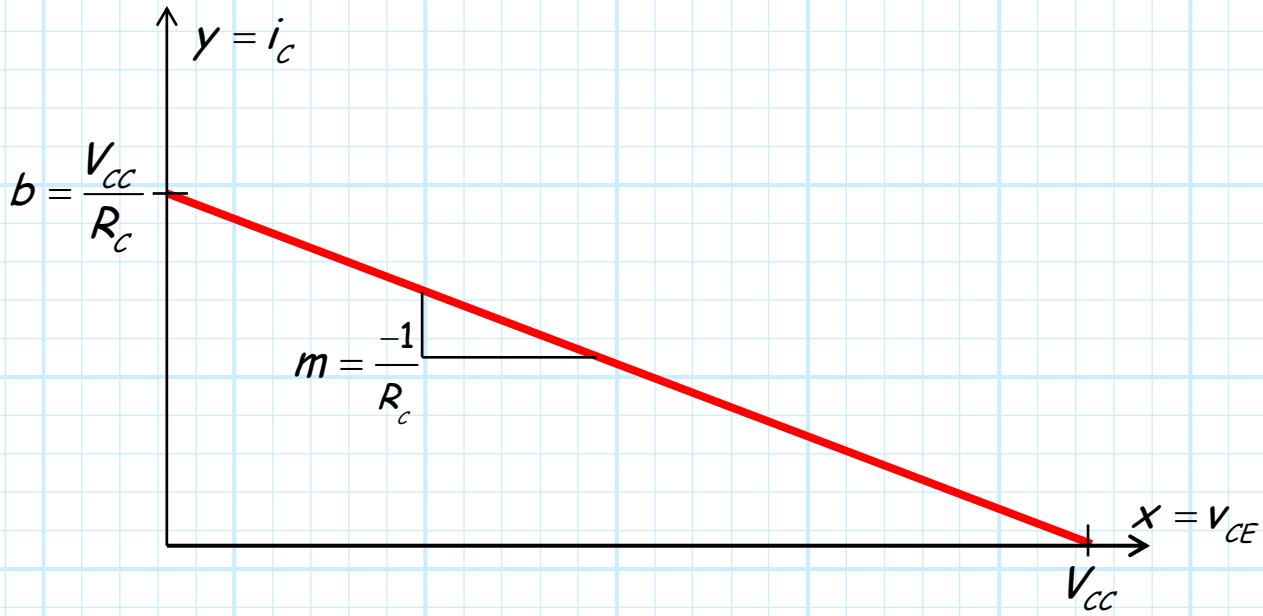
$$i_C = \frac{1}{R_C} v_{CE} + \frac{V_{CC}}{R_C}$$

Note this is an equation of a **line**!



The load line

This equation is referred to as the amplifier's **load line**, which we can graphically represent as:



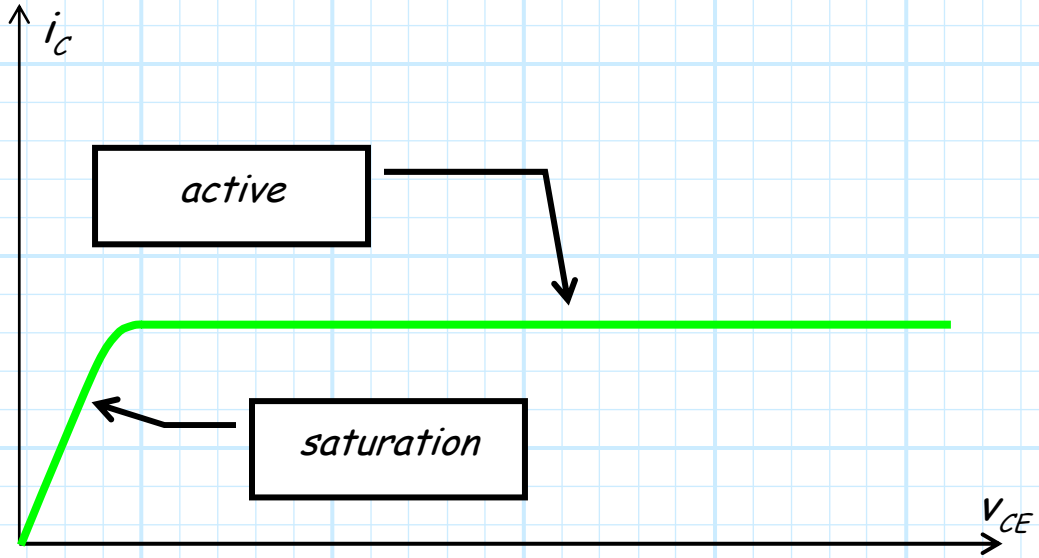
The load line provides the **circuit** relationship (via KVL) between i_C and v_{CE}.

→ The value of i_C and v_{CE} **must** lie somewhere along the load line!

i_C vs v_{CE} for a BJT

Exactly where on the load line depends on the **device** (BJT) relationship between i_C and v_{CE}.

Recall that this relationship is:

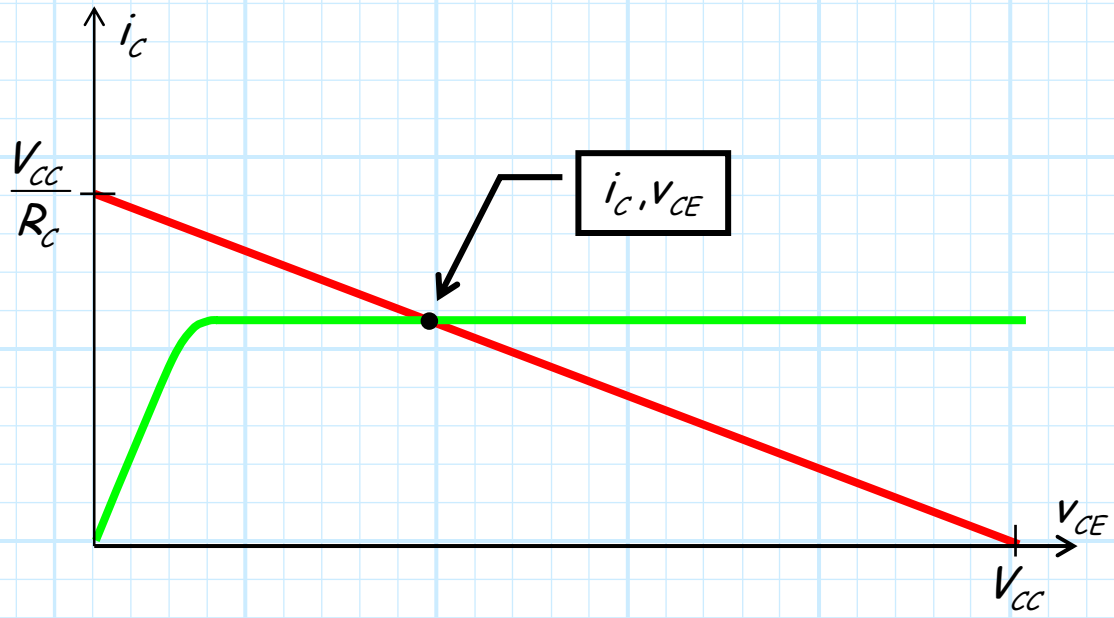


➡ The value of i_C and v_{CE} **must** also lie somewhere along this device curve!

Sort of like the Grandview triangle

Q: *How can the values for i_C and v_{CE} **simultaneously** be a point on the load line, and a point on the device (BJT) curve?*

A: Easy! the values for i_C and v_{CE} lie at the point where the two curves **intersect**!



But it all depends on the input!

Of course, the values of i_C and v_{CE} depend on the **input** to the amplifier:

$$v_I(t) = V_{BB} + v_i(t)$$

As the voltage $v_I(t)$ changes, so will the values i_C and v_{CE}.

Note, however, that the load line will **not** change—the slope $-1/R_C$ and y-intercept V_{CC}/R_C are **independent** of voltage $v_I(t)$.

What **does** change is the **BJT** relationship between i_C and v_{CE}.

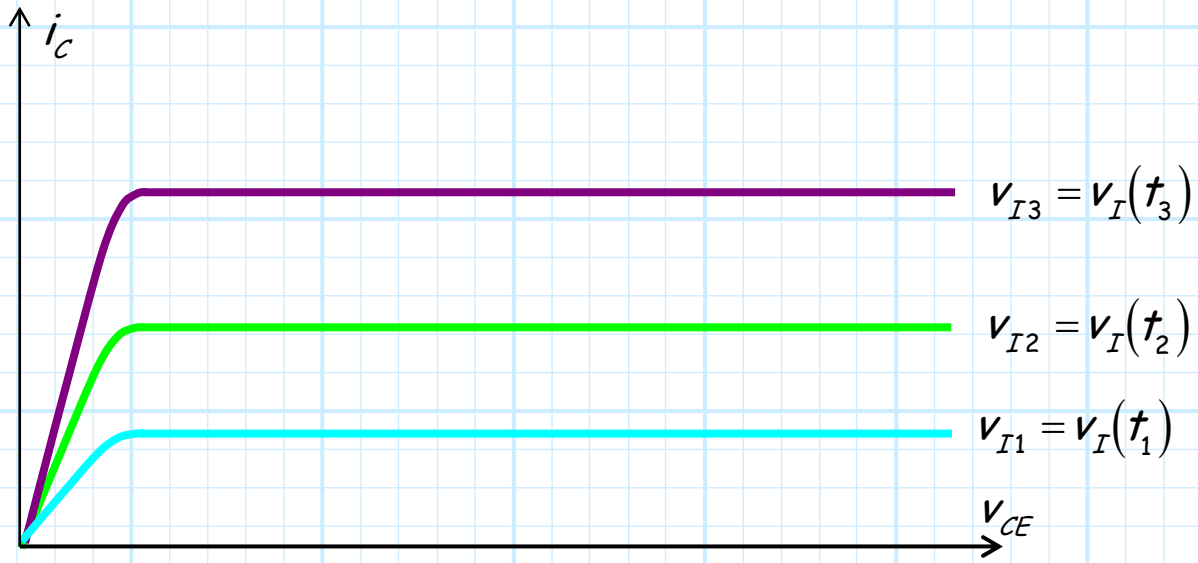
For example, in active mode, the collector current i_C is **independent** of v_{CE} (we're ignoring the Early effect)!

However, the collector current i_C of a BJT **is** dependent on the voltage base-to-emitter v_{BE}.

Thus, as $v_I(t)$ changes, so does v_{BE}, resulting in a **new** BJT relationship (curve) between i_C and v_{CE}.

i_C changes as the input changes

Graphically, we can represent this as:



where V_{I1}, V_{I2}, V_{I3} are three different **input** voltages such that $V_{I1} < V_{I2} < V_{I3}$.

Thus, as the **input** voltage $v_I(t)$ changes with time, the BJT i_C versus v_{CE} **curve** will change, and its **intersection** with the amplifier load line will change—i_C and v_{CE} will likewise be a function of **time**!

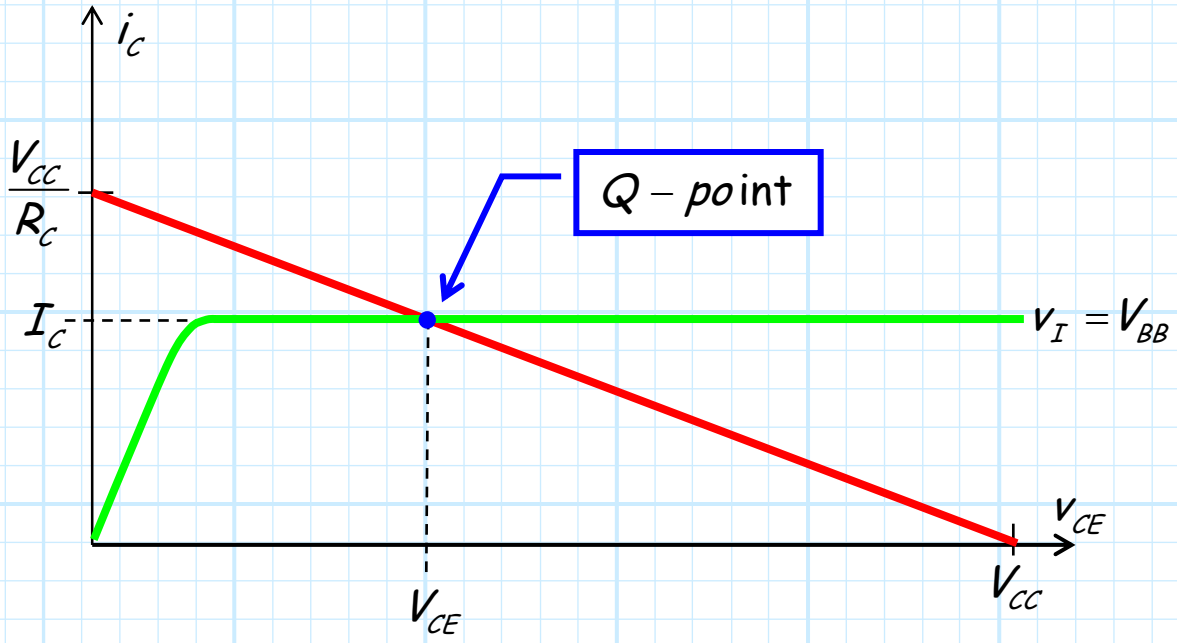
The operating point

Say that the **small-signal** input voltage is **zero** ($v_o(t) = 0$).

In this case, the input voltage is simply a **constant** bias voltage ($v_I(t) = V_{BB}$).

The collector current and voltage collector-to-emitter are likewise **DC bias** values (I_C and V_{CE}).

The intersection of the two curves in this case define the **operating point** (bias point, Q point) of the amplifier.

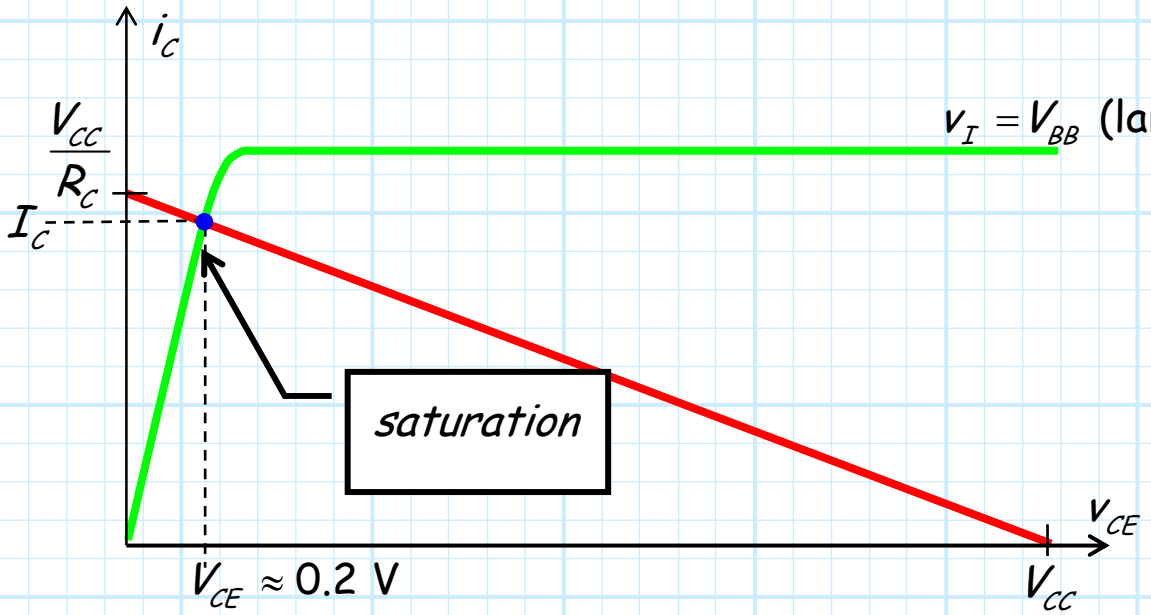


What happens if you make I_B too large

Q: *I see! We know that a **large** DC collector current results in a **large** transconductance g_m—a result that is typically required for **large voltage gain**. It appears that we should make V_{BB} (and thus I_C) as large as possible, **right?***

A: **NO!** There is a **big problem** with making the bias voltage V_{BB} too large—BJT **saturation** will result !

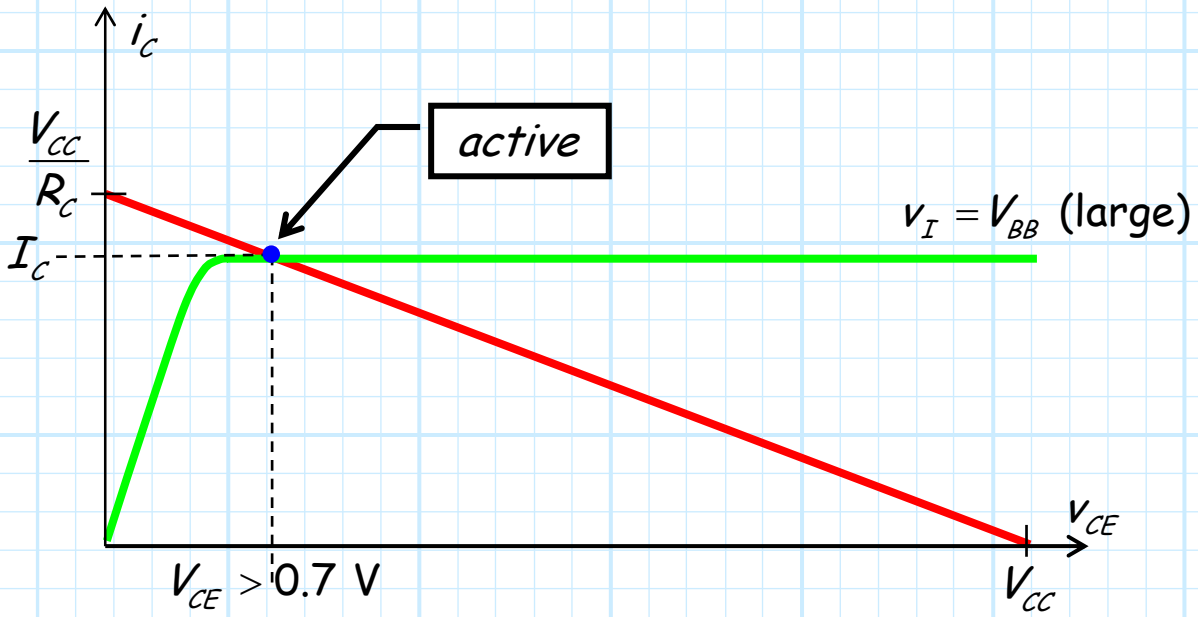
We can **graphically** show this unfortunate occurrence:



There's still a problem

A BJT in **saturation** makes a **poor** amplifier!

Q: *Oh I see! We need to set bias voltage V_{BB} to be large, but **not** so large that we push the BJT into saturation, right?*



A: **NO!!** There is a **big problem** with this strategy as well!

Remember, it is the **total** input voltage that will determine the BJT curve. If we DC bias the amplifier so that it is **nearly** in saturation, then even a small voltage v_i can "push" the BJT into saturation mode.

A little more than bias; then a little less than bias

For **example**, recall that the small signal input $v_i(t)$ is an **AC** signal. In other words its time averaged (i.e., DC) value is **zero**, meaning that the value of $v_i(t)$ will effectively be **negative** half of the time and positive the other half.

Say then that the **magnitude** of the small signal input is limited to a value Δv_i:

$$\left|v_i(t)\right| \le \Delta v_i$$

So that:

$$-\Delta v_i \le v_i(t) \le \Delta v_i \quad \text{for all time } t$$

and thus:

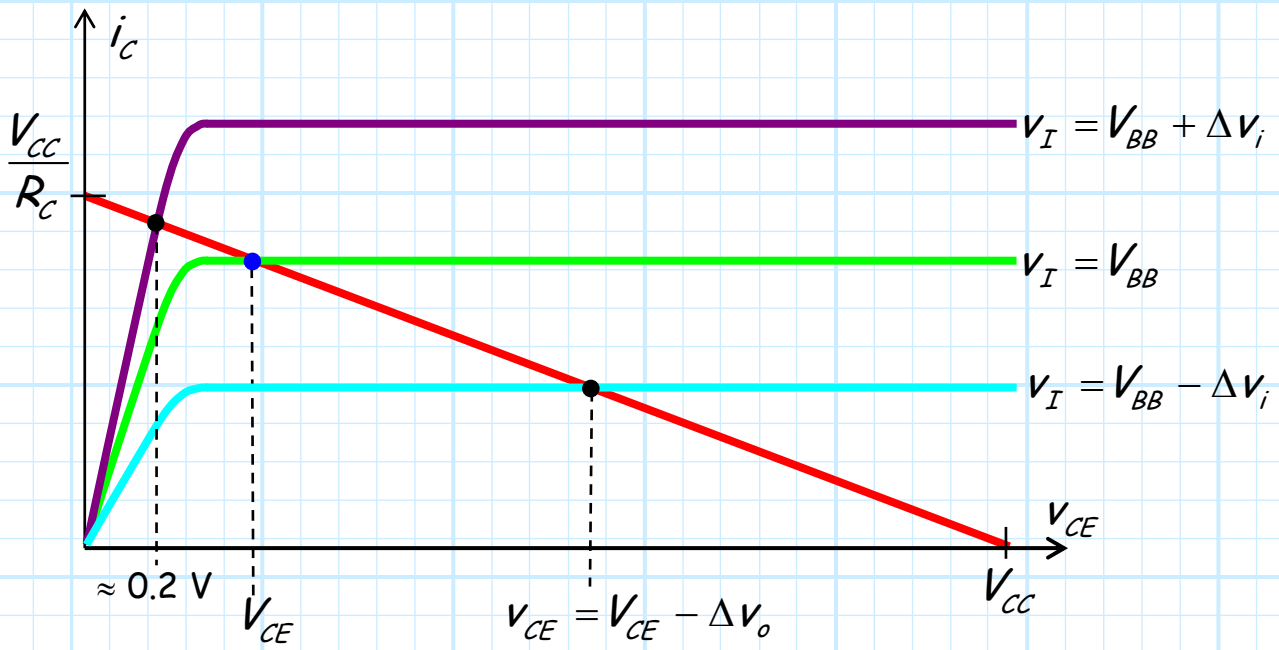
$$V_{BB} - \Delta v_i \le v_I(t) \le V_{BB} + \Delta v_i \quad \text{for all time } t$$

Let's now look at **three** scenarios for the small-signal input voltage v_i:

1) $v_i = -\Delta v_i$ 2) $v_i = 0$ 3) $v_i = +\Delta v_i$

We're hitting the floor

The resulting **output voltage** will of course be different for each case:



Look what happened here!

If the input small-signal is "large" and **positive**, the **total** input voltage (and thus total v_{BE}) will be **too large**, and thus push the BJT into **saturation**.

Distortion!!!!!!!!

The **output** voltage in this case (when $v_I = V_{BB} + \Delta v_i$) will simply be equal to:

$$v_O(t) \approx 0.2 \quad \text{(BJT saturated)}$$

as opposed to the **ideal** value:

$$v_O(t) = V_{CE} + \Delta v_o \quad \text{(BJT active)}$$

where $\Delta v_o = A_{vo}\,\Delta v_i$. Note for this amplifier, the small-signal voltage gain A_{vo} is **negative**, so that the value Δv_o is **also** negative:

$$\Delta v_o = A_{vo}\,\Delta v_i < 0$$

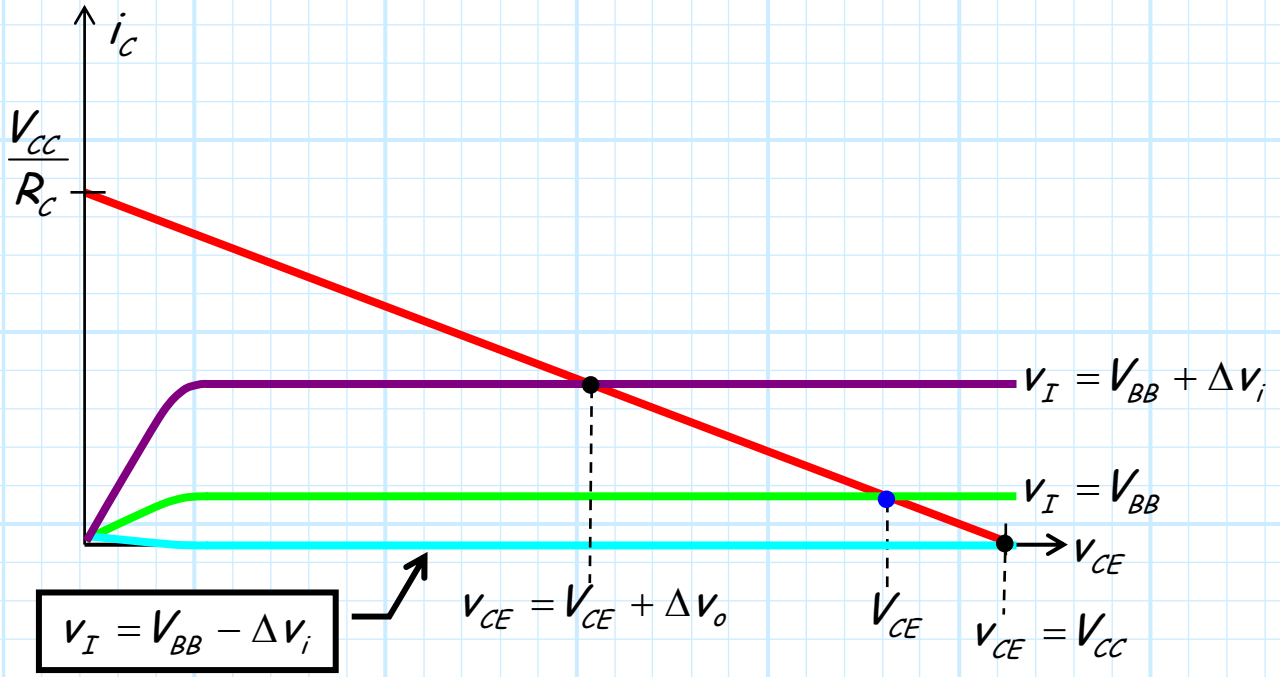
Since the BJT is in saturation during some portion of $v_i(t)$, the amplifier output signal will **not** look like the input signal—**distortion** will result!

I never said this was easy

Q: *Now I get it! We need to make V_{BB} **small**, so that the BJT does **not** enter saturation, and the output signal is **not** distorted!*

A: **NO!!** There is a **problem** with this too!

We can again **graphically** examine what happens if we make the bias voltage V_{BB} too **small**.



Look what happened here!

Now we're hitting the ceiling

If the **input** small-signal is "large" and **negative**, the **total** input voltage (and thus total v_{BE}) will be too **small**, and thus push the BJT into **cutoff**.

Note the collector current will be **zero** ($i_C = 0$) when the BJT is in cutoff!

The **output** voltage in this case (i.e., when $v_I = V_{CE} - \Delta v_i$) will simply be equal to:

$$v_O(t) = V_{CC} \quad \text{(BJT cutoff)}$$

as opposed to the **ideal** value:

$$v_O(t) = V_{CE} - \Delta v_o \quad \text{(BJT active)}$$

where $\Delta v_o = A_{vo}\,\Delta v_i$. Note for this amplifier, the small-signal voltage gain is **negative**, so that the value $-\Delta v_o$ is **positive**.

Since the BJT is in **cutoff** during some portion of $v_i(t)$, the amplifier output signal will **not** look like the input signal—**distortion** will result!

What do we do?

Q: *Yikes! Is there **nothing** we can do to avoid signal distortion?*

A: To get allow for the **largest** possible (distortion-free) output signal $v_o(t)$, we typically need to bias our BJT such that we are about **"half way"** between biasing the BJT in **saturation** and biasing the BJT in **cutoff**.

Note if the BJT is in **saturation**:

$$i_C \approx \frac{V_{CC}}{R_C}$$

(BJT saturation)

$$v_{CE} \approx 0.2\ \text{V}$$

Bias in the middle

Whereas, if it is in **cutoff**:

$$i_C = 0$$

(BJT cutoff)

$$v_{CE} = V_{CC}$$

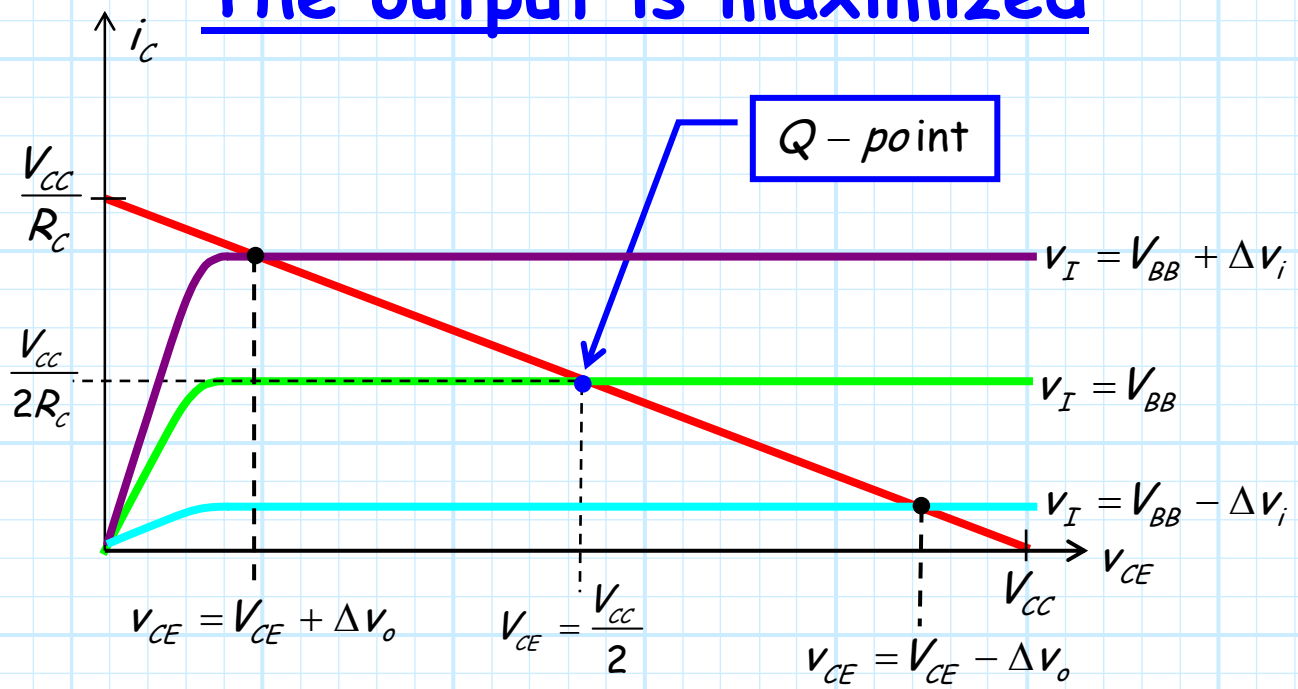
It is evident that for this particular amplifier, biasing **"half-way"** between saturation and cutoff means biasing such that:

$$V_{CE} \approx \frac{V_{CC}}{2}$$

or equivalently:

$$I_C \approx \frac{V_{CC}}{2R_C}$$

The output is maximized



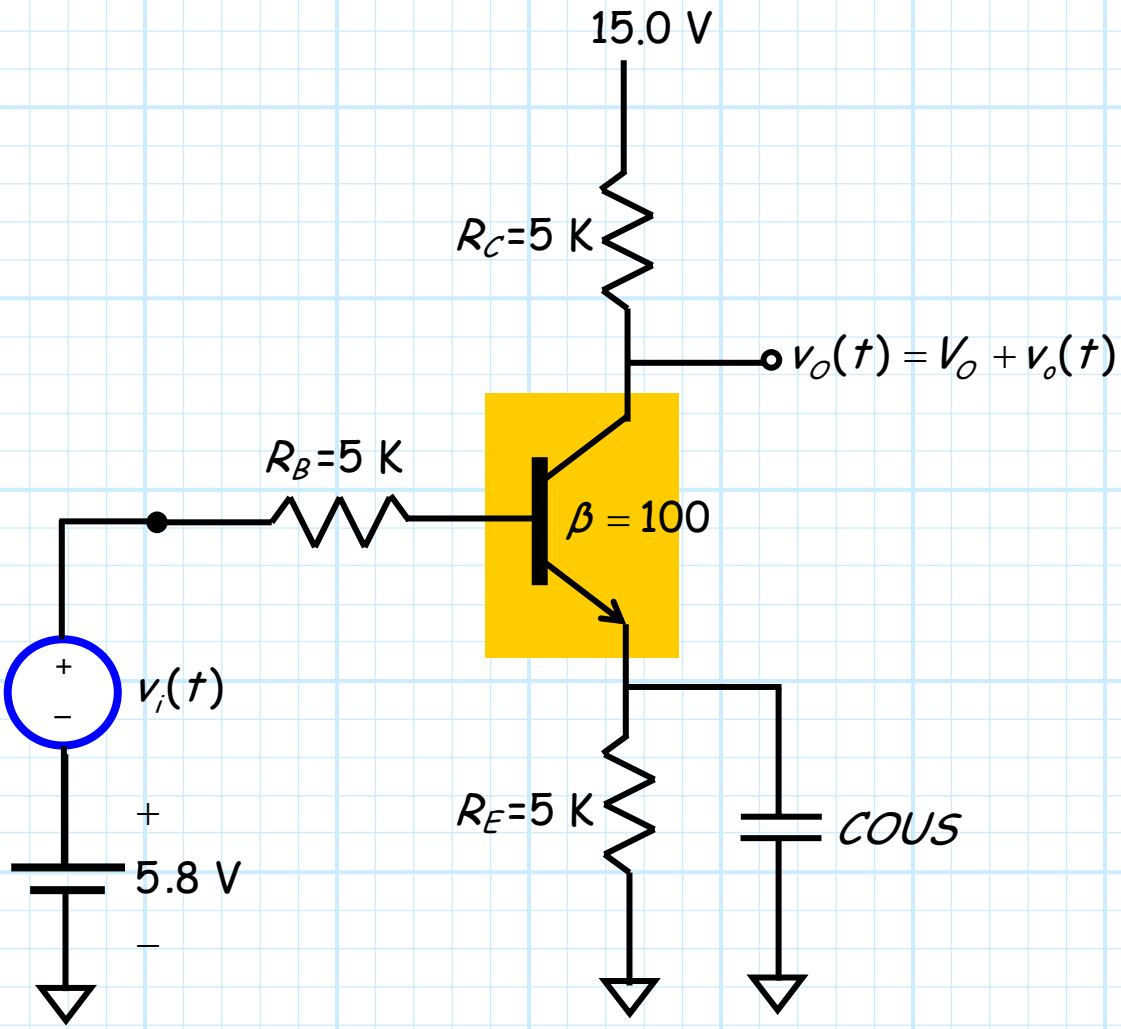
The bias solution above is optimal for **this** particular amplifier design. **Other** amplifier designs will result in **other** optimal bias designs—it is up to **you** determine what they are.

Remember, the **total** voltage $v_{CE}(t)$ must be larger than 0.7 V for all time; otherwise **saturation** (and thus signal distortion will result).

Likewise, the **total** collector current $i_C(t)$ must be greater than zero for all time; other wise **cutoff** (and thus signal distortion) will result.

Example: Amplifier Distortion

Recall this circuit from a previous handout:



We found that the small-signal **voltage gain** is:

$$A_{vo} = \frac{v_o(t)}{v_i(t)} = -66.7$$

Say the **input** voltage to this amplifier is:

$$v_i(t) = V_s \cos\omega t$$

Q: *What is the **largest** value that V_s can take without producing a **distorted** output?*

A: Well, we know that the **small-signal output** is:

$$\begin{aligned} v_o(t) &= A_{vo}\, v_i(t) \\ &= -66.7 V_s \cos\omega t \end{aligned}$$

BUT, this is **not** the output voltage!

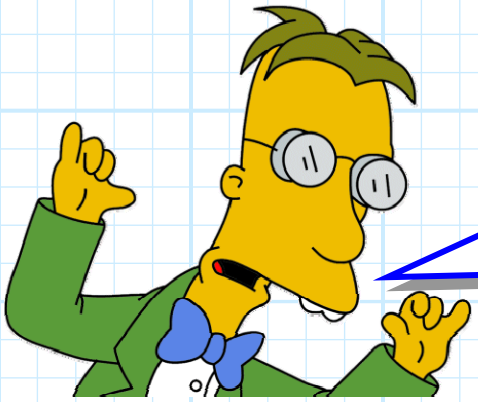
The **total** output voltage is the **sum** of the **small-signal** output voltage and the **DC** output voltage!

Note for this example, the **DC output** voltage is the **DC collector** voltage, and we recall we determined in an earlier handout that its value is:

$$V_O = V_C = 10 \text{ V}$$

Thus, the **total output voltage** is :

$$\begin{aligned} v_O(t) &= V_O + v_o(t) \\ &= 10.0 - 66.7\, V_s \cos\omega t \end{aligned}$$



*It is very important that you realize there is a **limit** on both how high and how low the **total** output voltage $v_o(t)$ can go!*

*That's right! If the **total** output voltage $v_o(t)$ tries to exceed these limits—even for a moment—the BJT will leave the **active** mode.*

*And leaving the active mode results in **signal distortion**!*

Let's break the problem down into **two** separate problems:

1) If **total** output voltage $v_O(t)$ becomes too **small**, the BJT will enter saturation.

2) If **total** output voltage $v_O(t)$ becomes too **large**, the BJT will enter cutoff.

We'll first consider **problem 1**.

For the BJT to remain in active mode, $v_{CE}(t)$ must remain **greater than 0.7** V for all time t (or equivalently $v_{CB}(t) > 0.0$).

From an earlier handout, we know that $V_E = 5.05$ V. The large **capacitor** on the emitter keeps this voltage **constant** with respect to time.

Therefore, the voltage $v_{CE}(t)$ will remain greater than 0.7 V **only** if the collector voltage $v_C(t)$ remains **greater** than $5.05 + 0.7 = 5.75$ V. Note 5.75 is the **base voltage** V_B.

Of course, the collector voltage is also the output voltage ($v_O(t) = v_C(t)$), so that we can conclude that the **output** voltage must remain **larger** than V_B=5.75 V to remain in **active** mode:

$$5.75 < v_O(t) = 10 - 66.7V_s \cos\omega t$$

In other words, the **lower** limit on the **total** output voltage is:

$$L_- = 5.75\,V$$

Note that we can solve this equation to determine the **maximum** value of small-signal **input** magnitude V_s:

$$\begin{aligned} 5.75 &< 10 - 66.7V_s \cos\omega t \\ 66.7V_s \cos\omega t &< 4.25 \\ V_s \cos\omega t &< 0.064 \end{aligned}$$

Since $\cos\omega t$ can be as large as 1.0, we find that the magnitude of the **input** voltage can be **no larger** than 64 mV, i.e.,

$$V_s < 0.064 \text{ V}$$

If the **input** magnitude exceeds this value, the BJT will (momentarily) leave the active region and enter the **saturation** mode!

Now let's consider **problem 2**

For the BJT to remain in **active** mode, the **collector** current must be **greater** than zero (i.e., $i_C > 0$). Otherwise, the BJT will enter **cutoff** mode.

Applying **Ohm's Law** to the collector resistor, we find the **collector current** is:

$$i_C = \frac{V_{CC} - v_O}{R_C} = \frac{15 - v_O}{5}$$

it is evident that collector current is **positive** only if $v_O < 15$ V.

In other words, the **upper** limit on the **total** output voltage is:

$$L_+ = 15.0\,V$$

Since:

$$v_O(t) = 10 - 66.7 V_s \cos\omega t$$

we can conclude that in order for the BJT to remain in **active** mode:

$$10 - 66.7 V_s \cos\omega t > 15.0$$

Therefore, we find:

$$V_s \cos\omega t > \frac{-5.0}{66.7} = -0.0075$$

Since $\cos\omega t \geq -1$, the above equation means that the **input** signal magnitude V_s can be **no larger** than:

$$V_s < 75 \text{ mV}$$

If the input magnitude **exceeds** 75 mV, the BJT will (momentarily) leave the active region and enter the **cutoff** region!

In **summary**:

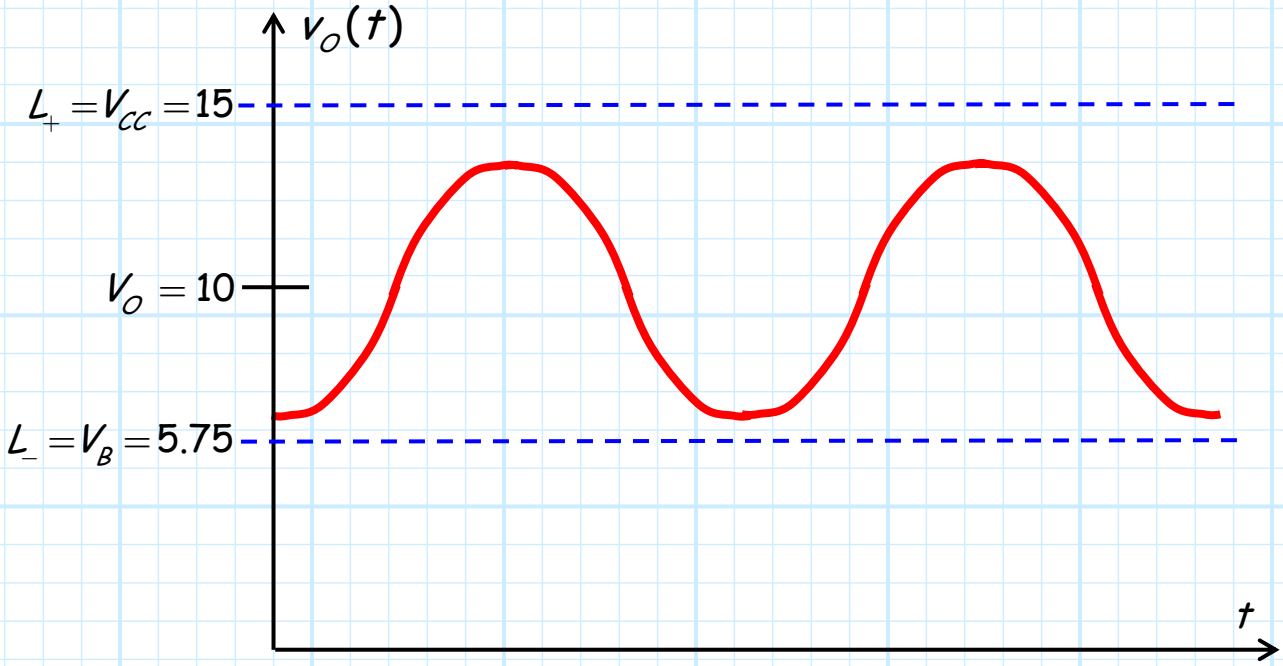
1) If $V_s > 64$ mV, the BJT will at times enter **saturation**, and **distortion** will occur!

2) If $V_s > 75$ mV, the BJT will at times enter **cutoff**, and **even more** distortion will occur!

To demonstrate this, let's consider **three** examples:

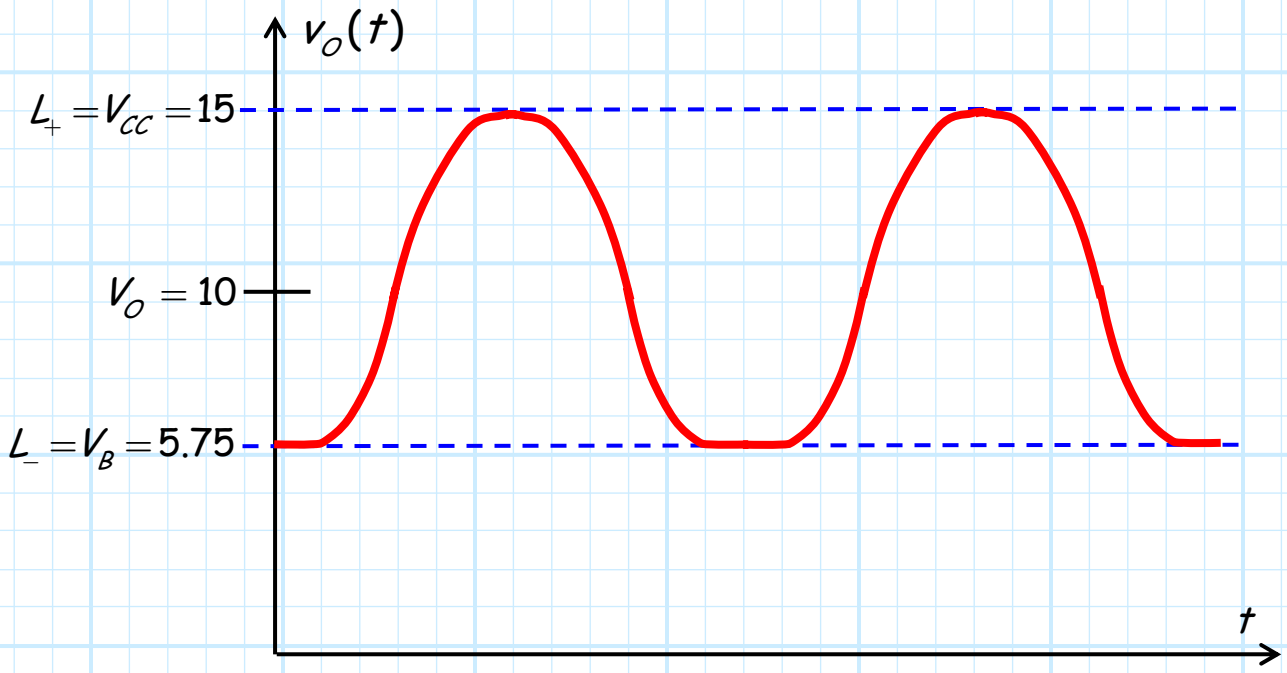
1. $V_s < 64$ mV

The output signal in this case remains between V_{CC}=15.0 V and V_B=5.75 V for **all** time t. Therefore, the output signal is **not distorted**.



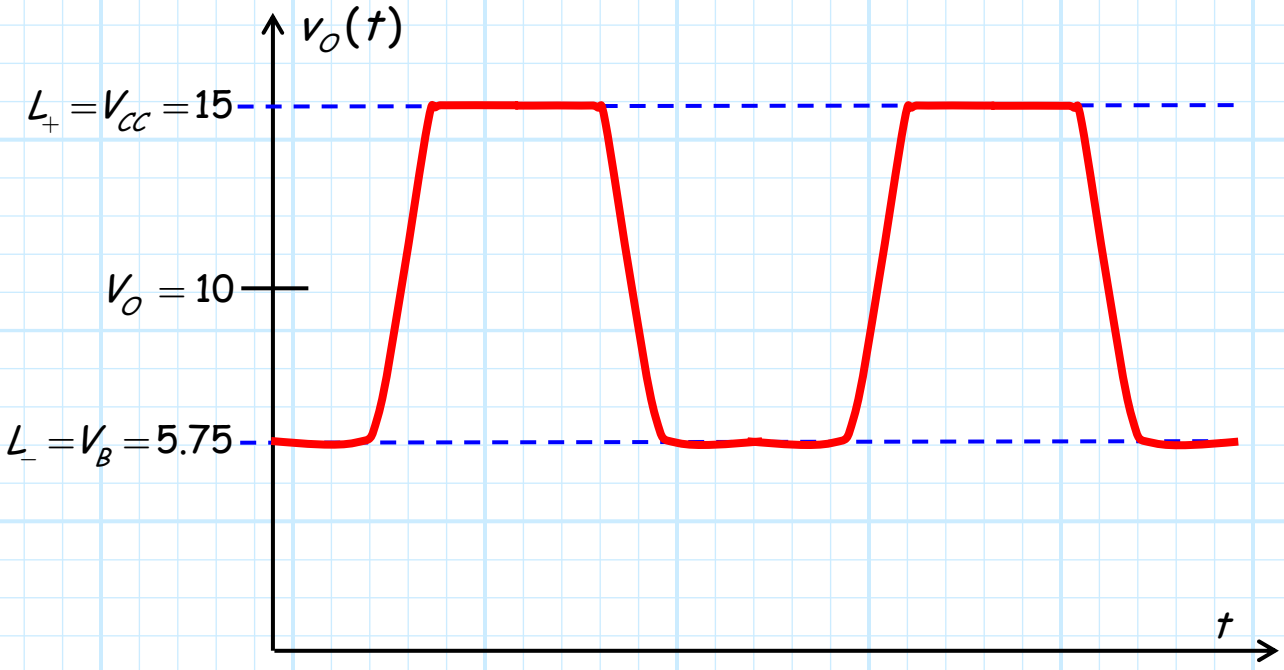
2. $64 \text{ mV} < V_s < 75 \text{ mV}$

The output signal in this case remains less than V_{CC}=15.0 V for all time t. However, the small-signal output is now large enough so that the total output voltage at times tries to drop **below** $V_B = 5.75\,\text{V}$ (i.e., V_{CE} drops below 0.7 V). For these times, the BJT will enter **saturation**, and the output signal will be **distorted**.



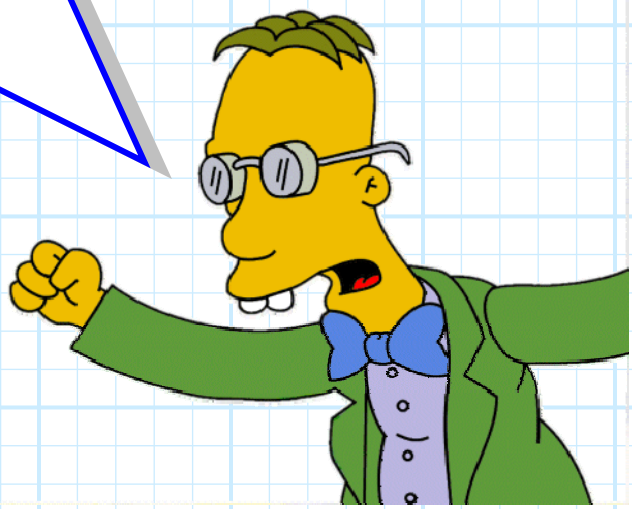
3. $V_s > 75$ mV

In this case, the small-signal input signal is sufficiently **large** so that the total output will attempt to exceed **both** limits (i.e., $V_{CC} = 15.0\,\text{V}$ and $V_B = 5.75$ V). Therefore, there are periods of time when the BJT will be in **cutoff**, and periods when the BJT will be in **saturation**.



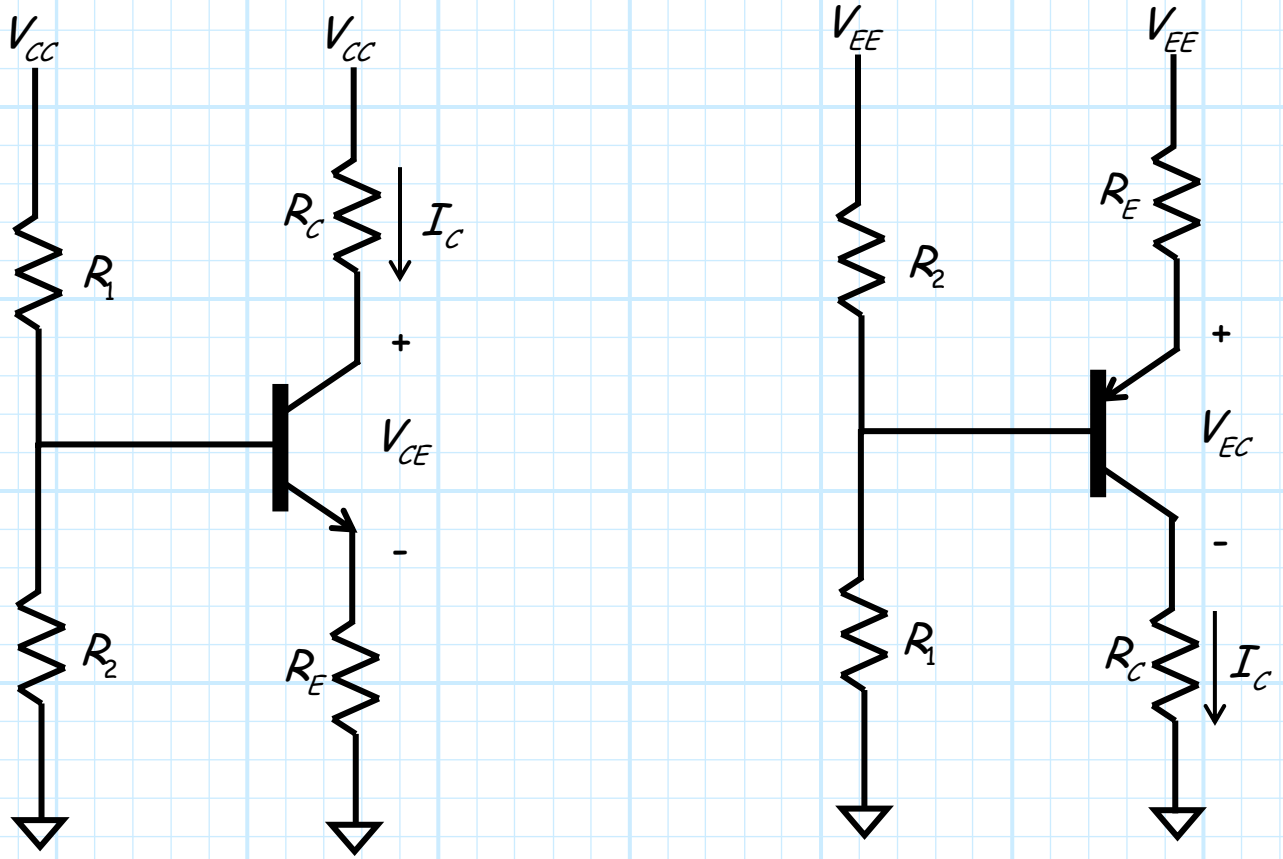
*For a given amplifier voltage gain, you must determine the **largest possible** input $v_i(t)$ that will produce a **distortion-free** output signal.*

*To do this, you must determine the **limits** of the **total** output voltage. There will be **two** limits—one for **saturation** (L_-) and one for **cutoff** (L_+).*



D.C Biasing using a Single Power Supply

The general form of a **single**-supply BJT amplifier biasing circuit is:



Just three goals

Generally, we have **three goals** in designing a biasing network:

1) Maximize Gain

Typically, we seek to set the operating point of the BJT amplifier such that the resulting small signal voltage gain is **maximized**.

However, we sometimes seek to set the bias point such that the **output resistance** is minimized, or the **input resistance** is maximized.

2) Maximize Voltage Swing

We seek to set the operating point of the BJT amplifier such that the maximum small signal output can a **large** as possible.

If we make V_{CE} too small, then the BJT will easily **saturate**, whereas if V_{CE} is too large, the BJT will easily **cutoff**.

This suddenly seems like a lot of goals

3) Minimize Sensitivity to changes in β

Manufacturing and temperature variances will result in significant changes in the value β.

We seek to design the bias network such that the amplifier parameters will be **insensitive** to these changes.

Q: *You're kidding me right?*

*We're supposed to achieve **all** these goals with just **four** resistors?*

A: Actually, the three design goals listed above are often in **conflict**.

We typically have to settle for a **compromise** DC bias design.

How we maximize gain

Let's take a closer look at each of the **three** design goals:

1) Maximize Gain

Typically, the small-signal **voltage gain** of a BJT amplifier will be proportional to transconductance g_m:

$$A_{vo} \propto g_m$$

Thus, to maximize the amplifier voltage gain, we must **maximize** the BJT transconductance.

Q: *What does this have to do with **D.C. biasing?***

A: Recall that the transconductance depends on the DC **collector current** I_C:

$$g_m = \frac{I_C}{V_T}$$

Maximize that darn bias current!

Therefore the amplifier voltage gain is typically **proportional** to the DC collector current:

$$A_{vo} \propto \frac{I_C}{V_T}$$

We of course can't decrease the thermal voltage V_T, but we can design the bias circuit such that I_C is **maximized**.

To maximize A_{vo}, maximize I_C

We don't want distortion!

2) Maximize Voltage Swing

Recall that if the DC collector voltage V_C is biased too close to V_{CC}, then even a small small-signal collector voltage $v_c(t)$ can result in a **total** collector voltage that is too **large**, i.e.:

$$v_C(t) = V_C + v_c(t) \geq V_{CC}$$

In other words, the BJT enters **cutoff**, and the result is a **distorted** signal!

To avoid this (to allow $v_c(t)$ to be as large as possible without BJT entering cutoff), we need to bias our BJT such that the DC collector voltage V_C is as **small** as possible.

How to avoid cutoff

Note that the collector voltage is:

$$V_C = V_{CC} - R_C I_C$$

Therefore V_C is minimized by designing the bias circuit such that the DC collector current I_C is as **large** as possible.

Q: *Hey hey! It looks like amplifier bias design is going to be **easy**. We can **both** maximize transconductance g_m **and** minimize the DC collector voltage V_C by maximizing the DC collector current I_C!*

A: Just a second! We must **also** consider the signal distortion that occurs when the BJT enters **saturation**.

But also avoid saturation

Saturation of course is avoided if the total voltage collector to emitter remains greater than 0.7 V, i.e.:

$$v_{CE}(t) = V_{CE} + v_{ce}(t) > 0.7 \text{ V}$$

Thus, to avoid BJT saturation—and the resulting signal distortion—we need to bias our BJT such that the DC voltage V_{CE} is as **large** as possible.

To minimize signal distortion, maximize V_{CE}

BJTs are pretty sensitive

3) Minimize Sensitivity to changes in β

We find that BJTs are very **sensitive** to temperature—specifically, the value of β is a function of temperature.

Likewise, the value of β is not particularly constant with regard to the manufacturing process.

We find that 100 otherwise "identical" BJTs will result have 100 **different** values of β!

Both of these facts lead to the requirement that our bias design be **insensitive** to the value of β.

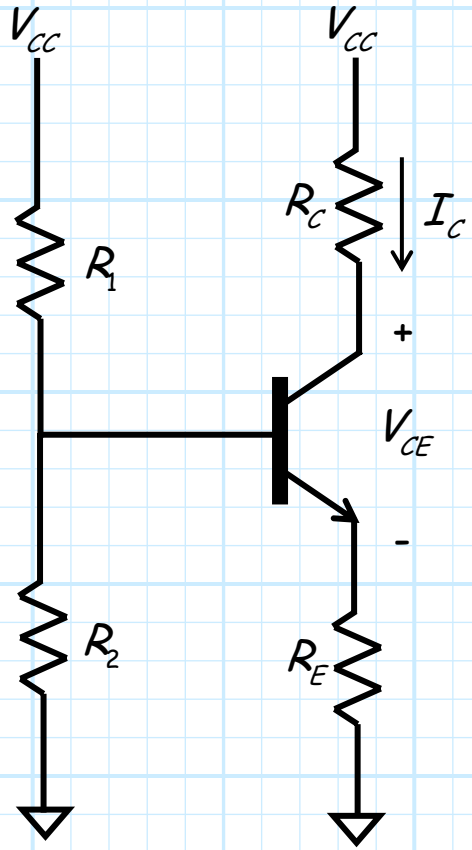
Specifically, we want to design the bias network such that the DC bias currents (e.g., I_C) do **not** change values when β does.

Mathematically, we can express this requirement as minimizing the value:

$$\frac{d\,I_C}{d\,\beta}$$

How do we determine this derivative?

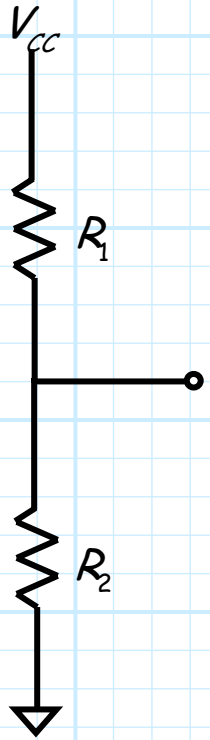
Let's determine this derivative value for our **standard** bias network:



Q: *Yuck! This looks like a disturbingly difficult circuit to analyze.*

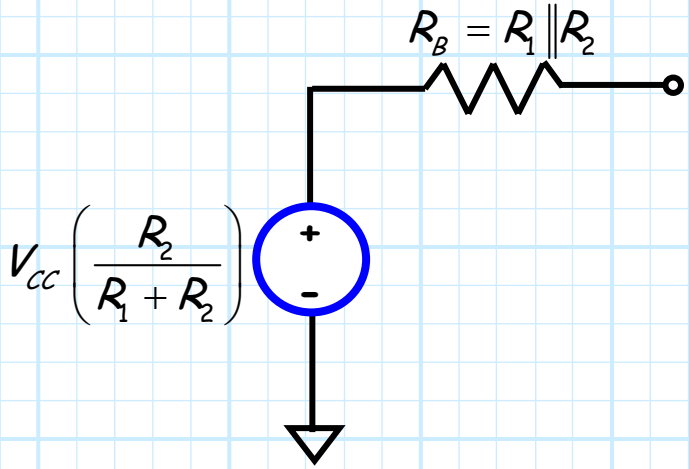
A: One way to **simplify** the analysis it to use a **Thevenin's** equivalent circuit.

Specifically, replace this portion of the bias circuit with its **Thevenin's equivalent**:

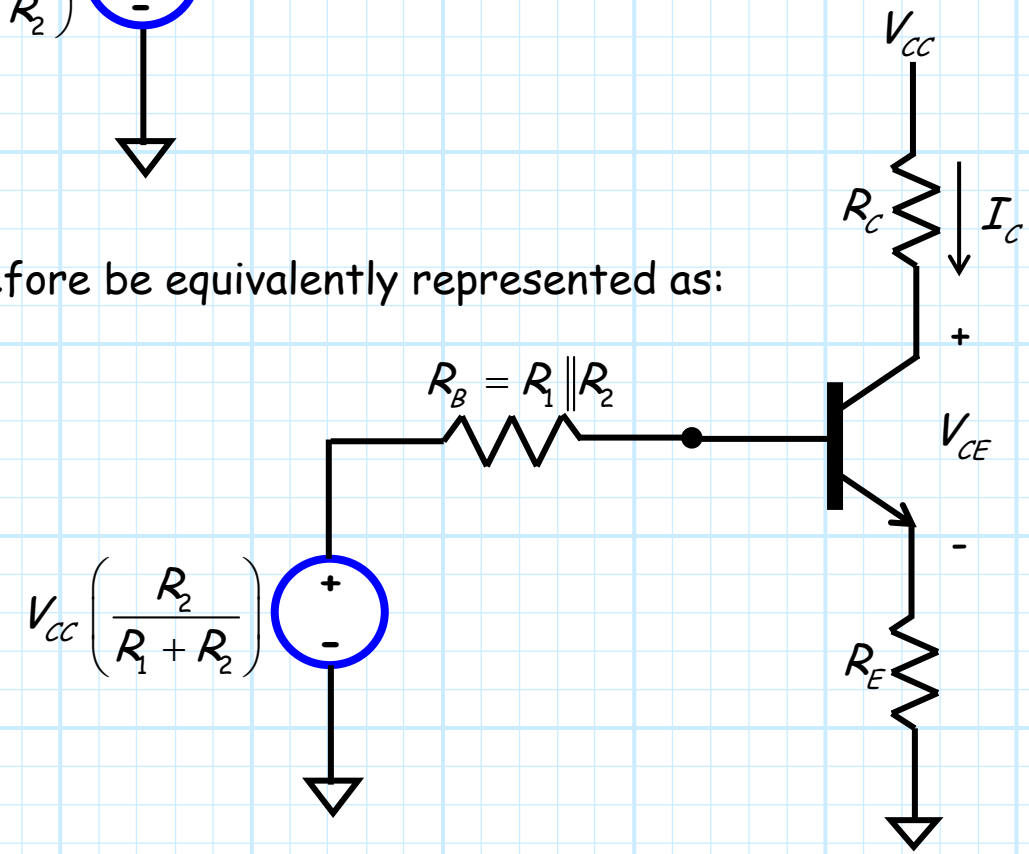


Good ol' Thevenin's!

We find that this **equivalent** circuit is:



The **bias network** can therefore be equivalently represented as:



You're always having fun if you're doing calculus

If we **ASSUME** that the BJT is in active mode, then we **ENFORCE** the proper equalities and **ANALYZE** this circuit to find collector current I_C:

$$I_C = \frac{\beta\left(V_{BB} - 0.7\right)}{\left(\beta + 1\right)R_E + R_B}$$

We find therefore that:

$$\frac{d\,I_C}{d\,\beta} = \frac{-\left(V_{BB} - 0.7\right)}{\left(\beta\dfrac{R_E}{R_B} + 1\right)^2}$$

Note then that:

$$\lim_{R_E/R_B \to \infty} \frac{d\,I_C}{d\,\beta} = 0$$

Maximize that darn resistor!

In other words, if we wish to make the DC collector current **insensitive** to changes in β, we need to make:

$$R_E \gg R_B$$

We of course could accomplish this by making the **base resistance** $R_B = R_1 \| R_2$ small, but we will find out later that there are problems with doing this.

Instead, we can minimize the circuit sensitivity to changes in β by maximizing the **emitter resistor** R_E.

To minimize $d I_C / d \beta$, maximize R_E

This seems so simple…

So, let's **recap** what we have learned about designing our bias network:

1. Make I_C as large as possible.
2. Make V_{CE} as large as possible.
3. Make R_E as large as possible.

Q: *Seems easy enough! Let's get started biasing BJT amplifiers!*

A: Not so fast! We still have a **serious problem**.

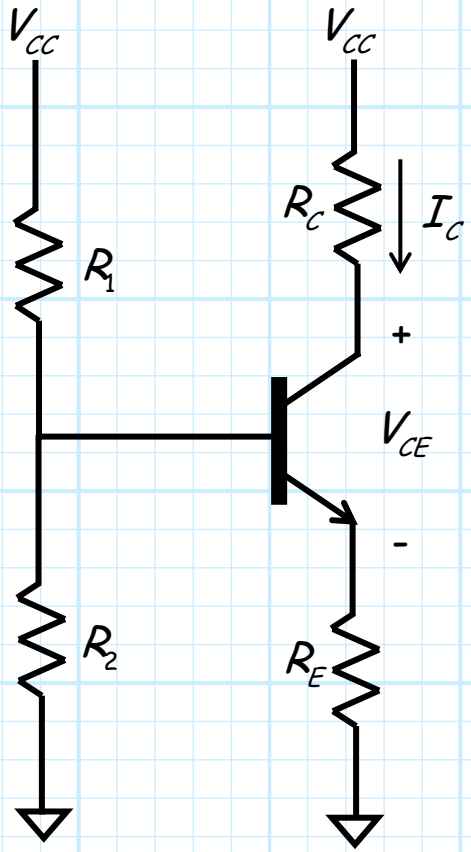
...NOT!

To see what this problem is, write the **KVL** equation for the **Collector-Emitter Leg** of the Bias Network:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

or

$$I_C R_C + V_{CE} + I_E R_E = V_{CC}$$



Maximize A_{vo} by **maximizing** this term.

Minimize distortion by **maximizing** this term.

Minimize β sensitivity by **maximizing** this term.

But the **total** of the three terms must equal this!

A logical compromise

Q: ***Yikes!*** *It's like owing* ***3*** *really big guys $15* ***each****, but having only $15 in your pocket.*

What do we do?

A: **Split** the total voltage **3 ways** (give each guy $5).

$$I_C R_C = \frac{V_{CC}}{3}$$

$$V_{CE} = \frac{V_{CC}}{3}$$

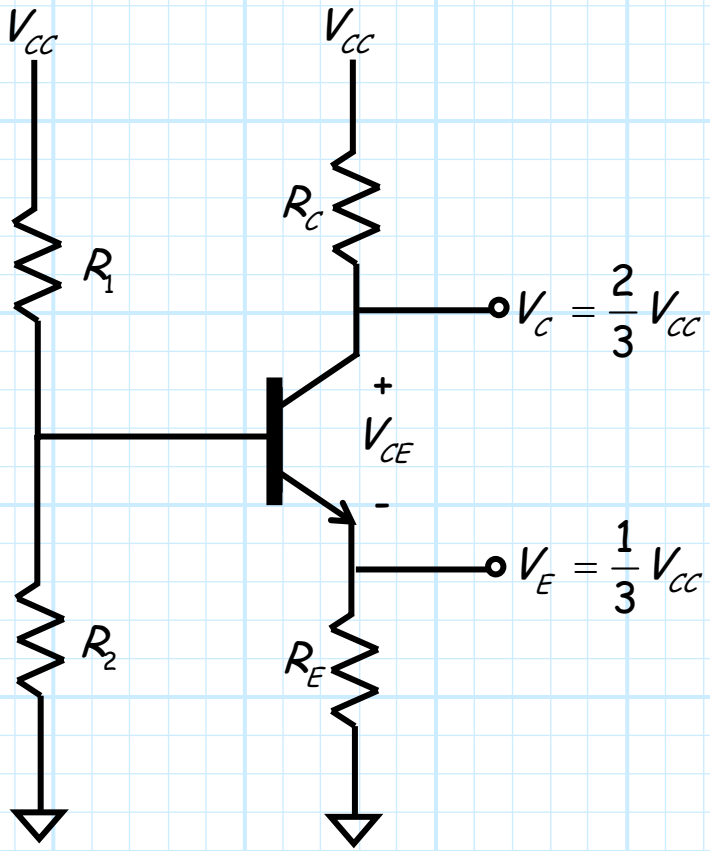
$$+ \qquad I_E R_E = \frac{V_{CC}}{3}$$

$$I_C R_C + V_{CE} + I_E R_E = V_{CC}$$

The result of this compromise

In other words, for an *npn* BJT, set:

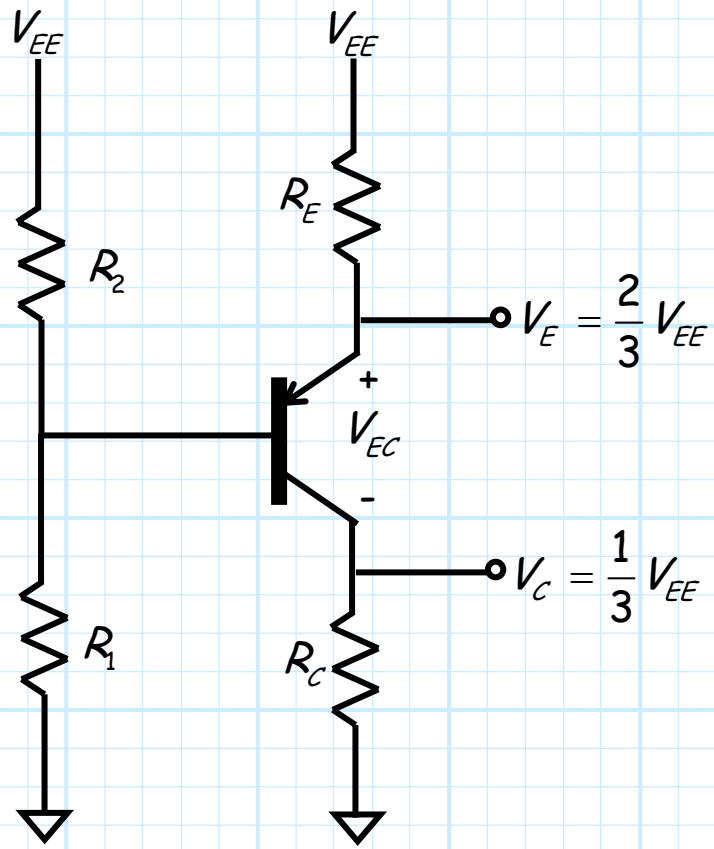
$$V_C = \frac{2}{3}V_{CC} \qquad \text{and} \qquad V_E = \frac{1}{3}V_{CC}$$



Don't forget *pnp*

Likewise, for a *pnp* BJT, set:

$$V_E = \frac{2}{3} V_{EE} \qquad \text{and} \qquad V_C = \frac{1}{3} V_{EE}$$



What should I_C be?

Q: *We have determined that the **product** $I_C R_C$ should be equal to $V_{CC}/3$.*

*We can of course accomplish this with a larger resistor R_C and a smaller current I_C, **or** a larger current I_C and a smaller resistor R_C. What **should** the value of I_C be?*

A: Generally speaking, the value of the **DC collector current** I_C affects:

1) Voltage Gain ($g_m \to \infty$ as $I_C \to \infty$).

2) Input Resistance ($r_\pi \to 0$ as $I_C \to \infty$).

3) BJT Output Resistance ($r_o \to 0$ as $I_C \to \infty$).

4) Power Consumption ($P \to \infty$ as $I_C \to \infty$).

5) Amplifier Bandwidth ($BW \to "\infty"$ as $I_C \to \infty$).

The "best" value of collector current I_C is a **trade** between these parameters.

There are two resistors left

Q: *OK, we now have enough information to set I_C, V_C, and V_E, and thus resistors R_C and R_E.*

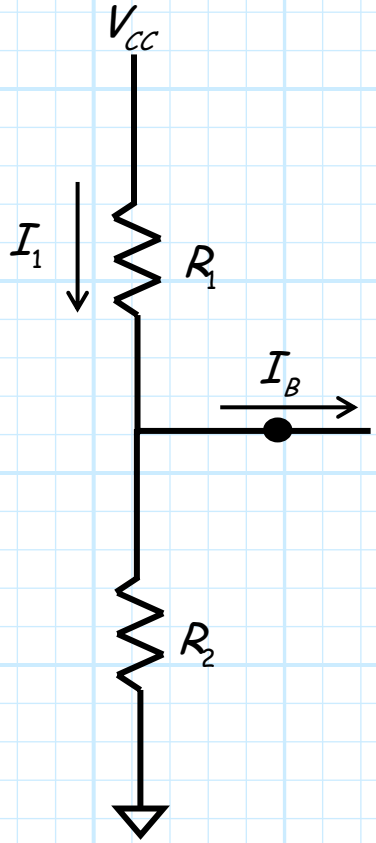
*But we still have **two** bias resistors left— R_1 and R_2. How do we determine their values?*

A: Well, we have found that **reducing** $R_B = R_1 \| R_2$ decreases the circuit sensitivity to β $\Rightarrow$ This is **good**!

But, we **will** find that **reducing** $R_B = R_1 \| R_2$ will often decrease the amplifier input resistance R_i $\Rightarrow$ This is **bad**!

Also, we find that reducing $R_B = R_1 \| R_2$ will increase the power dissipation $\Rightarrow$ This is also **bad**!

A "rule of thumb"



$$I_1 \approx \frac{V_{CC}}{R_1 + R_2} \qquad \text{if} \quad I_1 \gg I_B$$

$$\therefore \; P = V_{CC}\, I_1 \approx \frac{V_{CC}^2}{R_1 + R_2}$$

A general "**rule of thumb**" is to select the values of R_1 and R_2 so that I_C is:

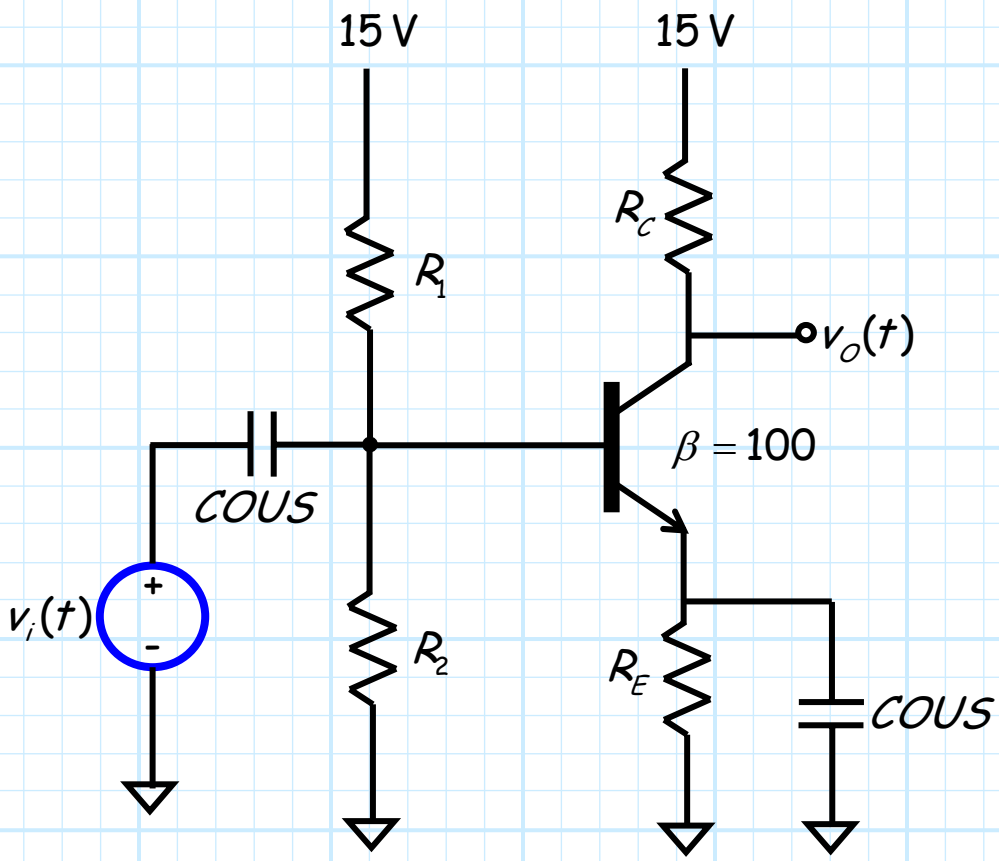
$$0.1\, I_C < I_1 < I_C$$

Remember, the resistors R_1 and R_2 also determine **the base voltage** V_B, which should approximately be:

$$V_B = V_{BE} + V_E$$
$$= 0.7 + \frac{V_{CC}}{3}$$

Example: Single-Supply DC Bias

Consider this small-signal amplifier:

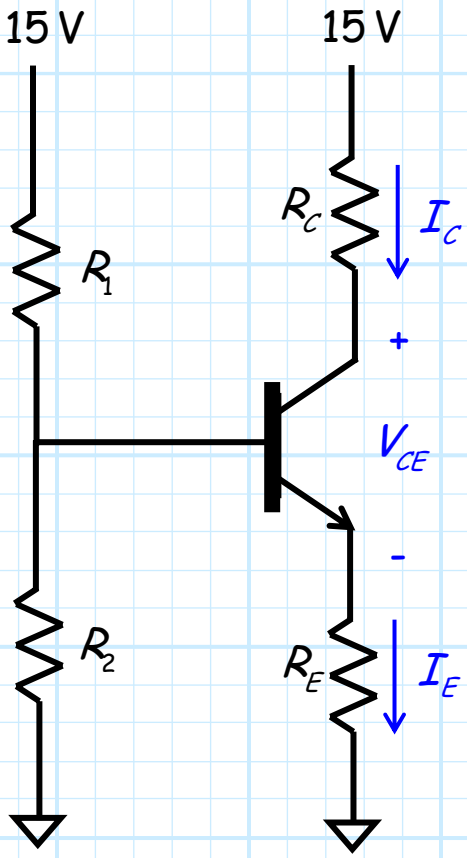


Say we decide that the **DC collector current** should be $I_C = 5\,\text{mA}$.

Let's find the **resistor** values for R_1, R_2, R_C and R_E that properly **bias** this amplifier!

Step 1: *Write the DC Circuit Schematic*

➡ After all, we are designing the **DC** bias!



Step 2: *Enforce the design goals for V_E and V_C*

Recall that our DC bias "rule-of -thumb" was to divide the V_{CC} voltage into "thirds" so that:

$$V_E = V_{CC}/3 = 5.0 \quad V$$

and

$$V_C = 2V_{CC}/3 = 10.0 \quad V$$

Since we want $I_C = 5\,mA$, we find that the **collector resistor** must be:

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{15 - 10}{5} = 1K$$

Likewise, the **emitter resistor** is:

$$R_E = \frac{V_E}{I_E} = \frac{\alpha}{I_C} V_E = \frac{5.0}{5.05} = 0.99K \cong 1K$$

Step 3: *Choose I_1 and find R_1 and R_2*

Recall our "**rule-of-thumb**" for the current I_1 is:

$$0.1\, I_C < I_1 < I_C$$

Let's pick a value in the middle, i.e.:

$$I_1 = 0.5\, I_C = 2.5\,mA$$

Since we know that that the **base voltage** is approximately:

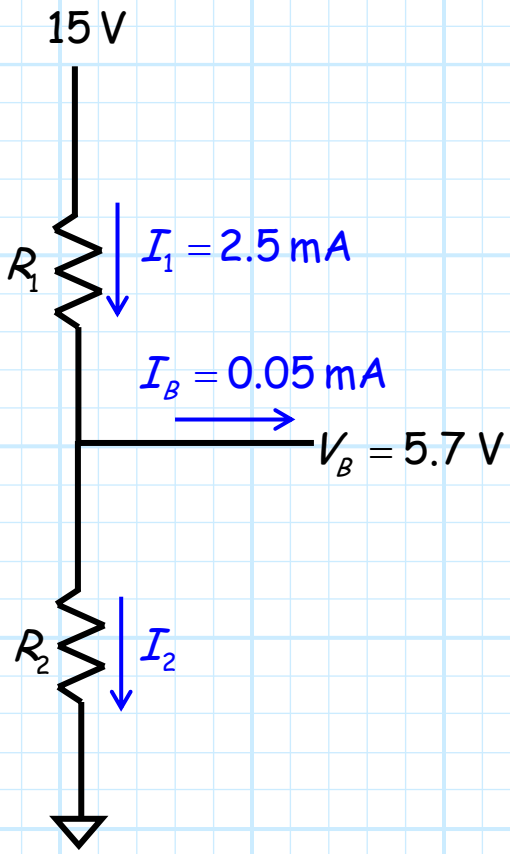
$$V_B \approx 0.7 + V_E = 5.7\ V$$

and we know that the **base current** is:

$$I_B = \frac{I_C}{\beta} = \frac{5.0}{100} = 0.05\ mA$$

we can thus determine resistor R_1:

$$R_1 = \frac{15.0 - V_B}{I_1}$$
$$= \frac{15.0 - 5.7}{2.5}$$
$$= 3.72\,\text{K}$$



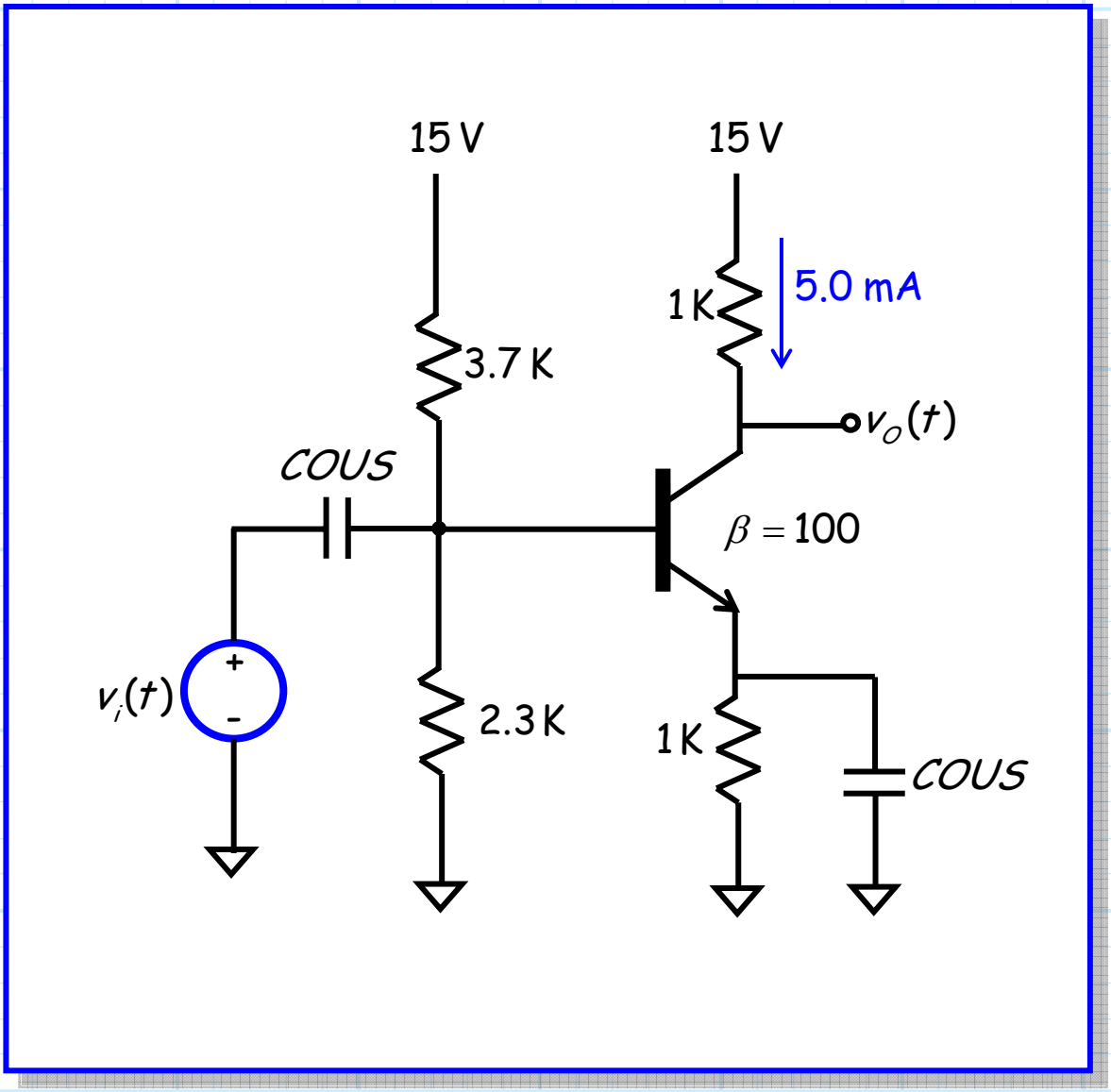
Likewise, since we know that the current I_2 is:

$$I_2 = I_1 - I_B$$
$$= 2.5 - 0.05$$
$$\approx 2.5\,\text{mA}$$

we can find the second resistor R_2:

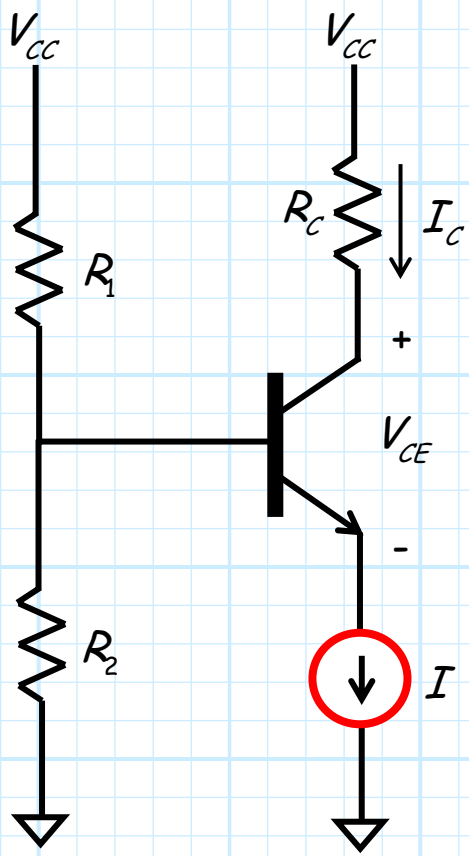
$$R_2 = \frac{V_B}{I_2} = \frac{5.7}{2.5} = 2.28\,\text{K}$$

Therefore, our completed **amplifier design** is:


15 V
15 V
1 K
5.0 mA
3.7 K
$v_O(t)$
COUS
$\beta = 100$
$v_i(t)$
+
-
2.3 K
1 K
COUS

BJT Biasing using a Current Source

Another way to bias a BJT small signal amplifier is to use one voltage source and one **current source**. This biasing scheme has a number of **important advantages**:



1. The DC emitter current is **independent** of β or BJT temperature!

Therefore, the DC collector current $I_C = \alpha I_E \approx I_E$ is nearly independent of these parameters as well.

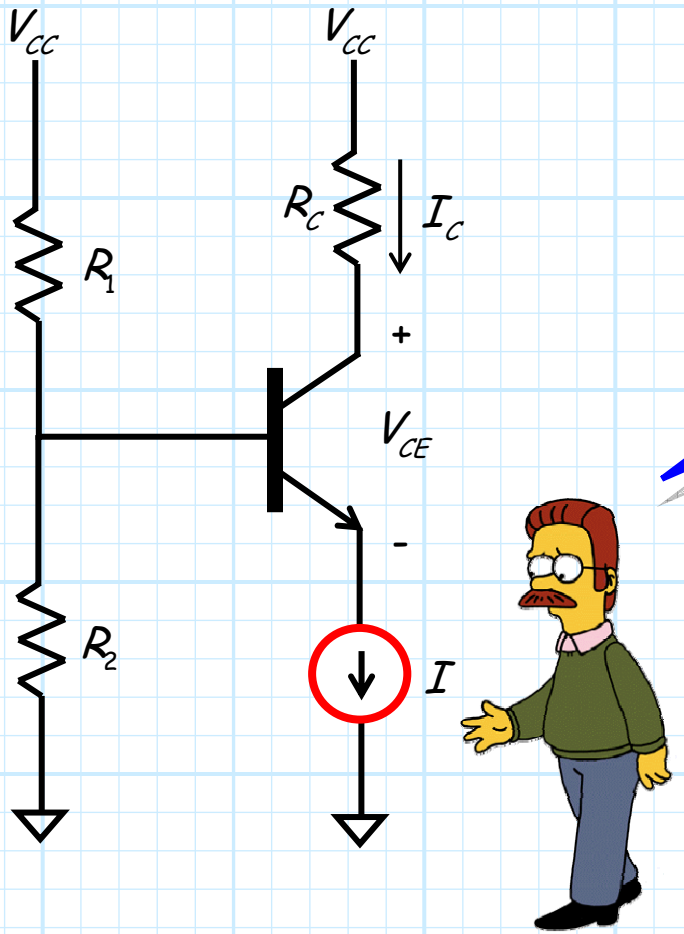
2. This means that the **emitter voltage** can be set at an arbitrarily low value!

Therefore, the output voltage swing can be much **larger** than an equivalent single-supply amplifier!

3. We can make resistors R_1 and R_2 **large** without making design sensitive to temperature and β.

The current source: not as easy as it appears

Note that **ideally**, we would set the emitter votage to **zero** ($V_E = 0$), and thus the collector voltage to $V_C = V_{CC}/2$ to **maximize** the output swing (i.e., maximize the largest possible **undistorted** output signal).



Q: *But, isn't it diddly darn difficult to actually build an **ideal** current source!?*

A: True! For reasons we shall study later, most current sources require a **minimum voltage** across them in order to operate properly.

Put collector voltage half way between floor and ceiling

Thus, our **bias rule** should be:

> *Make the DC emitter voltage V_E as **small** as possible (and still have the current source work!).*

Then set the **current source** to a value equal to the desired DC collector current (i.e., $I_C \approx I_E$):

$$I = I_E \approx I_C$$

To maximize the output voltage swing, we still want to place the DC collector voltage V_C **half way** between V_{CC} and V_E.

$$V_C = \frac{V_{CC} + V_E}{2}$$

The **collector resistor** therefore should be:

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{V_{CC} - V_C}{I} = \frac{V_{CC} - V_E}{2I}$$

R_1 and R_2: same as before

The remaining resistors R_1 and R_2 are determined in the **same** manner as with the single-supply bias design, i.e.:

$$R_1 = \frac{V_{CC} - V_B}{I_1}$$

and

$$R_2 = \frac{V_B}{I_2} \approx \frac{V_B}{I_1}$$

where the base voltage is approximately:

$$V_B = 0.7 + V_E$$

and the current I_1 is any value in the range:

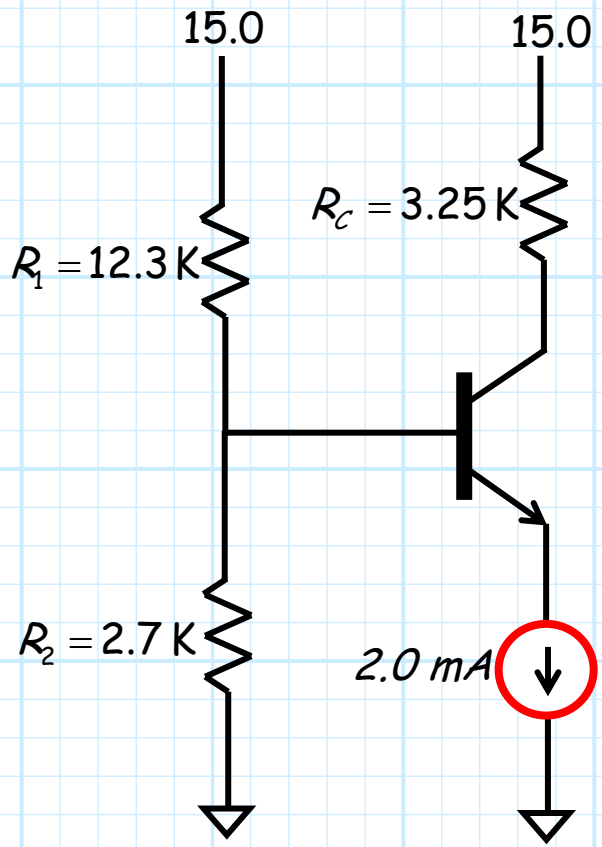
$$0.1 I_C < I_1 < I_C$$

Just the kind of subtle topic I might put on an exam

For **example**, say we wish to design a biasing network where:

$$I_C = 2\,mA \qquad V_E \geq 2.0V \qquad V_{CC} = 15.0\,V \qquad I_1 = 0.5\,I_C$$

The result would be:



*It is obvious to me that this bias design **satisfies** the parameters described above.*

*But, don't take my word for it—verify for **yourself** that these resistor values are correct.*

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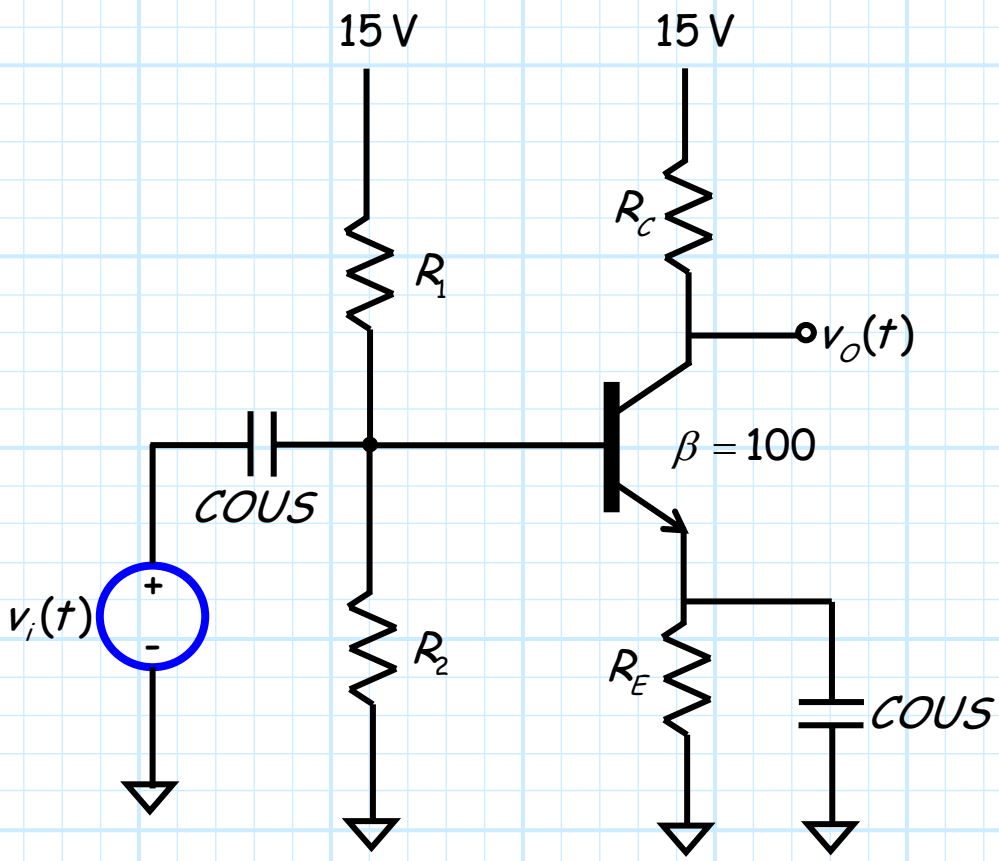

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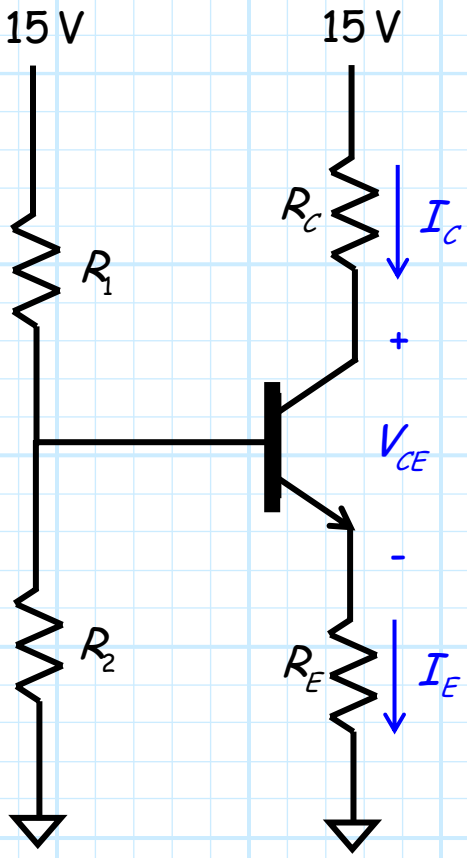

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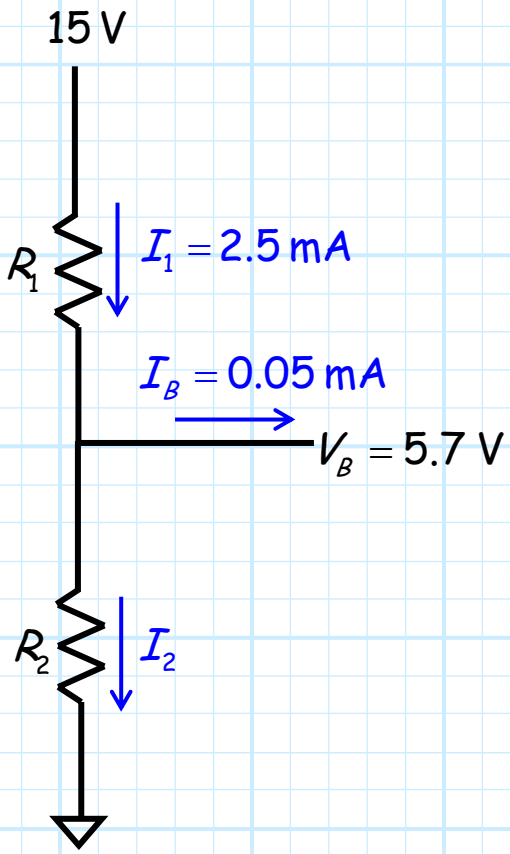

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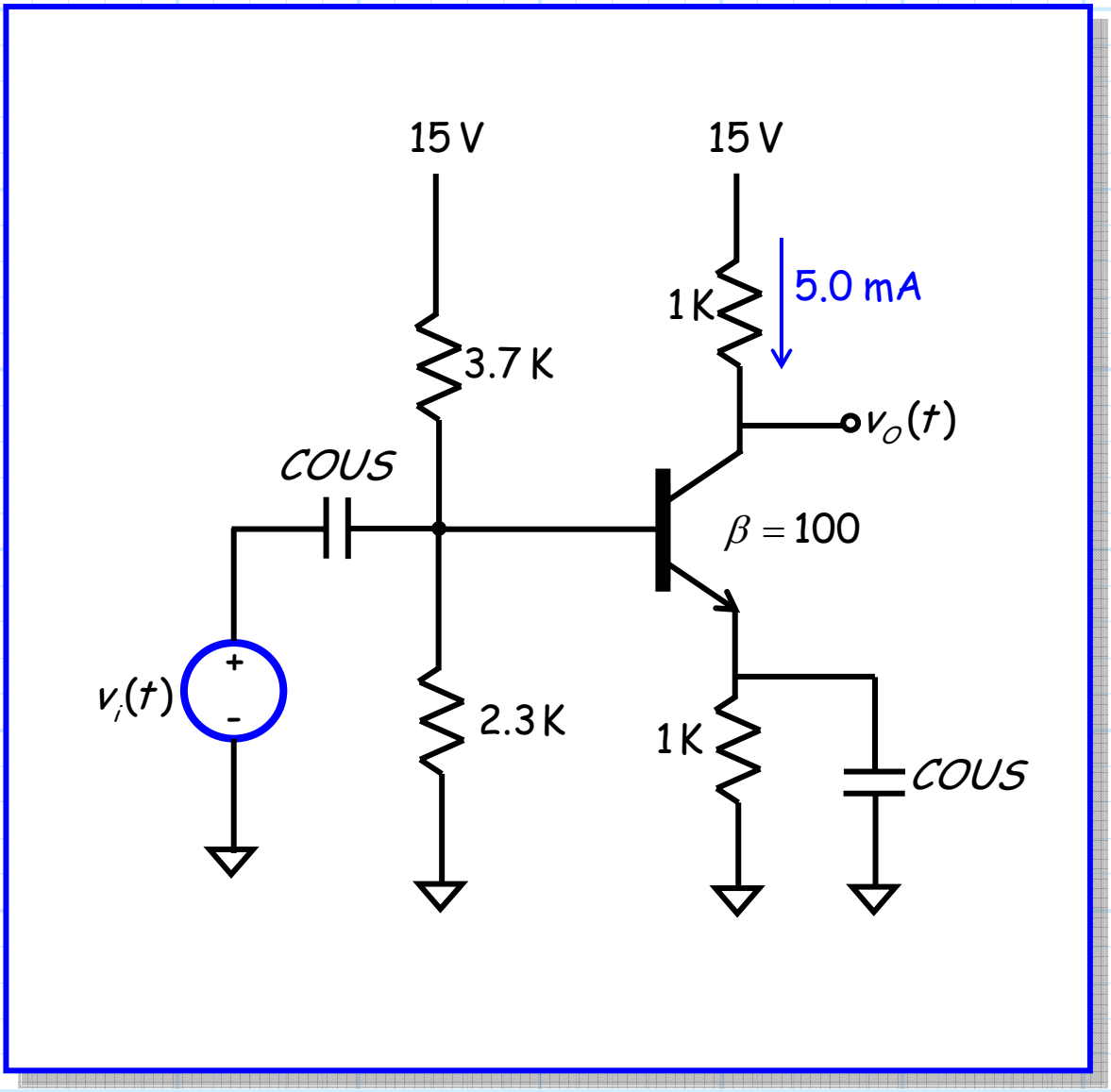
15 V
15 V
1 K
5.0 mA
3.7 K
$v_O(t)$
COUS
$\beta = 100$
$v_i(t)$
+
-
2.3 K
1 K
COUS