Multi-Stage Amplifiers

Consider **all** the types of transistor amplifiers that we have studied (e.g., differential pair, common emitter, source follower, etc.).

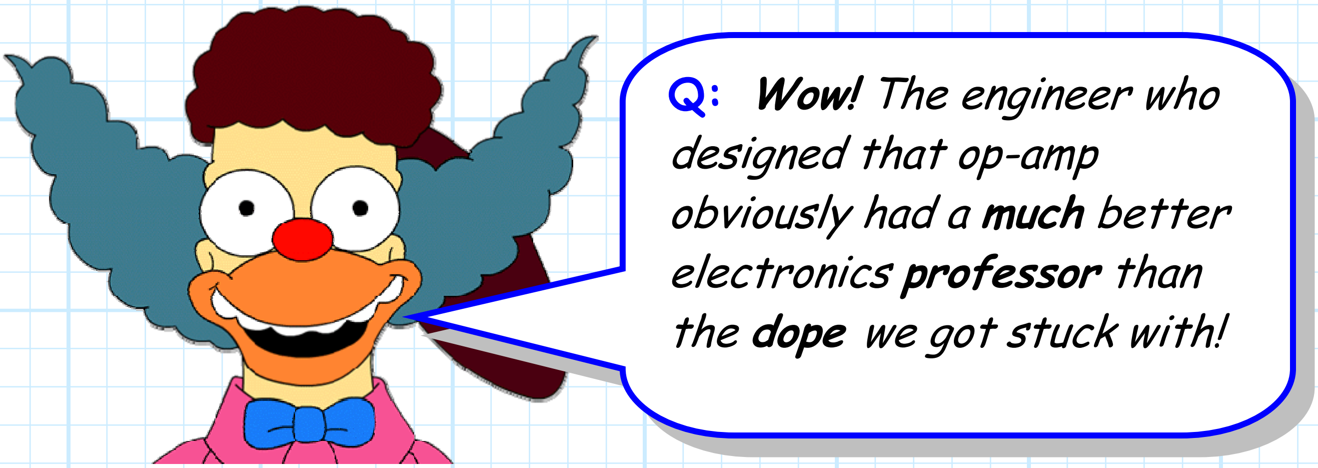
* Each had at least **one attractive** feature (e.g. high open-circuit voltage gain, low output resistance, differential gain, high input resistance, etc.)

* But each also had at least **one sub-optimum** feature (e.g., low-open-circuit voltage gain, low input resistance, high output resistance, etc.).

Q: *Yikes! Is building the perfect amplifier completely **impossible**??*

A: Well, certainly building a **perfect** amplifier is not achievable, but we **can** build amplifiers that are **very, very** good!

For example, consider the op-amp that you use in lab. It had a high input resistance, **and** a very high open-circuit (differential) voltage gain, **and** a low output resistance!



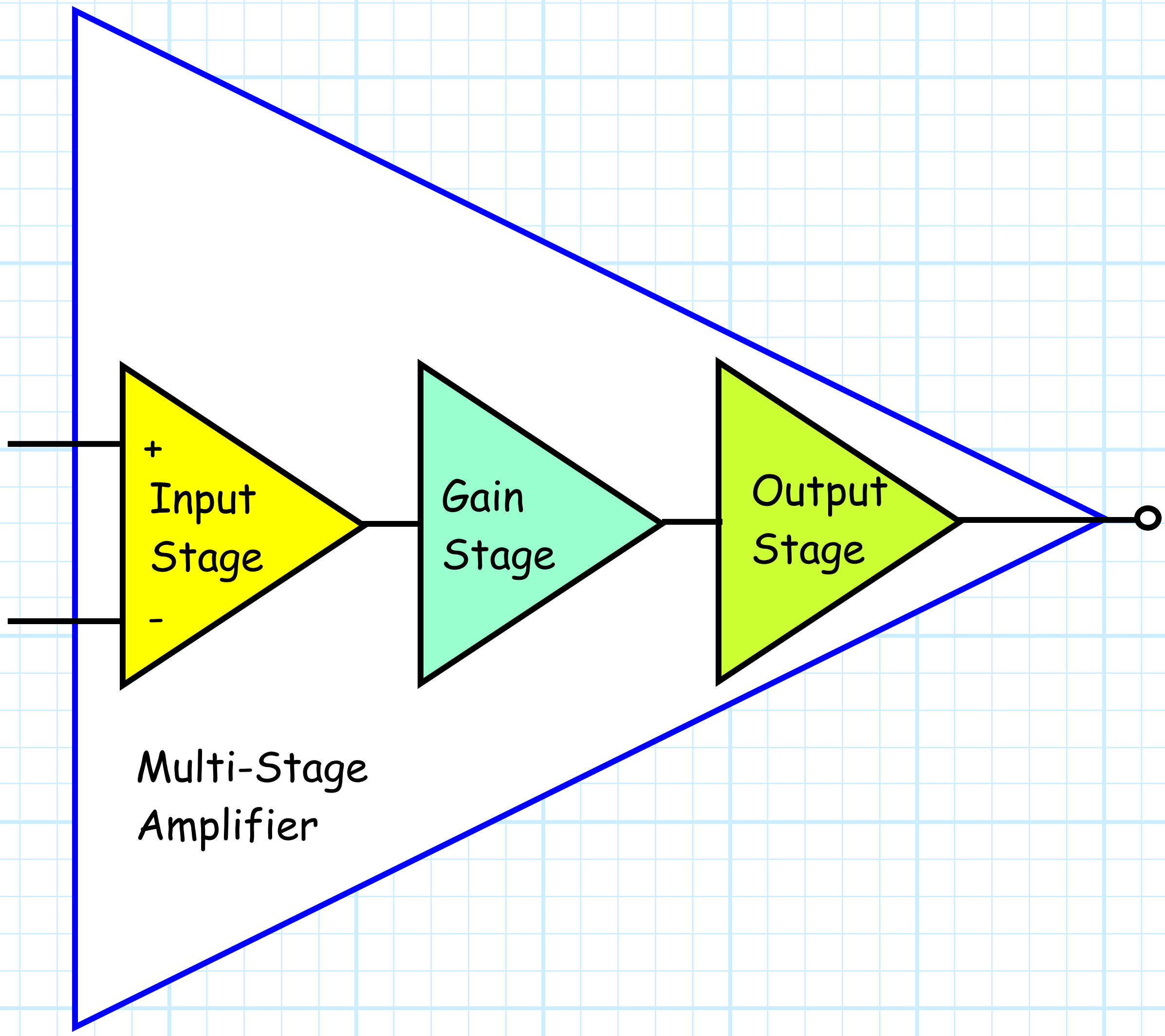
A: **Undoubtedly** so! However, that is **not** the main reason why the designer of your op-amp was successful. For you see, the op-amp you used in the lab was a **multi-stage amplifier!**

A **multi-stage amplifier** is a complex circuit constructed using **several** of the basic designs (e.g., common source, emitter follower) that we have studied. Typically, a multi-stage amplifier consists of **3 sections**:

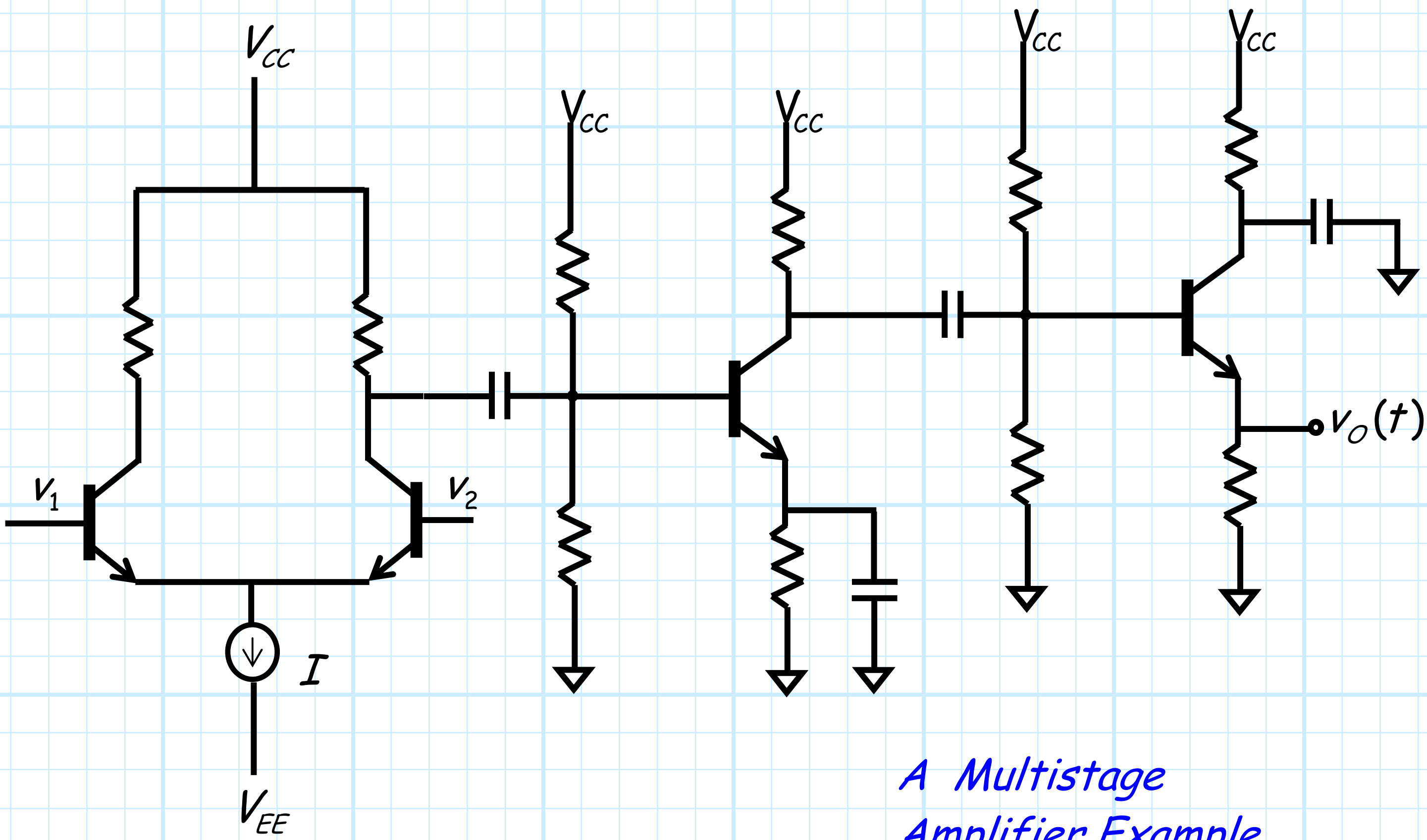
1. **The Input Stage** – This section has one purpose, to provide the multi-stage amplifier with a **high input resistance**. For differential amplifiers, this stage **must** also be a **differential** amplifier (e.g., a differential pair).

2. **The Gain Stages** - This section consists of one or more amplifiers (stages) with **high open-circuit voltage gain** (e.g., common emitter, common source). This section thus provides the required voltage gain for the multi-stage amplifier.

3. **The Output Stage** - The third and final section of the multi-section amplifier likewise has one purpose: to provide the multi-stage amplifier with a **low output resistance**. As such, this stage is often a common collector (emitter follower), or common drain (source follower).



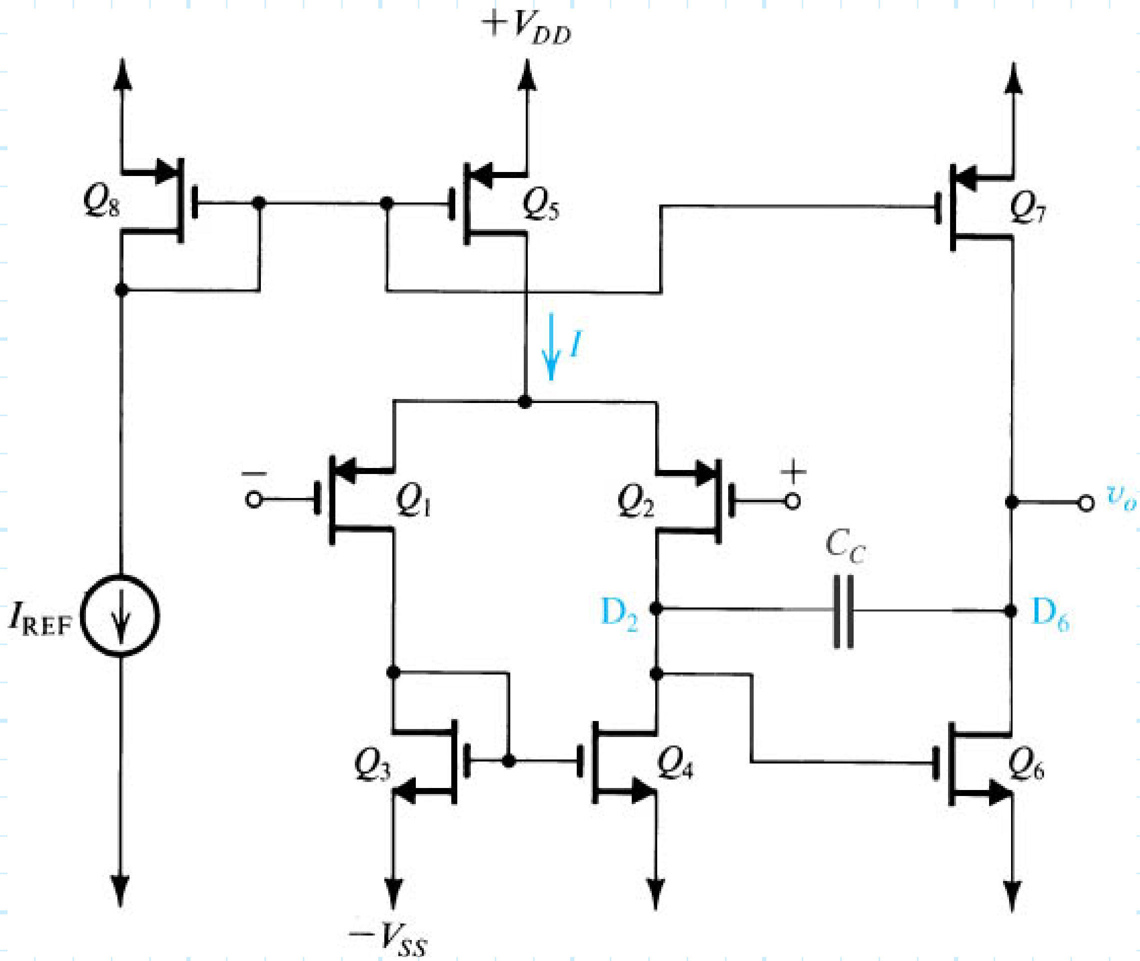
For example, consider this operational amplifier circuit:



A Multistage Amplifier Example

Note the **input** stage is a differential pair, the **gain** stage is common-emitter amp, and the **output** stage is a emitter follower (i.e., common-collector) amp.

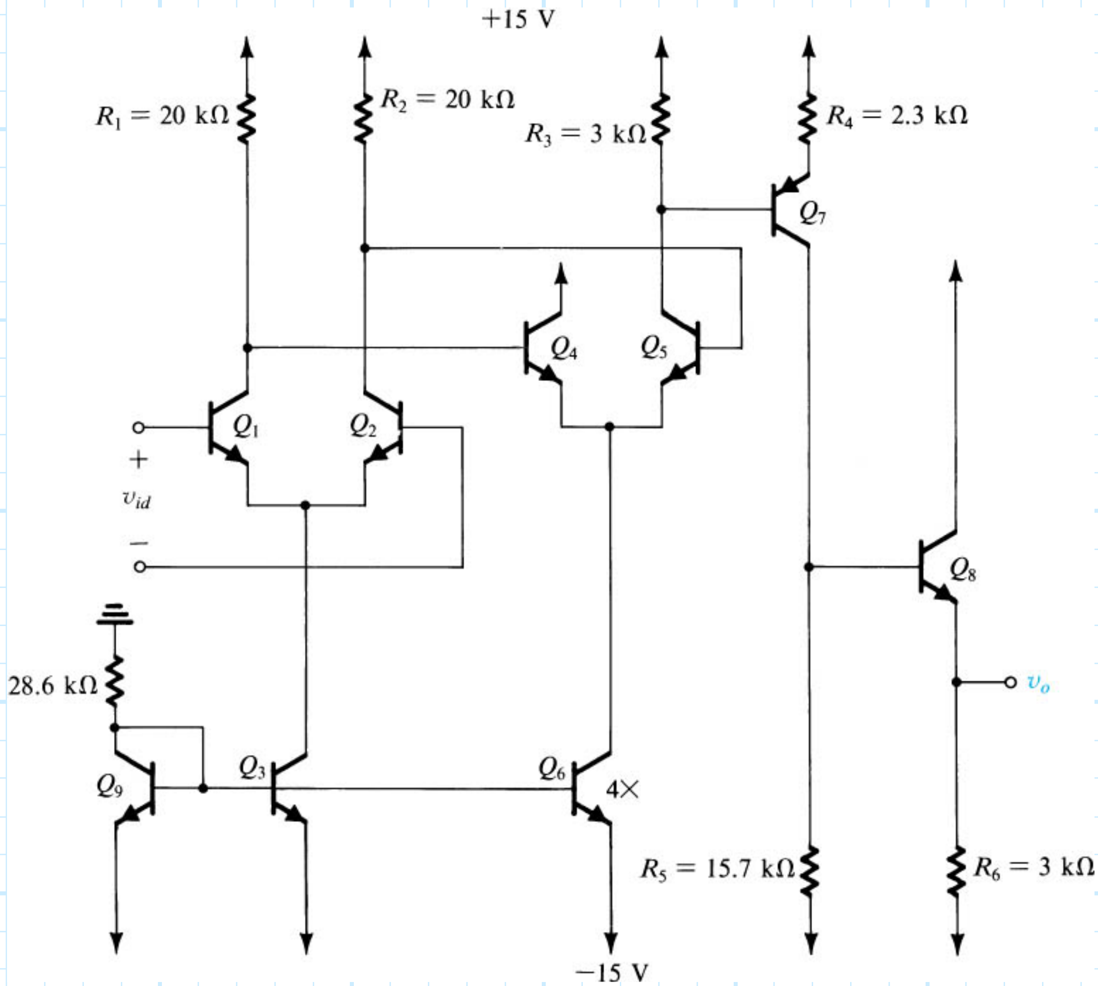
Consider now these **integrated circuit** Multi-Stage Amplifiers:



For this example, Q_8 is a **current source**, with Q_5 and Q_7 parts of a **current mirror**!

Transistor Q_5 provides the current source for a **PMOS differential pair**. PMOS devices Q_1 and Q_2 are the two input transistors for this differential pair, while Q_3 and Q_4 are the **active loads** of the differential pair—they act as the two drain resistors R_D.

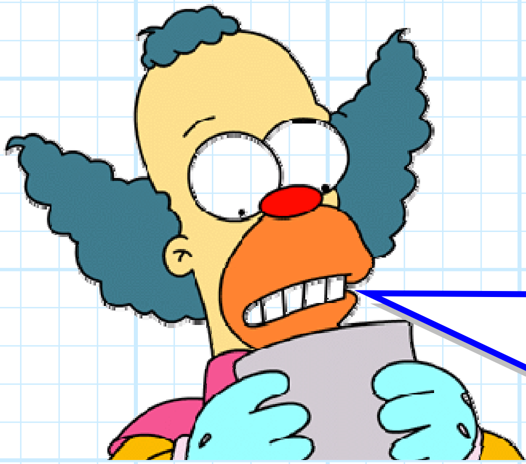
Finally, transistors Q_6 and Q_7 form a **common source** amplifier (high gain!) where the amplifier "load" is the **current source** Q_7. Note that the **output** resistance of this amp is **very high**!



In this multistage circuit, Q_9 forms a **current source**, and Q_3 and Q_6 complete the **current mirror**.

Clearly Q_1 and Q_2 form a **BJT differential pair**, as does transistors Q_4 and Q_5. The first differential pair is the **input** stage, where the second differential pair acts as a **gain** stage (recall the open-circuit voltage gain of a BJT diff. pair is large).

Transistor Q_8 is clearly part of an **emitter-follower** output stage.



Q: ***Wait*** *a second! I see where you have neglected to speak about* ***transistor*** Q_7*. It looks to me that it forms an amplifier that is* ***neither*** *a common emitter* ***nor*** *a common collector configuration!?!*

A: The reason for the section including Q_7 is "**DC shifting**". Note that there are **no** AC coupling (i.e., DC blocking) **capacitors** in this circuit, and thus the DC biasing of one stage **affects** the DC biasing of another.

The circuit associated with Q_7 allows the output of the second differential amplifier to be connected to the input of the emitter-follower without **messing up** the required **DC bias levels** for the collector of Q_5 and the base of Q_8.