Special Problem 4.10-1

A symmetric CMOS inverter has the following parameters:

$$V_{DD} = 5.0 \text{ V}$$

$$K = 0.5 \text{ mA/V}^2$$

$$V_t = 1.0 \text{ V}$$

The inverter output is first connected to an **open circuit**.

A. Determine the value of the **largest input voltage** that will result in an **output voltage** that is considered to be unambiguously a **high output state**.

B. Determine the **operating mode** (i.e., cutoff, saturation, triode) and **drain current** of the **PMOS transistor** if the input voltage is $\mathbf{v_I}$**=2.5**.

C. Now the inverter output is connected to the circuit shown below. Determine the **approximate output voltage** (using any valid simplifying approximation) of the inverter in this case, if the input voltage is $\mathbf{v_I}$ = **0.0 V**.