ADS Overview –Part 2

1. If you have closed ADS, re-open ADS by running the following menu command: **Start->Programs->Advanced Design System 2002C->Advanced Design System**. Then open your project by clicking on  .

2. Close all windows by choosing **File->Close All**. Then open a new design by choosing **File->New Design**. Set the settings as you did in the previous tutorial, only name the design TDR_Simulation. Choose "OK" when you are done.

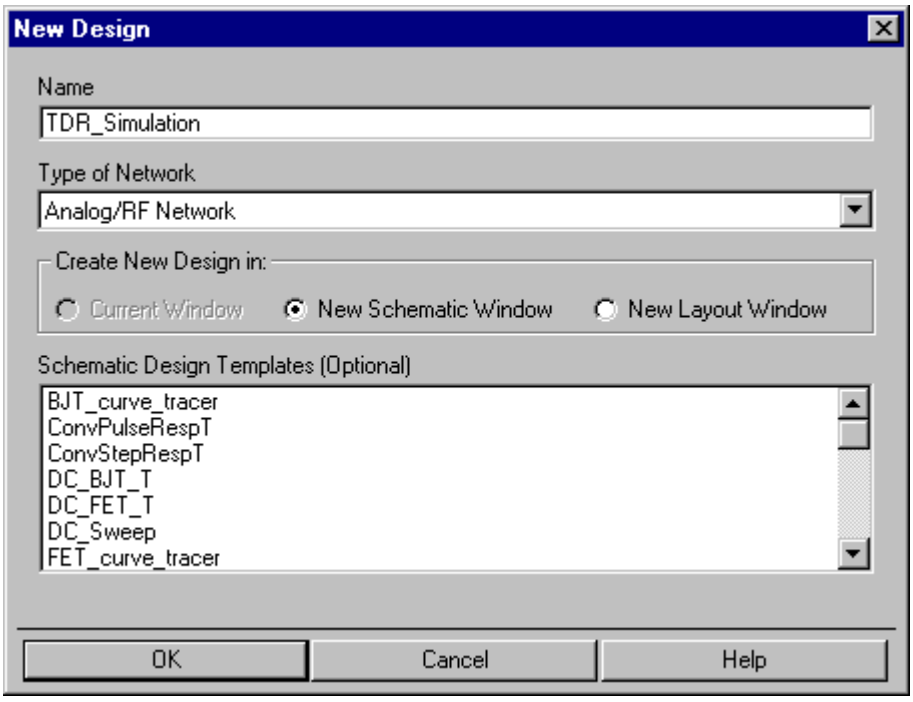

Figure 1: New design for TDR Simulation

3. Add the following components to your design as shown in Figure 2 below. Set the components parameters as shown in the figure.
   a. "Lumped-Components: Capacitor (C)" (rotate component with Ctrl-r)
   b. "Lumped-Components: Resistor (R)"
   c. "Source-Time Domain: Voltage Step (VtStep)"
   d. "TLines-Ideal: Ideal Transmission Line (TLIN)"
   e. "Simulation-Transient: Transient simulation controller (Trans)"
   f. Ground from tool bar.

This setup is similar to what we did in the time domain reflectometry lab. The voltage source is a unit step function which turns on at time = 0 [ns] and rises to 1 [V] instantly. This voltage propagates down the transmission line TLIN, but is split in half because of the voltage division that occurs between generator resistance RG and the characteristic impedance Z of the transmission line. The initial voltage wave is shorted through the capacitor and so the reflected wave completely cancels the forward wave. Then as the capacitor becomes an open circuit the reflected wave transitions from -0.5 [V] to 0.5 [V]. We will look at the voltages at the output of the generator and across the load. Label these nodes as shown in the figure. To label a node, click on 

. This opens the dialogue box shown in Figure 3 below. Type in the label VG and click on the wire between R1 and TL1. Type in the label VC and click on the wire between TL1 and C1. To remove a node label, you can erase the node name in the dialogue box and then click on the wire **or** select the wire and choose **Edit->Wire/Pin Label->Remove Wire/Pin Label**.

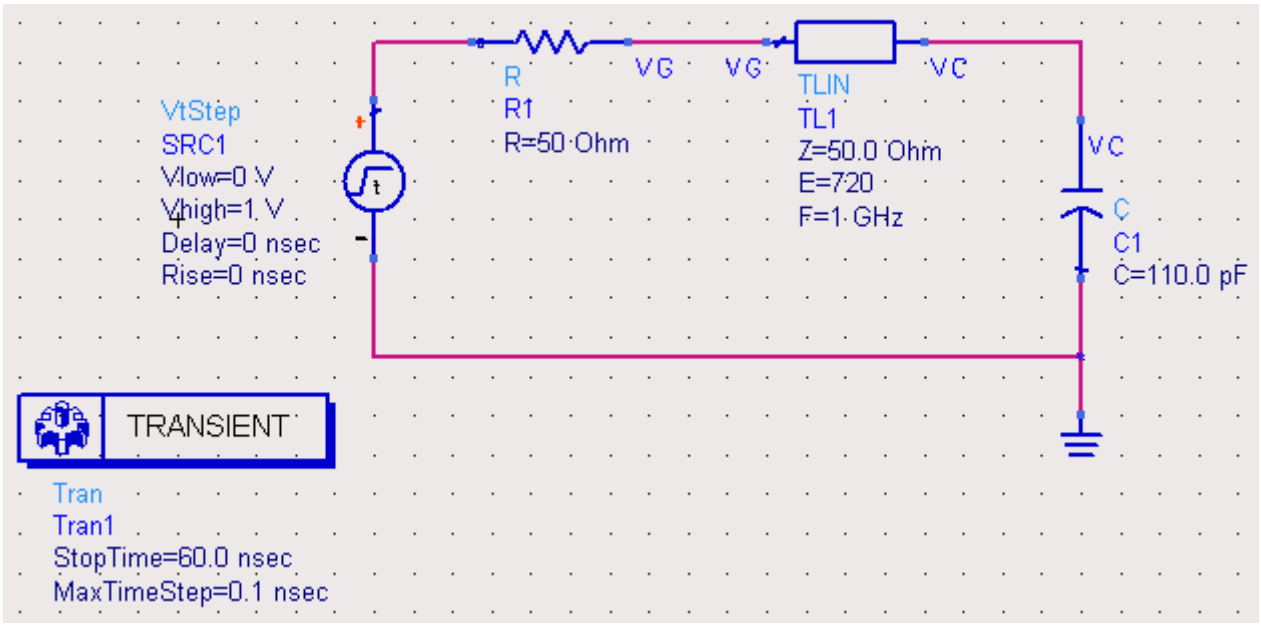

Figure 2: TDR simulation

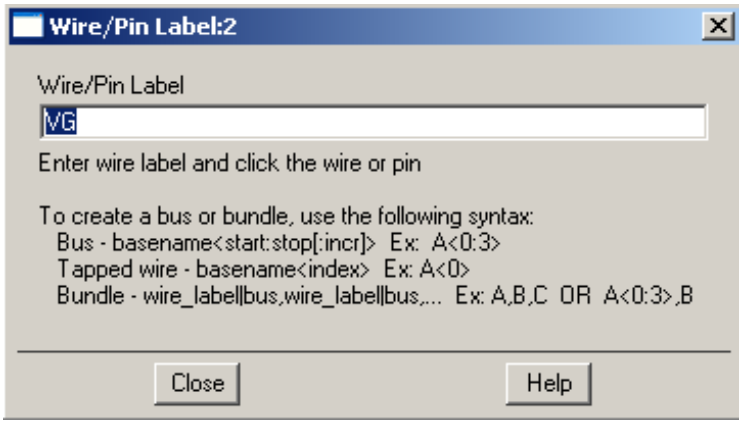

Figure 3:Adding node names

4. Setup your simulation by choosing **Simulate->Setup Simulation**. Set the settings as shown in Figure 4 below. Click on "Apply" to save the settings and then "Cancel" to close the dialogue box.

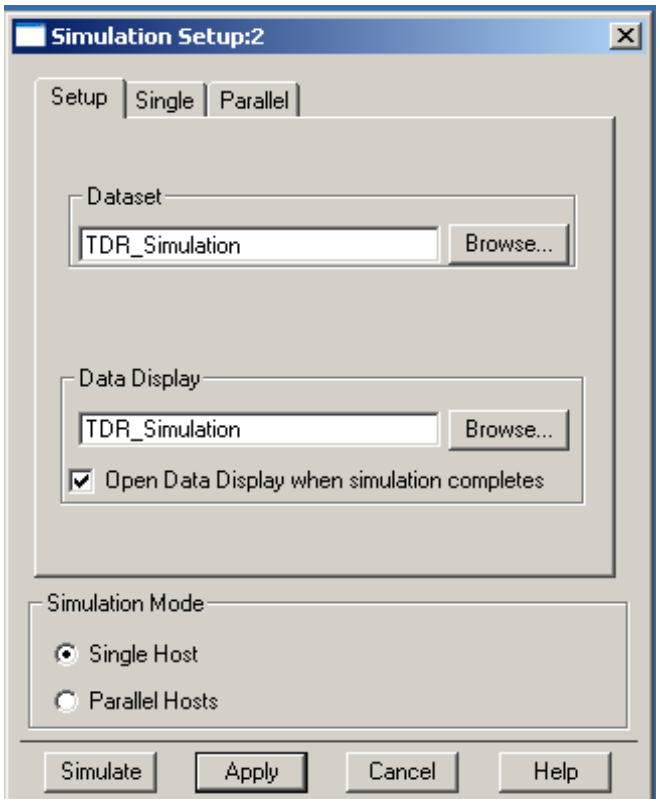

Figure 4: Simulation setup for TDR simulation

5. Now simulate your design by typing F7 or choosing **Simulate->Simulate**. Wait until the data display window opens as shown in Figure 5 below. The data that is

generated from a simulation set is called a data set. The viewer that we use for a dataset is called the data display. We can control where the data is stored and we can control which data display is connected to the schematic. Both the data set and the data display can be saved in separate files. In the data display window, the data display name shows up in the title bar. The default data set of the window is circled in red below. Both of these default to the name we chose for our schematic, but do not have to be the same name.

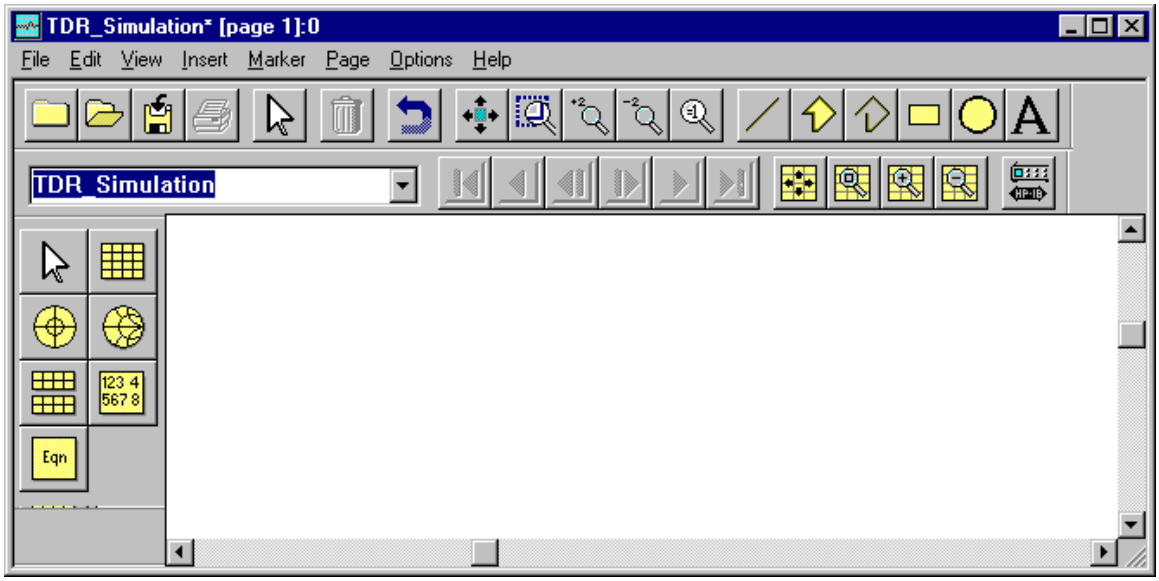

Figure 5: Data display window for TDR simulation

6. Add a rectangular plot by clicking on  . Place the rectangular plot on your data display as you would a component. When you do this, a plot traces and attributes window will open. Select VC and click on ">>Add>>". Then select VG and click on ">>Add>>". We have added two traces: VC versus time and VG versus time. When a transient simulation is done, the assumed x-axis is time. If we had wanted to explicitly set the x and y axes we would choose ">>Add Vs…>>". Your plot attributes window should look like Figure 6 below. Click "OK".

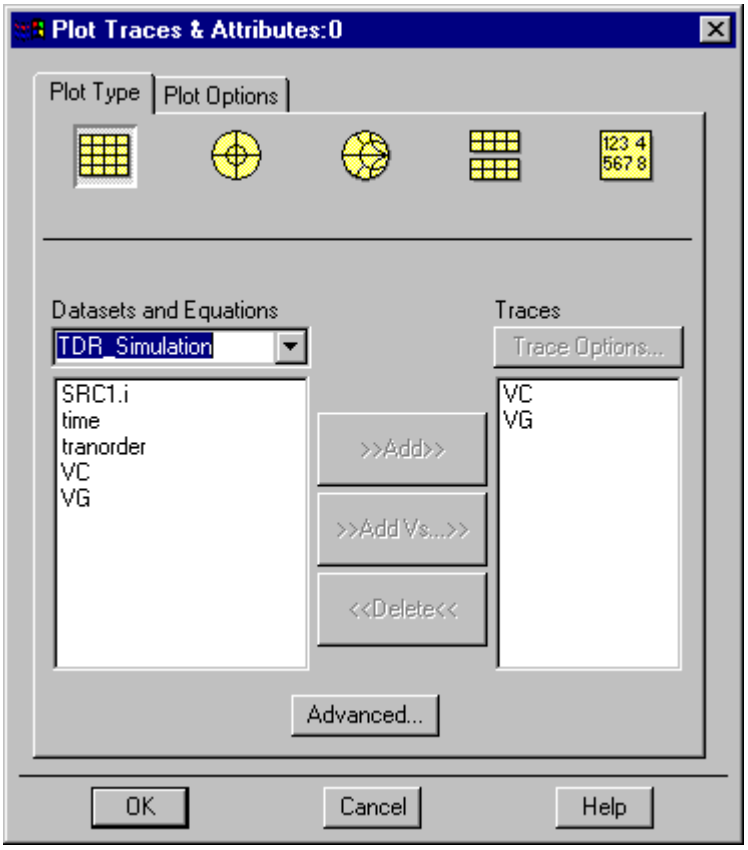

Figure 6: Plots traces and attributes window

7. You should see the graph in if your schematic and simulation are setup correctly. If it doesn't, double check that each of the steps above.

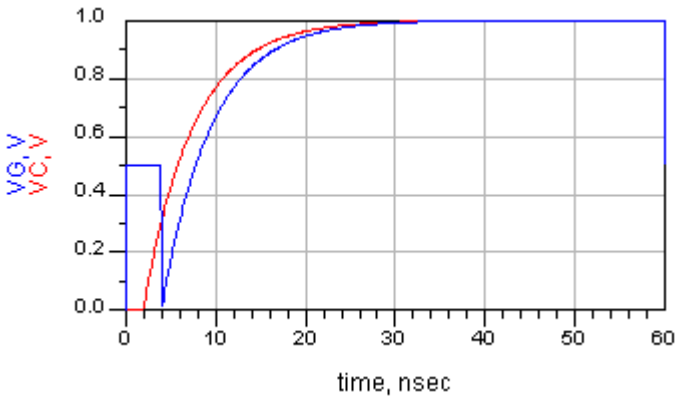

Figure 7: Transient voltages plot