EECS 443 Digital Systems Design
Lecture 1: Introduction
Instructor: Yang (Cindy) Yi
Course Syllabus

Instructor
Dr. Yang (Cindy) Yi
Office: 253 Nichols Hall and 2050 Eaton
Email: yyi@ku.edu
Office Hour: Tues. 10:00 AM - 11:00 AM at 2050 Eaton

Course Website
http://www.ittc.ku.edu/~yangyi/EECS443.html

Means of Communication
Your KU-assigned email will be the official means of communication for this course.

Prerequisites
Students should know conventional techniques in designing digital logic circuits. Prerequisite course is EECS 388. Students required to be taking the lab with the lecture.
Course Syllabus

Course Description

- Top down design methodology for FPGA and ASIC using VHDL
- VHDL modeling, simulation and synthesis tools
  - Combinational-Circuit Building Blocks
  - Sequential-Circuit Building Blocks
- Nexys 4 Artix-7 FPGA architectures and design methodologies with Xilinx Vivado Design Suite
  - Several sample designs are targeted and tested.
- FPGA design flow and design optimization techniques.
Required Textbooks:


Reference Text:

Homework and Lab Assignments:

You will be credited for turning in a complete homework and lab assignments. You are encouraged to see me and teaching assistant for any questions that you might have regarding the assignments and to check your answers against the posted solutions. If you work on your homework, you will be able to do a good job on your exams.

PLEASE NOTE: Partial credit will be given for late homework and lab assignments. You are allowed to discuss homework problems with your classmates but the final solution MUST be completed individually. You are required to STAPLE your assignments.

Exams:

There will be two midterm exams and final exam. No makeup exams will be offered. Exams will be close book and close notes. You are allowed to bring a “cheat sheet”: one A4-sized sheet, using both sides if you wish.
Project:
There will be one final project. The project might be completed in groups of up to three students depending on the complexity of the project. Project topics might be suggested by the student or assigned by the instructor. Project will have to be presented in class.

Class Participations and Pop Up Quiz:
Pop Up Quiz will be held in the beginning / middle of the class. Questions focus on the lecture slides and interview question samples from industrial companies.

Grading:

- Homework 10%
- Lab Assignments 20%
- Exams 30%
- Final Project 25%
- Class Participations and Pop Up Quiz 15%
- Bonus Question Participations 5 Points
What will you learn?

• Gain fundamental knowledge and understanding of principles and practice in digital design through class lectures, reading assignments, and lab experiments using VHDL, FPGA, and ASIC.

• What do we need from VHDL?
  
  - Describe Combinational logic, Level sensitive storage devices, Edge-triggered storage devices
  - Provide different levels of abstraction and support hierarchical design
Why is This Course Worth Taking?

- **VHDL** for synthesis - one of the most sought-after skills
- knowledge of state-of-the-art **tools** used in the industry
- knowledge of the modern **FPGA & ASIC technologies**
- knowledge of state-of-the-art **testing equipment**
- design portfolio that can be used during job interviews
- unique knowledge and practical skills that make you competitive on the job market
Design Process Control from VHDL
Skills Engineers Need to Get Ahead in Their Profession Today

<table>
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<tr>
<th>Skill</th>
<th>North America</th>
<th>Europe</th>
<th>Japan</th>
<th>China</th>
<th>Asia*</th>
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<td>Digital-design skills</td>
<td>74%</td>
<td>56%</td>
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<td>Software-development skills</td>
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<td>Analog-design skills</td>
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<td>Microprocessor-based skills</td>
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<td>Test-engineering skills</td>
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<td>50%</td>
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<tr>
<td>Control-engineering skills</td>
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<td>Mechatronics skills</td>
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<td>Other</td>
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<td>9%</td>
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* Editions of EDN Asia, whose readers were surveyed to obtain these results, serve Hong Kong, India, Korea, Malaysia, Singapore, Taiwan, and Thailand. See www.edn.com/global08 for data broken down by region.
Lab Sections

M 09:00 - 10:50 AM  EATN 2002 - LAWRENCE
W 09:00 - 10:50 AM  EATN 2002 - LAWRENCE
M 03:00 - 04:50 PM  EATN 2002 - LAWRENCE
W 03:00 - 04:50 PM  EATN 2002 – LAWRENCE

• GTA office hours
• You will get your lab access code from Colwell Jr., Thomas G. colwell@ku.edu
• There will be no lab meetings in the first week of classes!
Brief Introduction of the Instructor

- Ph.D. of ECE at Texas A&M University
- Research Intern, IBM
- Senior R&D Engineer, Freescale Semiconductor Inc.
- Senior R&D Engineer, Intel Corporation
- Member of Technical Staff, Texas Instruments Inc.
- Assistant Professor, UMKC.

Website: http://www.ittc.ku.edu/~yangyi/
Brief Introduction of the Instructor

Invited Talks at Industrial Companies:
- IBM/IBM Research (TJ Watson, Austin)
- Intel
- Samsung
- Qualcomm
- Global Foundries
- AMD
- Freescale
- Texas Instruments
- Agilent
- Nvidiia
- Synopsys

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<td>Samsung Electronics(1)</td>
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<td>16</td>
<td>14</td>
<td>Freescale Semiconductor</td>
<td>USA</td>
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</tbody>
</table>
Brief Introduction of the Instructor

• Research Interests:
  ▫ Integrated Circuit Modeling, Simulation, Design
  ▫ Advanced CMOS Device Construction and Process Integration
  ▫ High Speed and Low-Power Circuit Design
How about you?

• Your name, major, year.

• Why you take the course?

• What is your background in electronic circuits (courses & projects)?

• What do you want to learn from this course?

• Hobbies?
Next Class

- What are inside a chip?
- Basic Design Flow
- Design Cycles
- Two major HDLs
- Hardware and Software
- FPGA vs. ASIC
- FPGA Design Process

Read Ch. 2