EECS 443 Digital Systems Design
Lecture 2: Introduction to VHDL
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Outline

• What are inside a chip?
• Basic Design Flow
• Design Cycles
• Two major HDLs
• Hardware and Software
• FPGA vs. ASIC
• FPGA Design Process
Chips Everywhere!
What are inside a chip?

- A chip may include:

- Design issues:

Source: Byran Preas
Chip Design Productivity Crisis

37 Years of Scaling History

- Every generation
  - Feature size shrinks by 70%
  - Transistor density doubles
  - Wafer cost increases by 20%
  - Chip cost comes down by 40%

- Generations occur regularly
  - On average every 2.9 years over the past 35 years
  - Recently every 2 years
Basic Design Flow

- System design
- Logic design
- Physical design
Design and Technology Styles

- **Custom design**
  - Mostly manual design, long design cycle
  - High performance, high volume
  - Microprocessors, analog, leaf cells, IP ...

- **Standard cell**
  - Pre-designed cells, CAD, short design cycle
  - Medium performance, ASIC

- **FPGA/PLD**
  - Pre-fabricated, fast automated design, low cost
  - Prototyping, reconfigurable computing
Solutions

• Apply CAD tools
• High level abstraction

• Learn **HDL**!
Recommended reading

• Wikipedia – The Free On-line Encyclopedia

Two major HDLs

- Verilog
- VHDL
How to learn Verilog by yourself?
How to learn Verilog by yourself?
Course on digital logic/system design with VHDL

Comprehensive introduction to FPGA

Testing equipment
Two Implementation Approaches

**ASIC**
Application Specific Integrated Circuit

**FPGA**
Field Programmable Gate Array
FPGAs vs. ASICs

**ASICs**

**FPGAs**
What is an FPGA?
Design and implement a simple unit permitting to speed up encryption with RC5-similar cipher with fixed key set on 8031 microcontroller. Unlike in the experiment 5, this time your unit has to be able to perform an encryption algorithm by itself, executing 32 rounds.....

Library IEEE;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity RC5_core is
    port(
        clock, reset, encr_decr: in std_logic;
        data_input: in std_logic_vector(31 downto 0);
        data_output: out std_logic_vector(31 downto 0);
        out_full: in std_logic;
        key_input: in std_logic_vector(31 downto 0);
        key_read: out std_logic;
    );
end RC5_core;
FPGA Design process (2)
Next Class

• VHDL Fundamentals
• Design Entity
• Libraries
• STD_LOGIC Demystified
• Modeling Wires and Buses
• Types of VHDL Description (Modeling Styles)