EECS 443 Digital Systems Design
Lecture 8: FSM VHDL Code
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Outline

- Algorithmic State Machine (ASM) Charts
- VHDL Code
- Examples
- Alternative Coding Style
- Control Unit Example: Arbiter
• Required reading
  • P. Chu,
    *FPGA Prototyping by VHDL Examples*
    Chapter 5, FSM

• Recommended reading
  • S. Brown and Z. Vranesic,
    *Fundamentals of Digital Logic with VHDL Design*
    Chapter 8, Synchronous Sequential Circuits
    Sections 8.1-8.5
    Section 8.10, Algorithmic State Machine (ASM) Charts
Review of Previous Classes - 1

Moore FSM

- Output is a Function of the Present State Only

![Diagram of Moore FSM]

- Inputs
- Next State function
- Present State register
- Output function
- Outputs
- Clock
- Reset
Mealy FSM

- Output is a Function of the Present State and the Inputs

Review of Previous Classes - 2
Review of Previous Classes - 3

Elements used in ASM charts

(a) State box
(b) Decision box
(c) Conditional output box
Questions: State Diagrams?
Questions: ASM Chart?

Recognizes Sequence “10”
Questions - Mealy and Moore FSM?

- Fewer states
- Responds one clock cycle earlier
- Lower Area
- Safer. Less likely to affect the critical path.
ASM Chart of Moore Machine

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY FSM_Moore_1 IS
    PORT ( clk : IN STD_LOGIC ;
             reset : IN STD_LOGIC ;
             input : IN STD_LOGIC ;
             output : OUT STD_LOGIC ) ;
END FSM_Moore_1 ;

Recognizes Sequence "10"
ARCHITECTURE behavioral of FSM_Moore_1 IS

END behavioral;
ASM Chart of Mealy Machine

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY FSM_Mealy_1 IS
PORT ( clk : IN STD_LOGIC ;
reset : IN STD_LOGIC ;
input : IN STD_LOGIC ;
output : OUT STD_LOGIC ) ;
END FSM_Mealy_1 ;
ARCHITECTURE behavioral of FSM_Mealy_1 IS

END behavioral;
Pop Up Quiz

Asserts the single output whenever its input string has at least two 1’s in sequence.
VHDL Code
VHDL Code
More Example: Serial Adder

S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*

*Chapter 8, Synchronous Sequential Circuits*

*Sections 8.5: Series Adder example*

Mealy-type serial adder FSM

Moore-type serial adder FSM
Alternative Coding Style

Process(Present State, Input)

Process(clk, reset)

Based on RTL Hardware Design by P. Chu
ASM Chart of Moore Machine

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY FSM_Moore_2 IS
  PORT ( clk : IN STD_LOGIC;
         reset : IN STD_LOGIC;
         input : IN STD_LOGIC;
         output : OUT STD_LOGIC );
END FSM_Moore_2 ;
ARCHITECTURE behavioral of FSM_Moore_2 IS

END behavioral;
ASM Chart of Mealy Machine

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY FSM_Mealy_2 IS
    PORT ( clk : IN STD_LOGIC;
            reset : IN STD_LOGIC;
            input : IN STD_LOGIC;
            output : OUT STD_LOGIC);
END FSM_Mealy_2;

END ASM Chart of Mealy Machine;
ARCHITECTURE behavioral of FSM_Mealy_2 IS

END behavioral;
Control Unit Example: Arbiter

• Design of an FSM that is slightly more complex than the previous examples.
• The purpose of the machine is to control access by various devices to a shared resource in a given system. Only one device can use the resource at a time.
• Assume that all signals in the system can change values only on the positive edge of the clock signal. Each device provides one input to the FSM, called a request, and the FSM produces a separate output for each device, called a grant.
Control Unit Example: Arbiter

Assume that there are three devices in the system, called device 1, device 2, and device 3. The request signals are named \( r_1 \), \( r_2 \), and \( r_3 \), and the grant signals are called \( g_1 \), \( g_2 \), and \( g_3 \). Device 1 has the highest priority.
State Diagram

Moore-type machine
Simplified State Diagram

Alternative style of state diagram for the arbiter
ASM Chart for Control Unit

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY arbiter IS
    PORT ( Clk, Reset: IN STD_LOGIC ;
        r: IN STD_LOGIC_VECTOR(1 TO 3) ;
        g: OUT STD_LOGIC_VECTOR(1 TO 3)
    );
END arbiter ;
VHDL code of arbiter - Style 1

ARCHITECTURE Behavior OF arbiter IS
  TYPE State_type IS (Idle, gnt1, gnt2, gnt3);
  SIGNAL y : State_type;
END Behavior ;
ARCHITECTURE Behavior OF arbiter IS
    TYPE State_type IS (Idle, gnt1, gnt2, gnt3);
    SIGNAL y, y_next : State_type;
VHDL code of arbiter - Style 2

END Behavior ;
Simulation results for the arbiter circuit
Next Class

- VGA – Video Graphics Array
- VGA – Characteristic Features
- Operation of a CRT monitor
- VGA Controller

P. Chu, *FPGA Prototyping by VHDL Examples*

*Chapter 12, VGA Controller I: Graphic*