1. Please discuss the advantages and disadvantages of the following IC design styles: (1) custom design; (2) standard cell design; (3) FPGA.

Solutions:

1. (a) Advantages of custom design:
   - High performance: Low power, high speed & minimum area
   - Suitable for high end application so that the high volume offset the high design time and high cost.

Disadvantages of custom design:

   - High cost
   - High development time
   - Manual design
   - Mask creation

(b) Advantages of standard cell design:

   - Suitable for medium performance requirement
   - Short design phase due to the use of standard cells and CAD tools
   - Placement & routing of standard cells only

Disadvantages of standard cell design:

   - Not suitable for high performance requirement
   - High cost design revision

(c) Advantages of FPGA and PLD based design:

   - Low cost
   - Suitable for rapid prototyping
   - Suitable for low end application
   - Low cost design revisions.

Disadvantages of FPGA and PLD based design:

   - Low performance
2. Please discuss the advantages and disadvantages of those two implementation approaches: (1) FPGA (2) ASIC.

Solutions:

- **ASIC:** Application Specific Integrated Circuit: designed all the way from behavioral description to physical layout, designs must be sent for expensive and time consuming fabrication in semiconductor foundry

- **FPGA:** Field Programmable Gate Array: no physical layout design; design ends with a bitstream used to configure a device; bought off the shelf and reconfigured by designers themselves

3. Please discuss the advantages and disadvantages of those two hardware description languages: (1) Verilog (2) VHDL

Solution:

Verilog

Slightly better at gate/transistor level

Language style close to C/C++

Pre-defined data type, easy to use

VHDL

Slightly better at system level

Language style close to Pascal

User-defined data type, more flexible

Equally effective, personal preference
4. Please write the symbol and truth table of Basic Gates – AND, OR, NOT, NAND, NOR

5. Derive the truth table for the function \( f(x_1, x_2, x_3, x_4) = \)

\[
x_1 \overline{x}_3 \overline{x}_4 + x_2 \overline{x}_3 x_4 + x_1 \overline{x}_2 \overline{x}_3
\]

\[
\Rightarrow f(x_1, x_2, x_3, x_4) = x_1 x_3 \overline{x}_4 + x_2 \overline{x}_3 x_4 + x_1 x_2 \overline{x}_3
\]

\[
= x_1 x_3 \overline{x}_4 + x_2 \overline{x}_3 x_4 + x_1 x_2 \overline{x}_3
\]

\[
= x_1 x_3 \overline{x}_4 + x_2 \overline{x}_3 x_4 + x_1 \overline{x}_3
\]

\[
= x_2 \overline{x}_3 x_4 + x_1 \overline{x}_3 = (x_2 \overline{x}_4 + x_1) \overline{x}_3
\]
6. Use DeMorgan’s theorem to implement the sum of products of problem 5 using only NAND and NOR gates. (Hint: Read examples 2.6 and 2.7 in the supplemental materials).