1. Consider the VHDL code below. What type of circuit does the code represent? Comment on whether or not the style of code used is a good choice for the circuit that it represents.

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY problem IS
    PORT ( w : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
           En : IN STD_LOGIC;
           y0, y1, y2, y3 : OUT STD_LOGIC );
END problem;

ARCHITECTURE Behavior OF problem IS
BEGIN
    PROCESS (w, En)
    BEGIN
        y0 <= '0'; y1 <= '0'; y2 <= '0'; y3 <= '0';
        IF En = '1' THEN
            IF w = "00" THEN y0 <= '1';
            ELSIF w = "01" THEN y1 <= '1';
            ELSIF w = "10" THEN y2 <= '1';
            ELSE y3 <= '1';
            END IF;
        END IF;
    END PROCESS;
END Behavior;
```

2. Show how the function

\[ f(w_1, w_2, w_3) = \sum m(0, 2, 3, 4, 5, 7) \]

be implemented using a 3-to-8 binary decoder and an OR gate.

3. Write VHDL code that represents the function in problem 2, using one selected signal assignment.

4. Using a conditional signal assignment, write VHDL code for an 8-to-3 priority encoder.

5. Repeat problem 4, using an if-then-else statement.