1. Consider the VHDL code in Figure P6.2. What type of circuit does the code represent? Comment on whether or not the style of code used is a good choice for the circuit that it represents.

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY problem IS
  PORT ( w : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
         En : IN STD_LOGIC;
         y0, y1, y2, y3 : OUT STD_LOGIC );
END problem;

ARCHITECTURE Behavior OF problem IS
BEGIN
  PROCESS (w, En)
  BEGIN
    y0 <= '0'; y1 <= '0'; y2 <= '0'; y3 <= '0';
    IF En = '1' THEN
      IF w = "00" THEN y0 <= '1';
      ELSIF w = "01" THEN y1 <= '1';
      ELSIF w = "10" THEN y2 <= '1';
      ELSE y3 <= '1';
      END IF;
    END IF;
  END PROCESS;
END Behavior;
```

The code is a 2-to-4 decoder with an enable input. It is not a good style for defining this decoder. The code is not easy to read. Moreover, the VHDL compiler often turns if statements into multiplexers, in which case the resulting decoder may have multiplexers controlled by the $En$ signal on the output side.

2. Show how the function

$$f(w_1, w_2, w_3) = \sum m(0, 2, 3, 4, 5, 7)$$

be implemented using a 3-to-8 binary decoder and an OR gate.
3. Write VHDL code that represents the function in problem 2, using one selected signal assignment.

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY prob6.19 IS
  PORT ( w : IN STD_LOGIC_VECTOR(1 TO 3);
         f : OUT STD_LOGIC);
END prob6.19;

ARCHITECTURE Behavior OF prob6.19 IS
BEGIN
  WITH w SELECT
  f <= '0' WHEN "001",
       '0' WHEN "110",
       '1' WHEN OTHERS;
END Behavior;
```

4. Using a conditional signal assignment, write VHDL code for an 8-to-3 priority encoder.

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY prob6.24 IS
  PORT ( w : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
         y : OUT STD_LOGIC_VECTOR(2 DOWNTO 0);
         z : OUT STD_LOGIC);
END prob6.24;

ARCHITECTURE Behavior OF prob6.24 IS
BEGIN
  y <= "111" WHEN w(7) = '1' ELSE
       "110" WHEN w(6) = '1' ELSE
       "101" WHEN w(5) = '1' ELSE
       "100" WHEN w(4) = '1' ELSE
       "011" WHEN w(3) = '1' ELSE
       "010" WHEN w(2) = '1' ELSE
       "001" WHEN w(1) = '1' ELSE
       "000";
  z <= '0' WHEN w="00000000" ELSE '1';
END Behavior;
```

5. Repeat problem 4, using an if-then-else statement.
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY prob6_25 IS
  PORT ( w : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
         y : OUT STD_LOGIC_VECTOR(2 DOWNTO 0);
         z : OUT STD_LOGIC);
END prob6_25;

ARCHITECTURE Behavior OF prob6_25 IS
BEGIN
  PROCESS ( w ) BEGIN
    IF w(7) = '1' THEN
      y <= "111";
      ELSIF w(6) = '1' THEN
        y <= "110";
      ELSIF w(5) = '1' THEN
        y <= "101";
      ELSIF w(4) = '1' THEN
        y <= "100";
      ELSIF w(3) = '1' THEN
        y <= "011";
      ELSIF w(2) = '1' THEN
        y <= "010";
      ELSIF w(1) = '1' THEN
        y <= "001";
      ELSE
        y <= "000";
      END IF;
    IF w = "00000000" THEN
      z <= '0';
    ELSE
      z <= '1';
    END IF;
  END PROCESS;
END Behavior;