1. Consider the timing diagram in Figure 1, assuming that the $D$ and $Clock$ inputs shown are applied to the circuit in Figure 2, draw waveforms for the $Q_a$ and $Q_b$.

2. Draw the timing diagram of a four-bit counter.
3. (1) Explain the difference between synchronous circuits and asynchronous circuits. (2) Draw the output waveform of both the synchronous circuits and asynchronous D Flip Flop.

![D Flip Flop Diagram]

4. Write the VHDL code for 8-bit register with asynchronous reset

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY reg8 IS
    PORT(
        D, Reset, Clock : IN STD_LOGIC;
        Q : OUT STD_LOGIC_VECTOR(7 DOWNTO 0)
    );
END reg8;
```

5. We discussed the 4 bit up-counter with synchronous reset in our class. Please write the VHDL code for 4-bit up-counter with asynchronous reset.

```vhdl
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;

ENTITY upcount_ar IS
    PORT(
        Clock, Reset : IN STD_LOGIC;
        Q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
    );
END upcount_ar;
```