1. Consider the timing diagram in Figure 1, assuming that the $D$ and $Clock$ inputs shown are applied to the circuit in Figure 2, draw waveforms for the $Q_a$ and $Q_b$.

Solution:
2. Draw the timing diagram of a four-bit counter.

Solution:

3. (1) Explain the difference between synchronous circuits and asynchronous circuits. (2) Draw the output waveform of both the synchronous circuits and asynchronous D Flip Flop.

Solution:
4. Write the VHDL code for 8-bit register with asynchronous reset

```
ARCHITECTURE behavioral OF reg8 IS
BEGIN
  PROCESS ( Reset, Clock )
  BEGIN
    IF Reset = '1' THEN
      Q <= "00000000" ;
    ELSIF rising_edge(Clock) THEN
      Q <= D ;
    END IF ;
  END PROCESS ;
END behavioral ;
```

5. We discussed the 4 bit up-counter with synchronous reset in our class. Please write the VHDL code for 4-bit up-counter with asynchronous reset.
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;

ENTITY upcount_ar IS
  PORT ( Clock, Reset : IN STD_LOGIC;
         Q : OUT STD_LOGIC_VECTOR (3 DOWNTO 0));
END upcount_ar;

Solution:
ARCHITECTURE behavioral OF upcount_ar IS
  SIGNAL Count : STD_LOGIC_VECTOR (3 DOWNTO 0);
BEGIN
  PROCESS (Clock, Reset)
  BEGIN
    IF Reset = '1' THEN
      Count <= "0000";
    ELSIF rising_edge(Clock) THEN
      Count <= Count + 1;
    END IF;
  END PROCESS;
  Q <= Count;
END behavioral;