EECS 140/141 Introduction to Digital Logic Design
Spring Semester 2017
Assignment #12 Due 18 April 2017

Reading: Sections 7.4 - 7.9 in Brown/Vranesic

1. Problem 7.1, p. 476, concerning D latches and flip-flops.


3. Starting with Figure 7.11 on p. 393 of your textbook, replace every NAND gate with a NOR gate, keeping all the labels for the various inputs, outputs, and intermediate signals. Explain how the resulting circuit is a negative-edge-triggered D FF. Specifically, provide an explanation of its operation similar to what is contained in the first two paragraphs of section 7.4.2.


5. Problem 7.13, p. 478 in Brown/Vranesic, concerning a universal shift register. This problem is not very well specified, so here are some more specifications. Do this problem for a 4-bit register. We clearly need 2 binary inputs: one to specify the direction of the shift and the other to specify whether or not to use the parallel load feature. Let these two inputs be defined as follows. Let $S$ be the binary input that specifies the shift direction: if $S = 0$, the circuit should shift right, and if $S = 1$, the circuit should shift left. Then let $L$ be the parallel load control: if $L = 1$, the circuit should load bits $r_3r_2r_1r_0$ into the register.

6. Problem 7.40, part (a) only, p. 482, concerning a control circuit.