Design and Implementation of a Link Level Adaptive Software Radio

Information & Telecommunication
Technology Center

Richard A. Killoy

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Presentation Overview

- Brief Overview of RDRN
- Motivation - Why build this radio?
- Transceiver System Level Description
- Transmit and Receive Chain Implementation
- Summary & Future Work

RDRN Overview

- Design High-Speed wireless ATM/IP Comm. Systems with Network and DLL adaptability which are rapidly deployable.
- Sponsored by DARPA's GLO-MO initiative

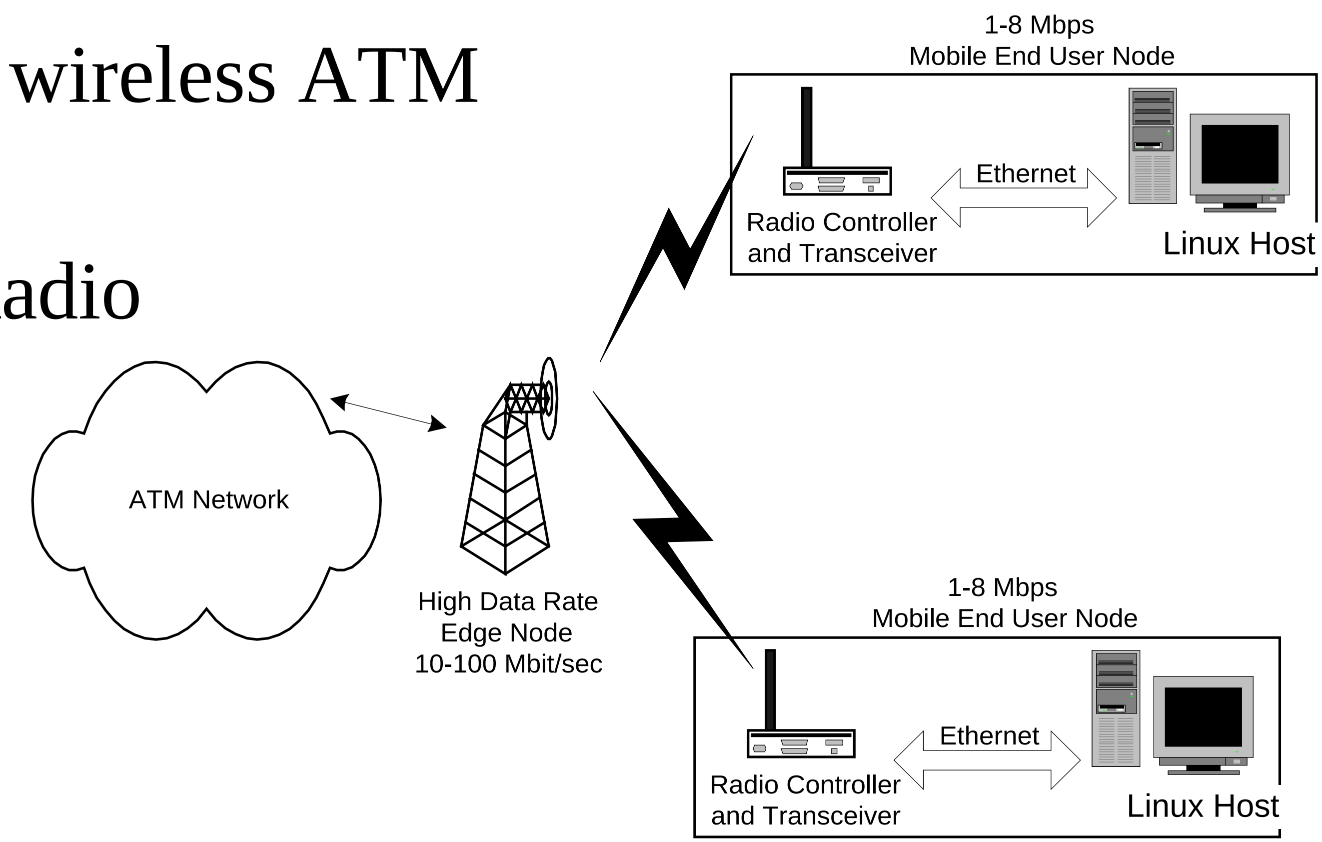
<u>This years goals</u>:

- Channel Estimation & Link Adaptation
- Software Radios
- Adaptive Networking
- Resource Reservation Styles
- Comparative Performance Evaluation of IP vs. ATM

RDRN System Architecture

Three Overlaid Radio Networks:

- Low-Power Orderwire for signaling
- High Capacity wireless ATM backbone
- Cellular-like Radio Network for ATM access to end users

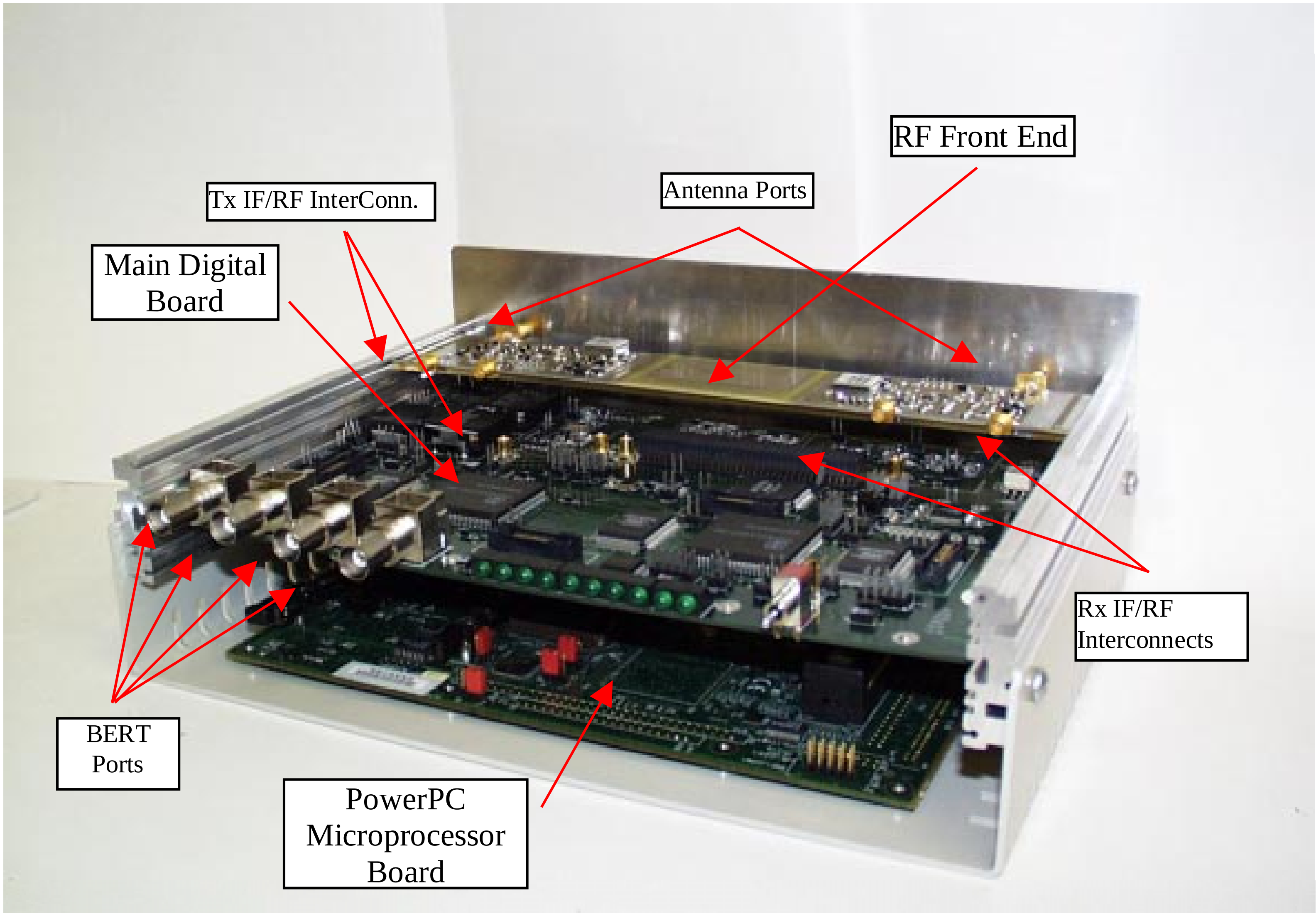


Motivation

Goal	Solution Strategy Employed
Channel Estimation Algorithms	The use of adaptive equalization, functioning as channel estimators.
Link Level Adaptation Algorithms	Software radio allows us the flexibility to change link level parameters.
Radios to Test, Evaluate, and Validate the channel estimation and link-level algorithms	Software radios implementing the use of high-speed ADC and various DSP chips. These chips can be programmed dynamically via a PowerPC processor.

Adaptive Parameter	Allowable Values
RF Section	
Transmit Power Control, TPC	5 dBm to 25 dBm in 2 dB increments
Carrier Frequency	Carrier frequency can be tuned within RF bandwidth in increments of 10 MHz
*RF Front End	Static Design, but supports 5.3 GHz, 2.4 GHz, and 1.2 GHz band.
Physical Layer	
Modulation format	BPSK, QPSK
Data Rate	1, 2, 4 MSPS
Data Link Layer	
FEC	Limited by complexity of combinational logic circuit implemented in Alteras
Multiple Access Scheme	TDMA, FDMA or hybrid combination of both
RF Preamble for TDMA	Limited by length of time slot
HDLC Frame Length	Limited by Ethernet Packet Size, 1.5 kB

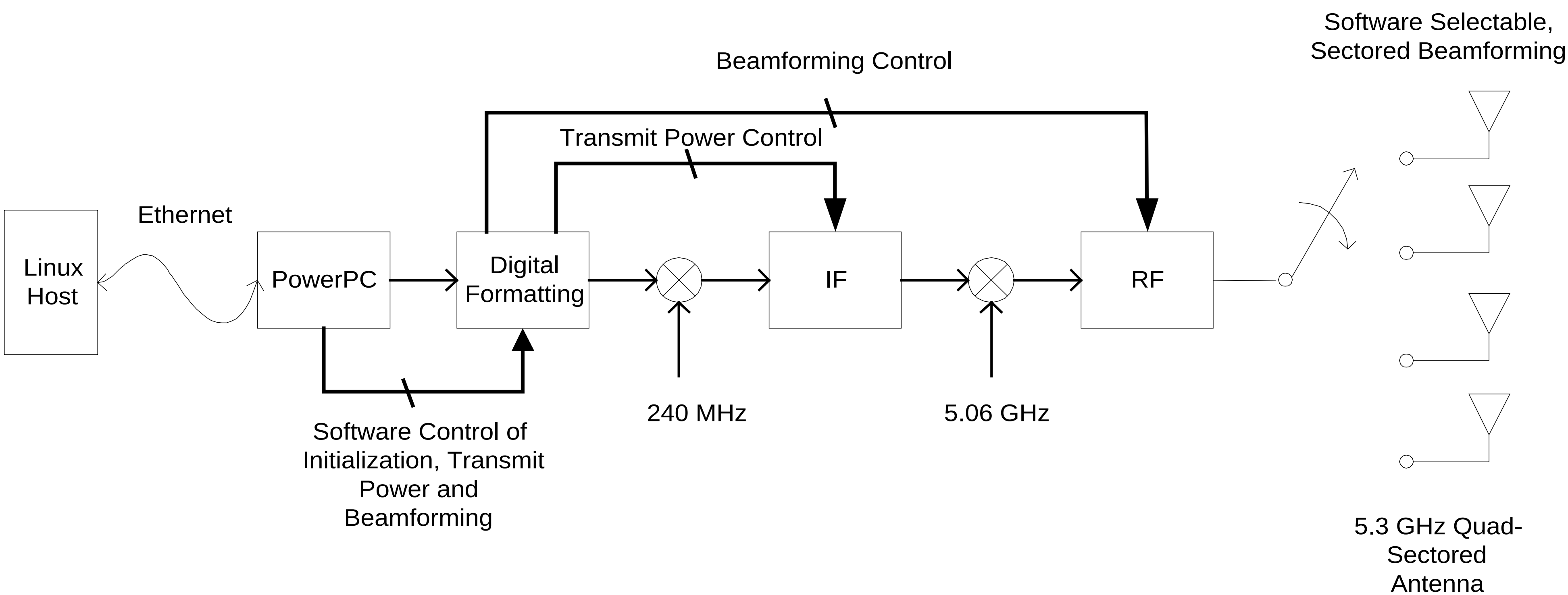
Complete System Including Housing



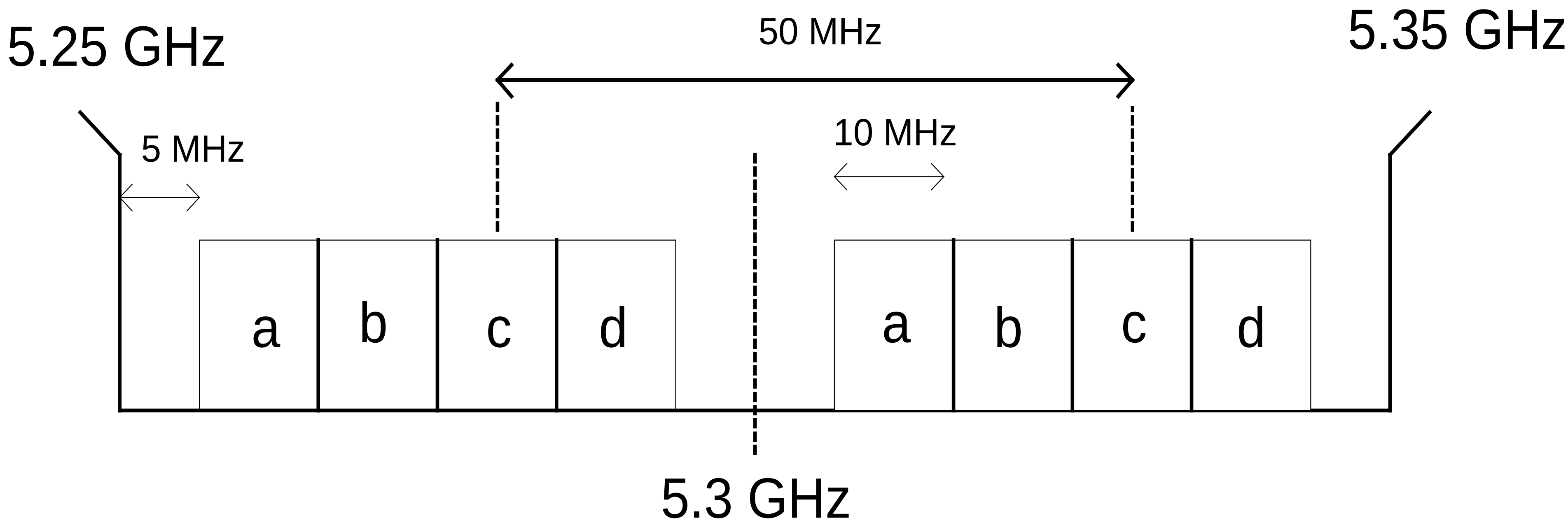
Transmitter Requirements

- Transmit within RF bands at 5.3 GHz, 2.4 GHz, and 1.2 GHz
- Frequency Agility – ability to select from multiple channels within each RF band
- Average power output of +30 dBm (1W) from each antenna
- RF Bandwidth = 100 MHz
- Channel BW = 10 MHz
- Selectable QPSK or BPSK modulation
- Symbol Rates of 1, 2, or 4 Msymbols/sec
- Multiple Access: FDD with TDMA/FDMA
- Transmit Power Control (2 dB steps from 5 dBm to 25 dBm)
- Transmit Power ON/OFF capability (TDMA)
- TxData received from PowerPC
- LO Spurious level = -28 dBm
- LO Phase Noise <= -130 dBc/Hz at 50 MHZ offset

Transmitter System Level Diagram



Spectrum Utilization



4 TX Channels

4 RX Channels

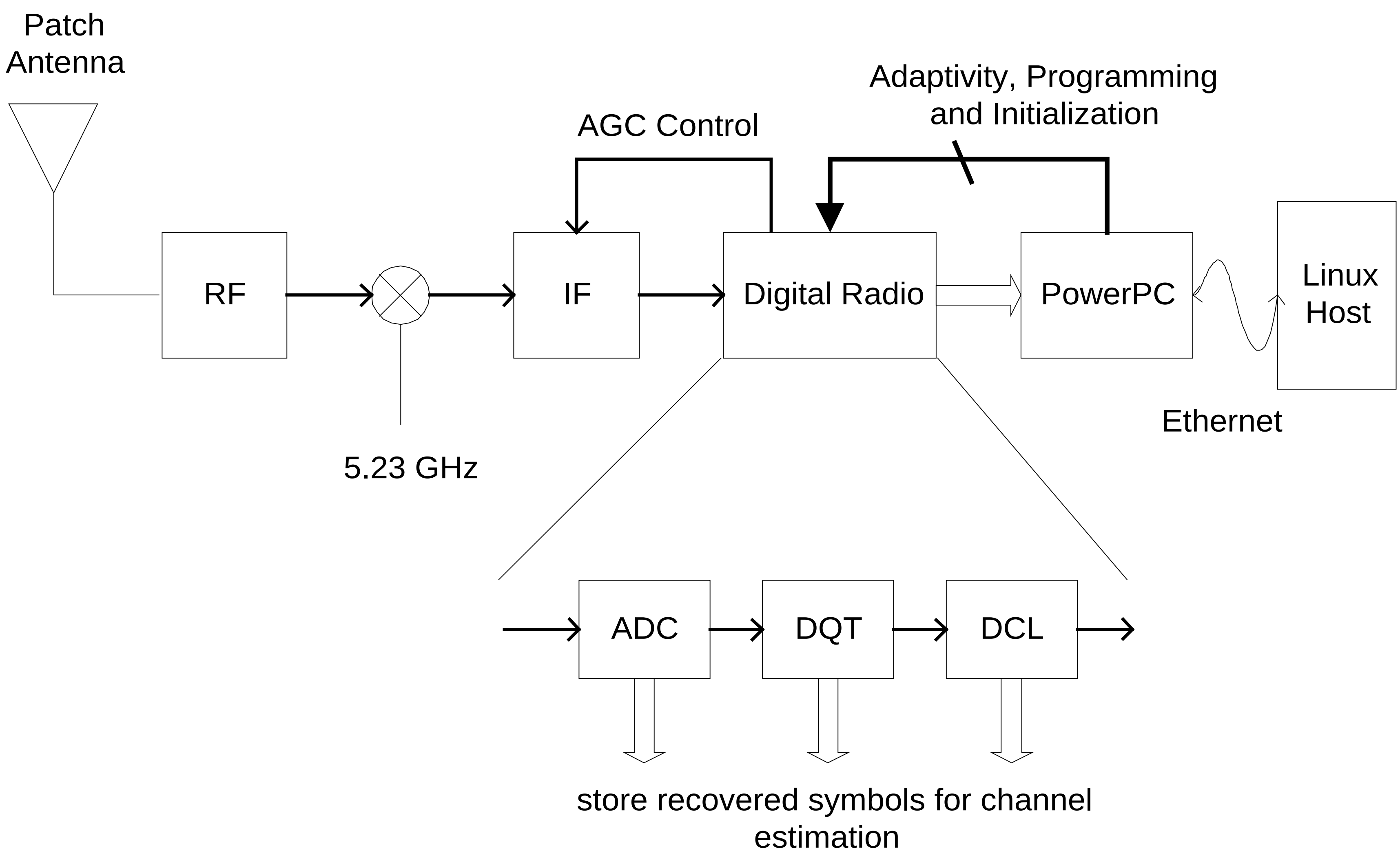
1 Channel = 10 MHz

RF Band = 100 MHz

Receiver Requirements

- Receive within RF bands at 5.3 GHz, 2.4 GHz and 1.2 GHz
- Frequency Agility – ability to select from four channels within RF band
- Full Duplex Operation
- Digital IF Architecture (subsampling)
- Demodulate QPSK or BPSK modulation
- Receiver band selectivity = 100 MHz
- Receiver channel selectivity = 10 MHz
- Symbol Rates from 1, 2 or 4 MSymbols/sec
- Dynamically configurable – must be a multidimensional radio with varying software profiles (Software Radio)
- RxData passed to PowerPC
- NF_{max} <= 10 dB
- Receiver sensitivity = -85 dBm
- Dynamic Range = 60 dB

Receiver System Level Diagram



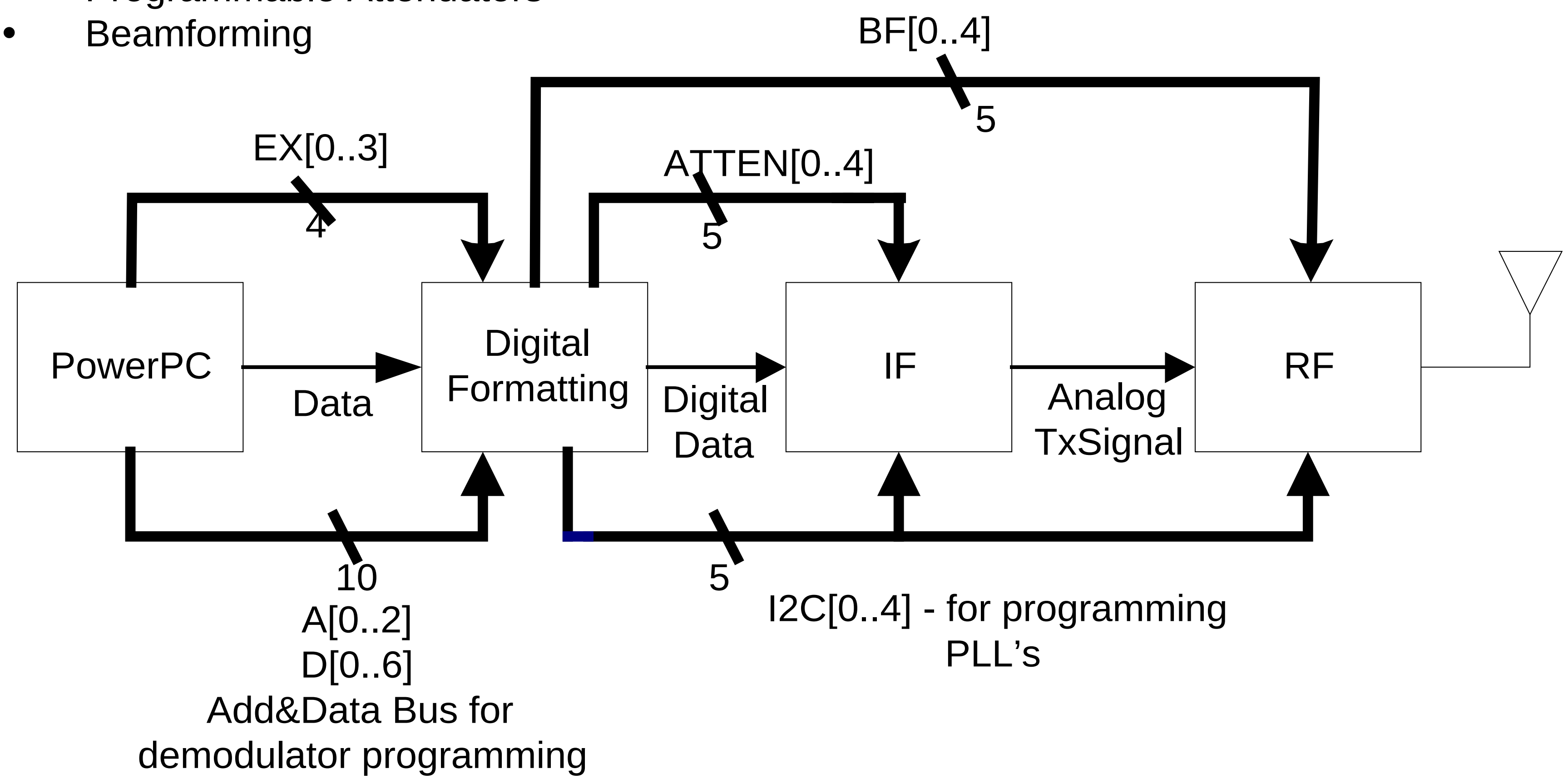
Benefits to Digital Demodulation

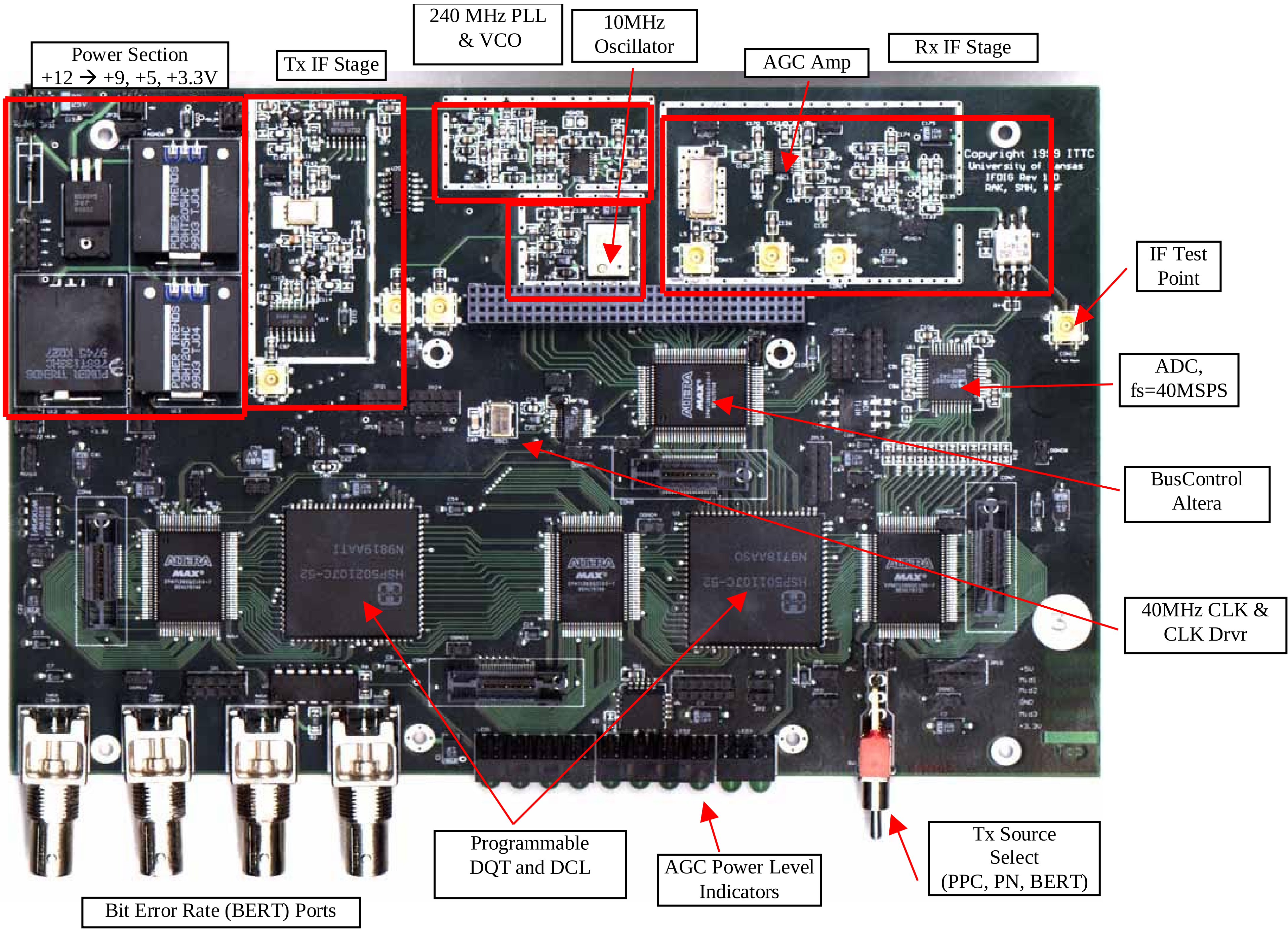
- No need for tuning filters
- Can Construct Linear Phase Filters
- Flexible BW selection
- Multiple Modulation Formats can be supported
- System can be simulated “exactly”
- Multiple Radio “Personalities” as easy as setting up tables

Control Bus Architecture

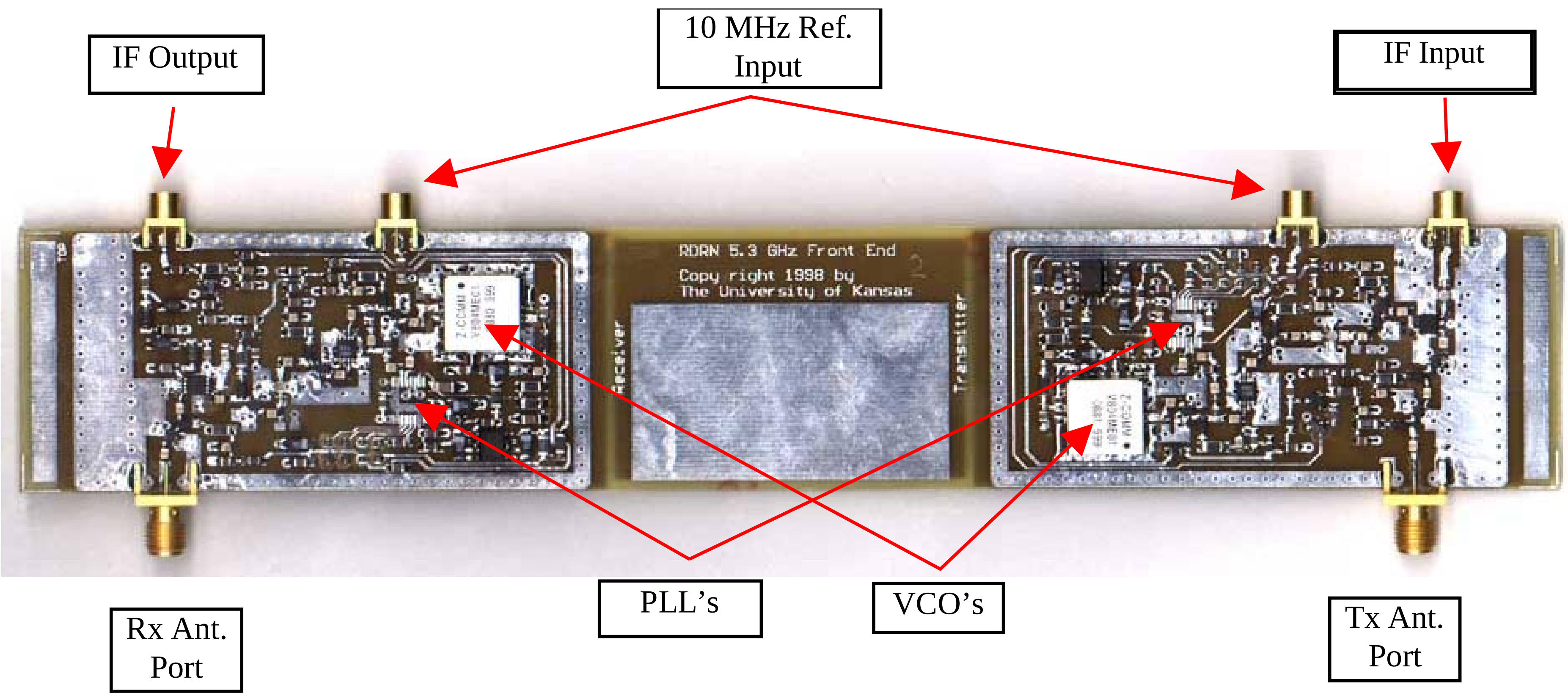
Control Bus is a serial bus controlling:

- PLL programming
- Programmable Attenuators
- Beamforming




Power Section
+12 → +9, +5, +3.3V
Tx IF Stage
240 MHz PLL & VCO
10MHz Oscillator
AGC Amp
Rx IF Stage
IF Test Point
ADC, fs=40MSPS
BusControl Altera
40MHz CLK & CLK Drvr
Tx Source Select (PPC, PN, BERT)
AGC Power Level Indicators
Programmable DQT and DCL
Bit Error Rate (BERT) Ports
Copyright 1999 ITTC
University of Kansas
IFDIG Rev 1.0
RAK, SMH, KMF

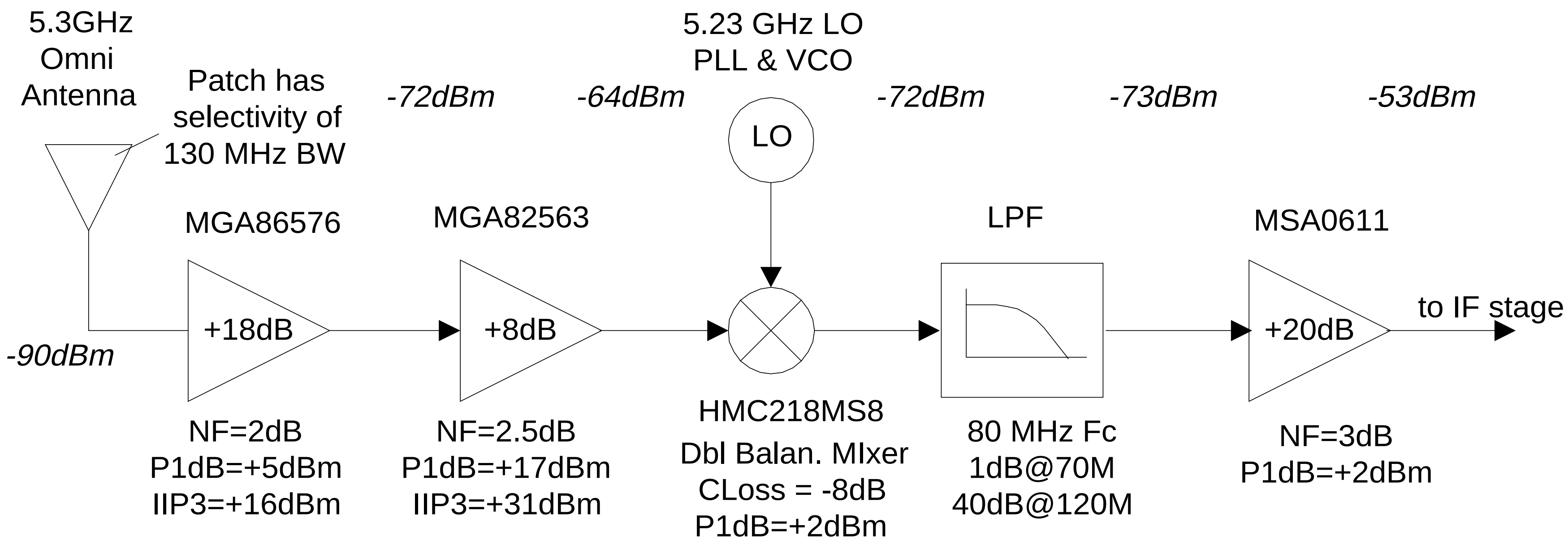
5.3 GHz Modular RF Front End



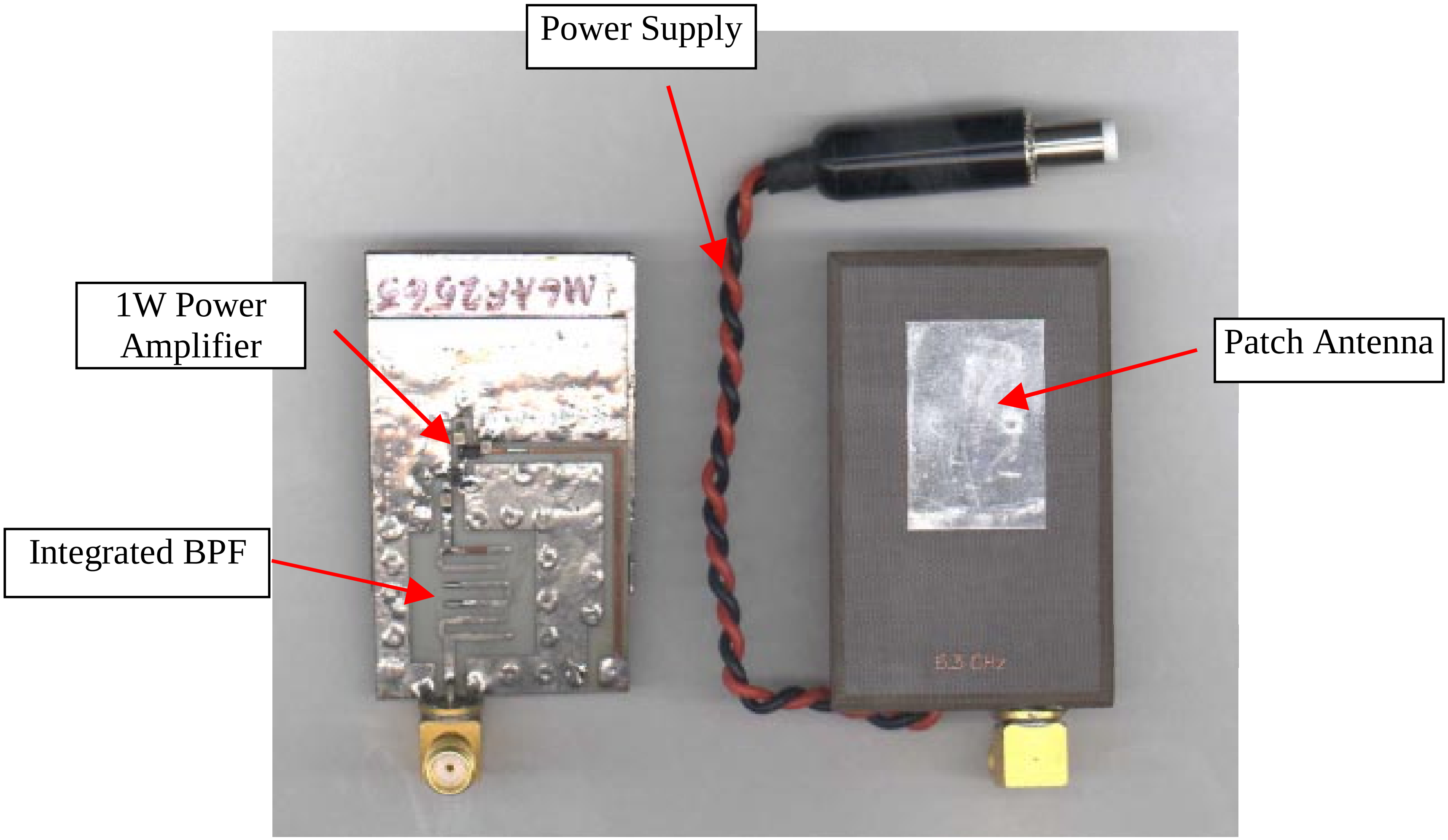
Average Power Requirements

	Voltage [V]	Current [A]	Power Needed [W]
Regulators (alone)	12	40m	0.480
Analog Sections	12	120m	1.44
9V sections	12	190m	2.28
Total for Analog Sections	12	350m	4.2
5V Digital. (Quiescent Only)	5V	1.6	8
3.3V Digital. Powering only Altera's (Quiescent Only)	3V	333m	1
Total Power for Digital			9 W
Total Power PPC (Quiescent), datasheet claims 8W			5 W
Total Power	**12 V**	**1.52 A**	**18.2 W**

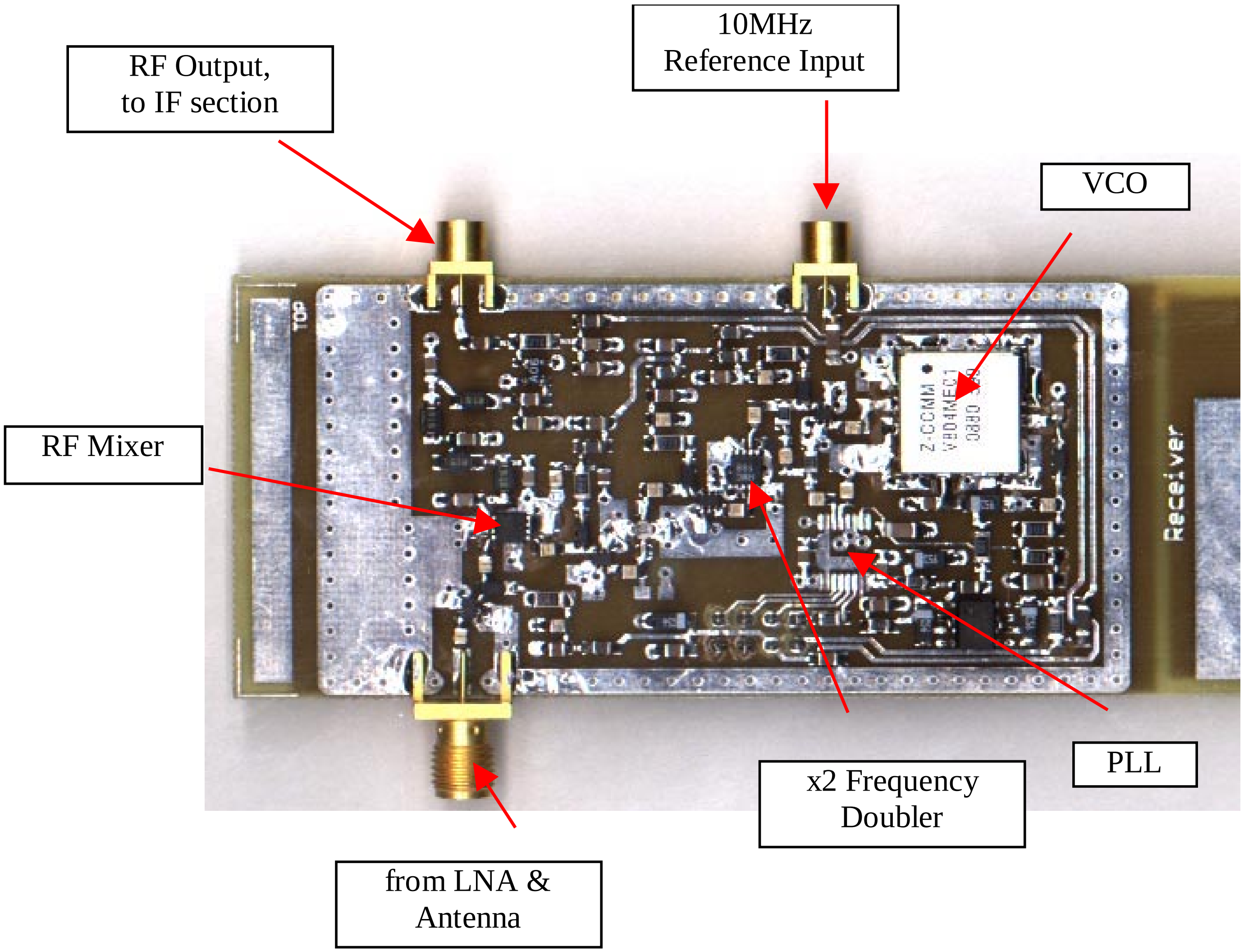
Receiver Implementation



Patch Antenna Sub-Assembly



View of RF Receiver

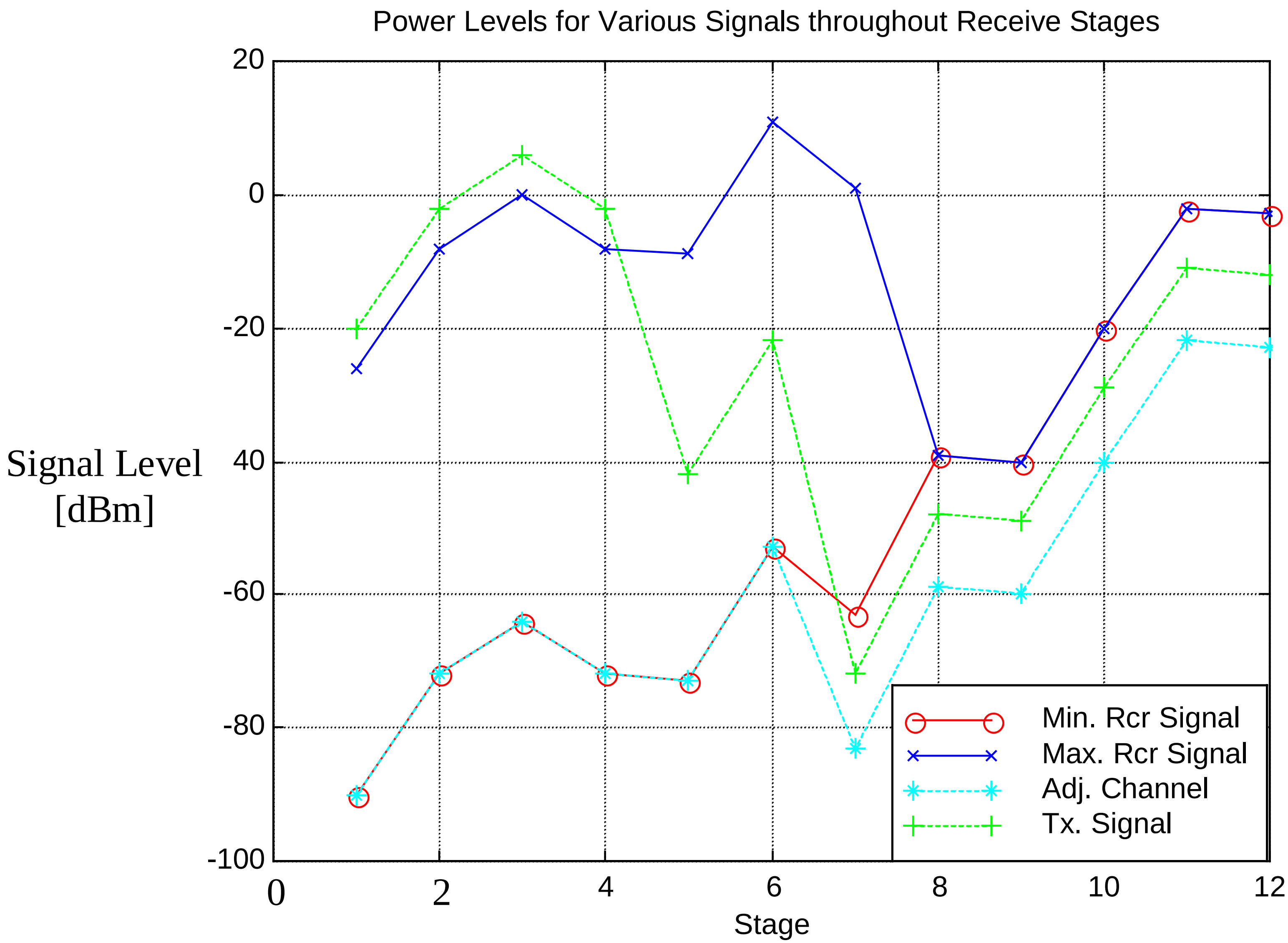


Input Signal Levels Throughout Receive Chain

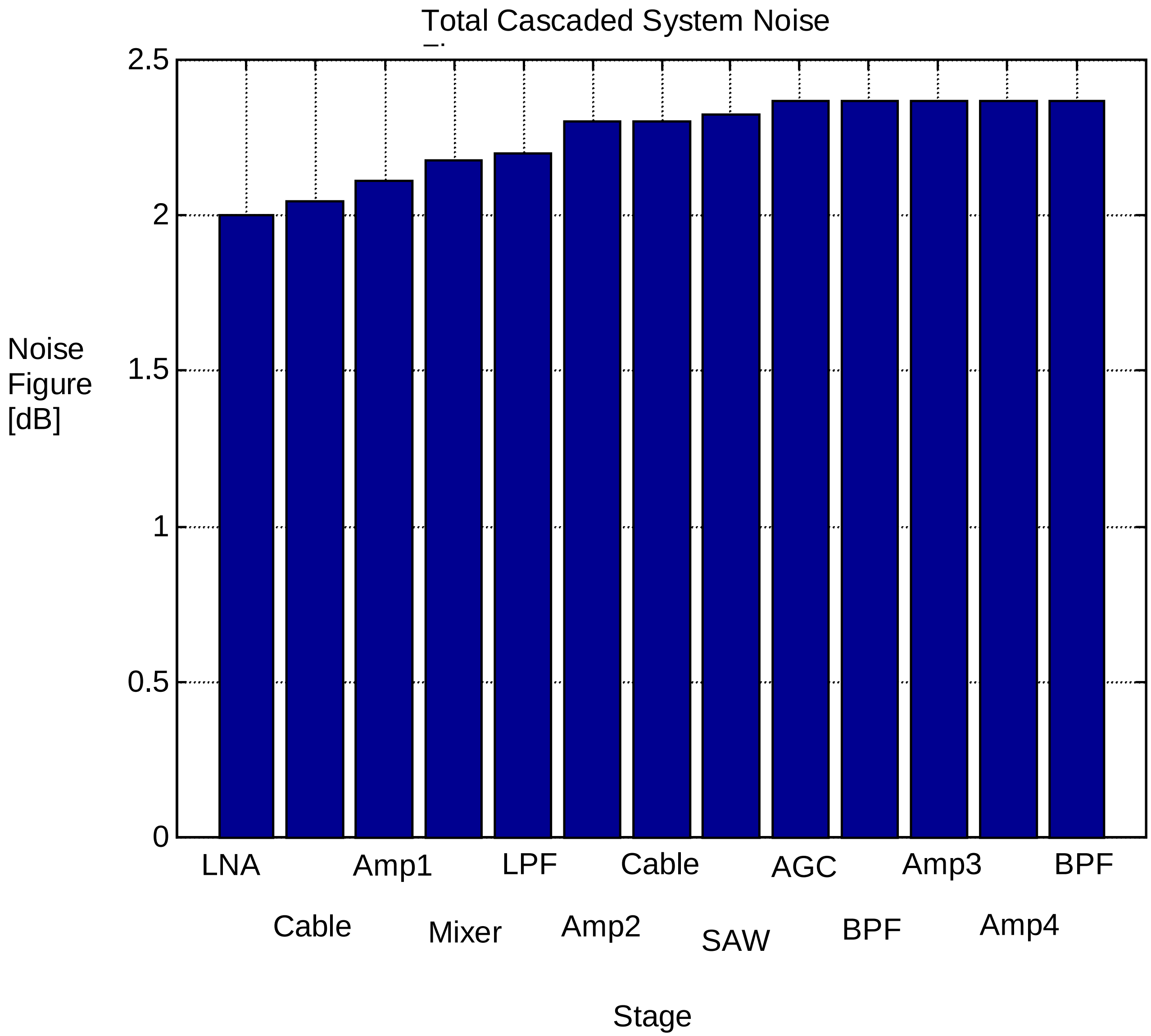
Stages within Receive Chain – all Input Power Levels in dBm

P_{TX} @ 1W	LNA	82563	Mixer	LPF	0611	SAW	AGC	BPF	0611	2011	BPF	ADC
Desired Signal – Min	-90	-72	-64	-72	-73	-53	-63 (+24)	-39	-40	-20	-2	-3
Desired Signal -- Max.	-26	-8	0	-8	-9	+11	+1 (-40)	“	“	“	“	“
Adjacent Channel at 10MHz Offset	-90	-72	-64	-72	-73	-53	-83 (+24)	-59	-60	-40	-22	-23
	-26	-8	0	-8	-9	+11	-19 (-40)	-59	-60	-40	-22	-23
Tx Signal 50M offset, 1W, 50dB* isolation	-20	-2*	+6	-2 (-40)	-42	-22 (-50)	-72 (+24)	-48	-49	-29	-11	-12
							-72 (-40)	-112	-113	-93	-75	-76

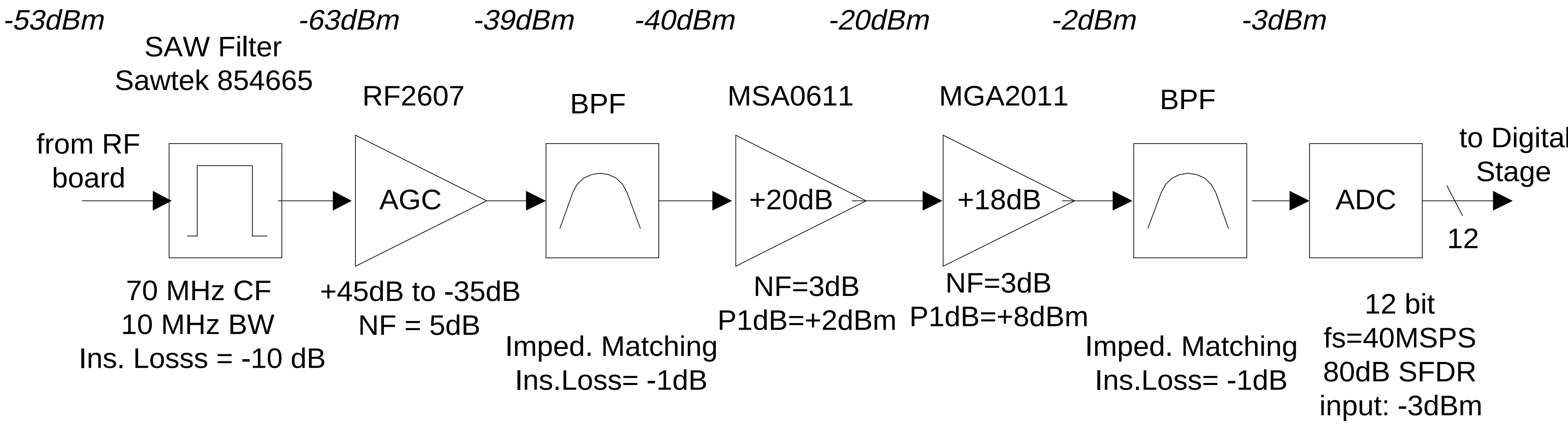
Receive Signal Levels



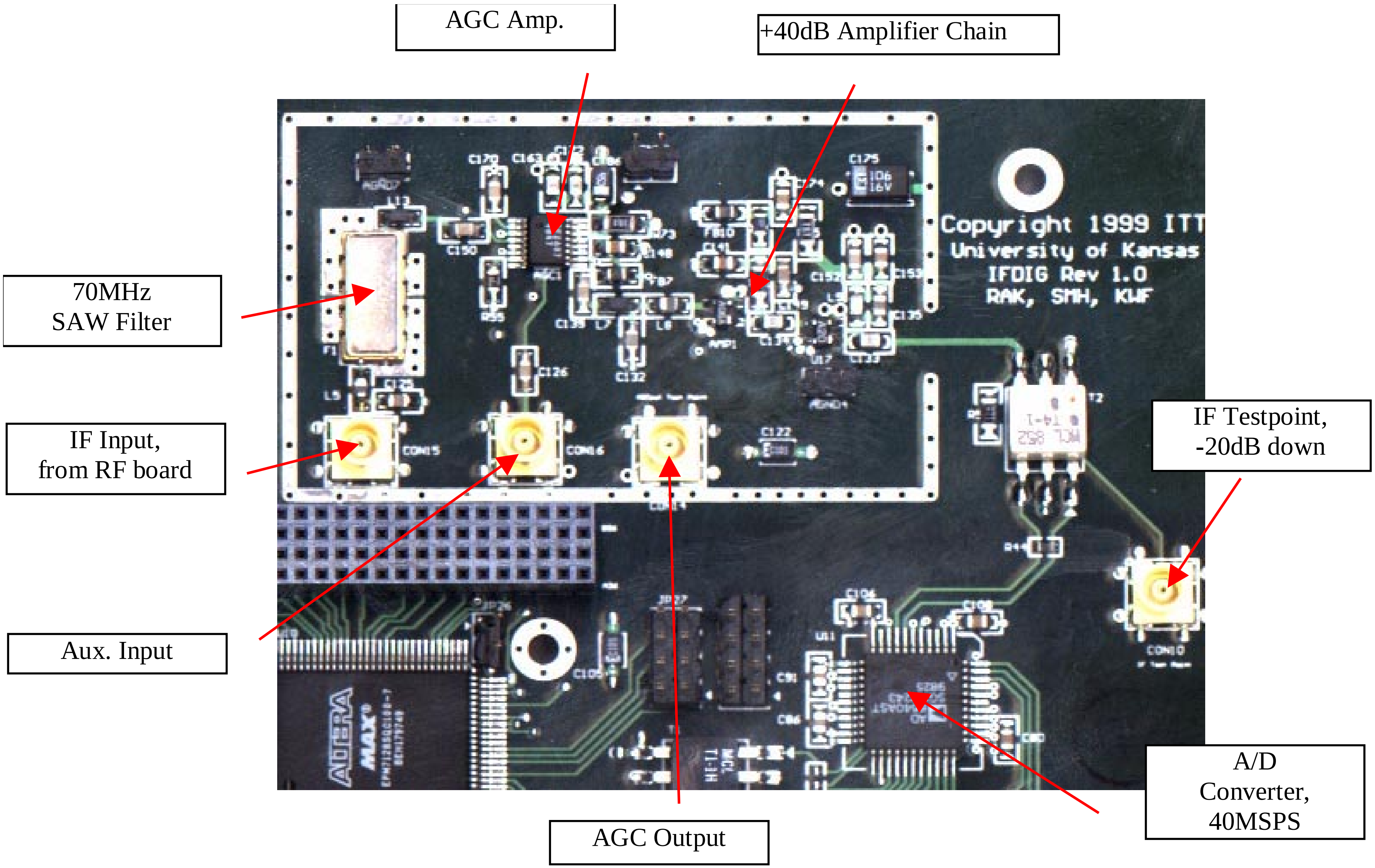
System Noise Figure



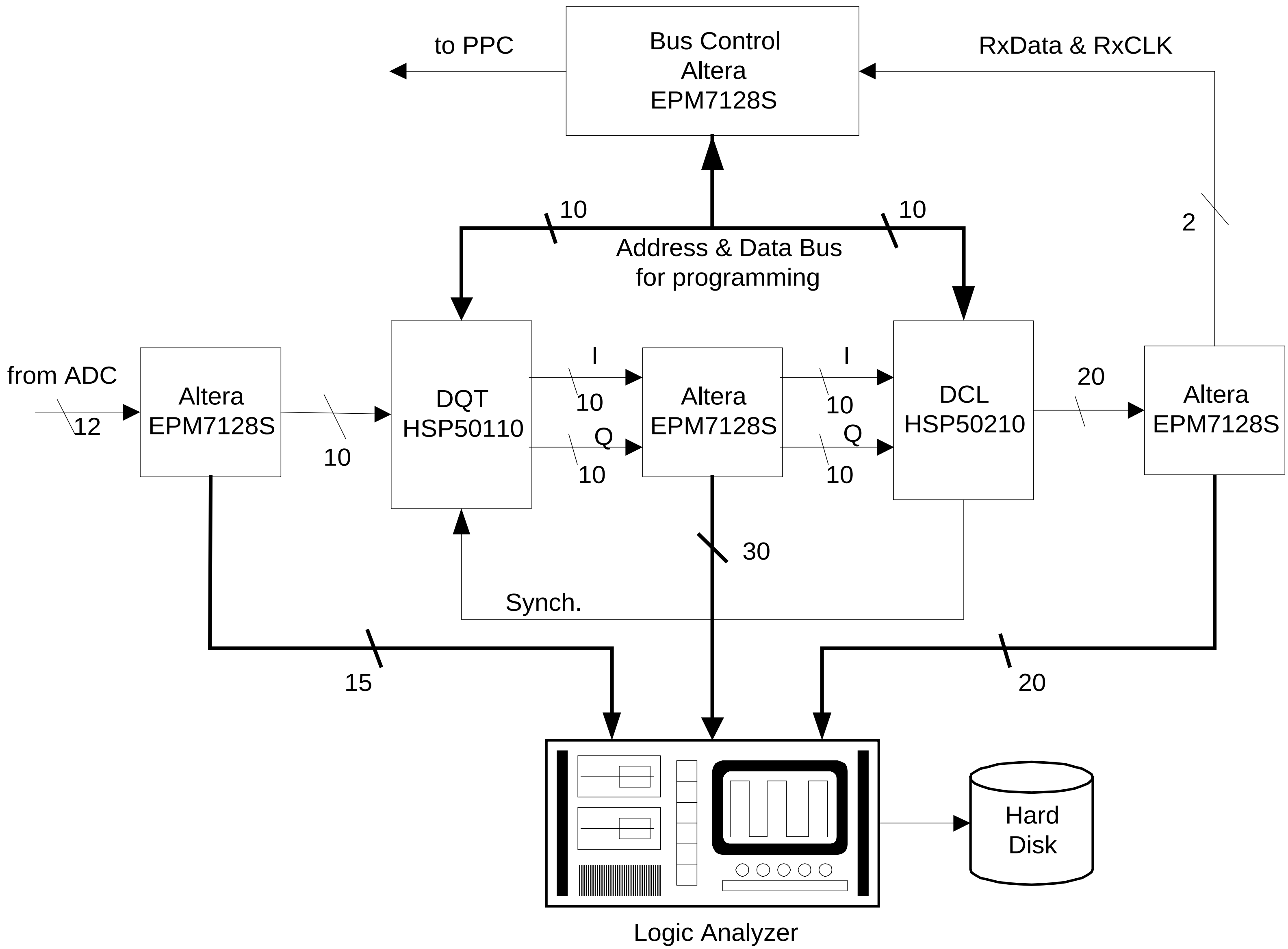
Receiver, IF to ADC



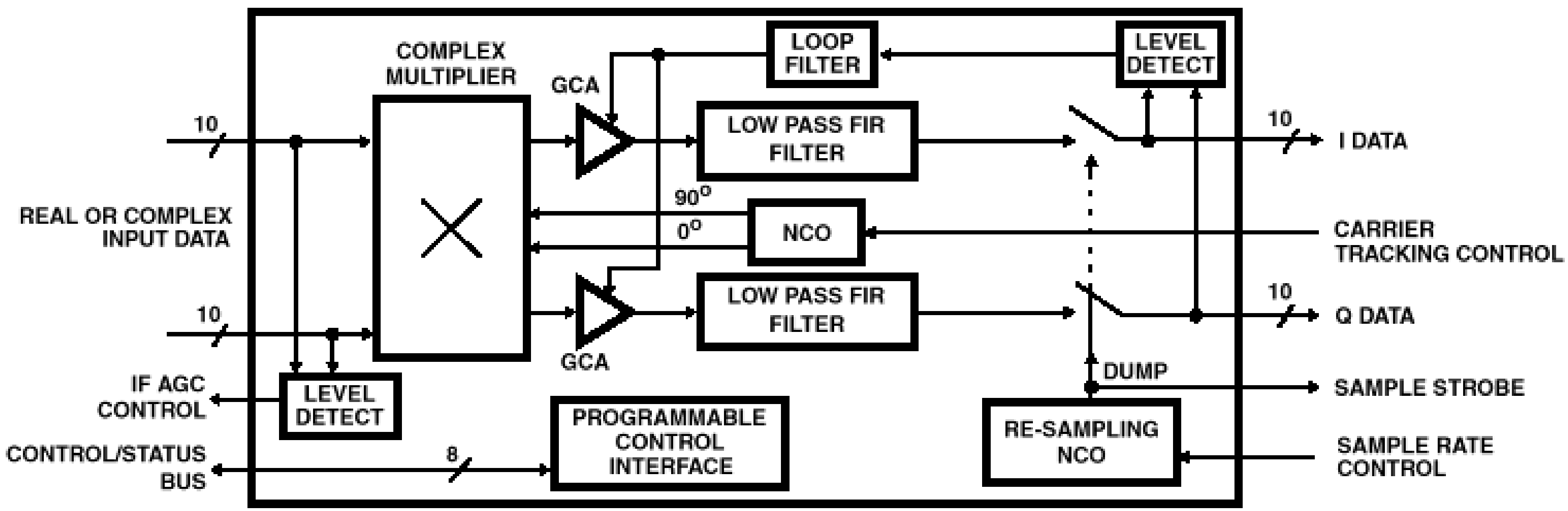
Receiver, IF to ADC



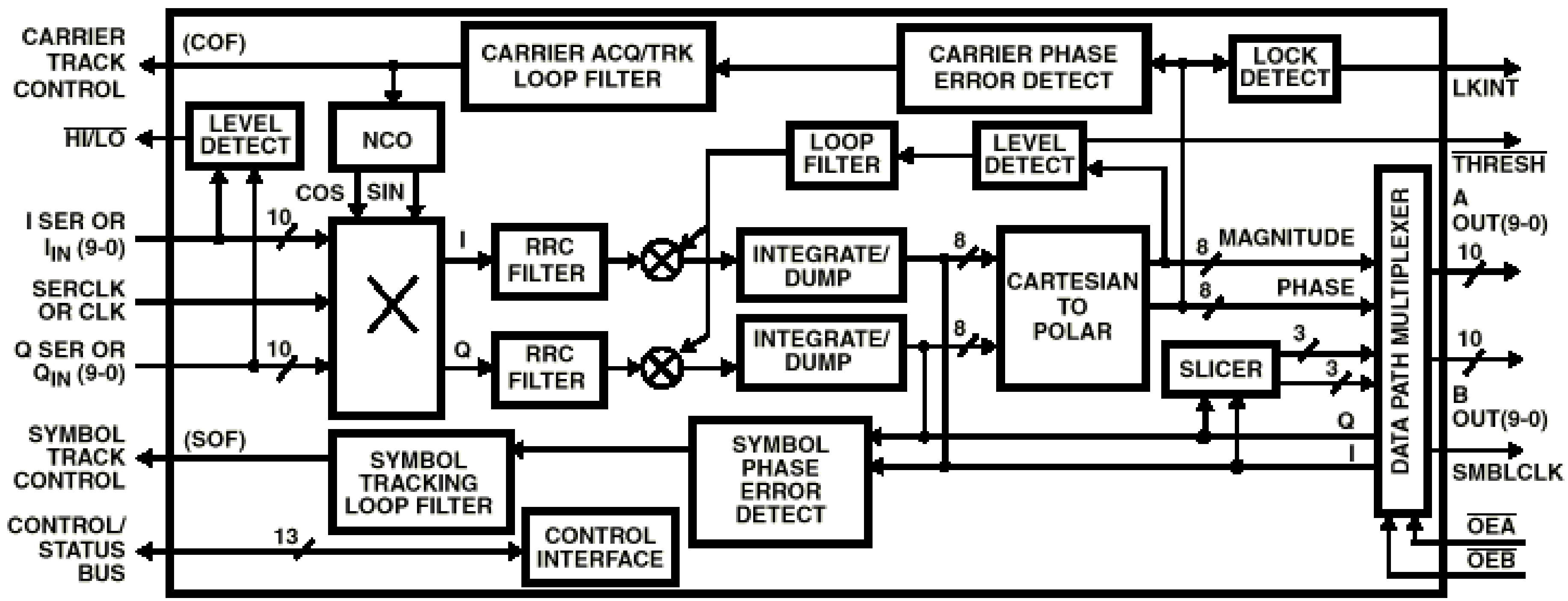
Digital Section



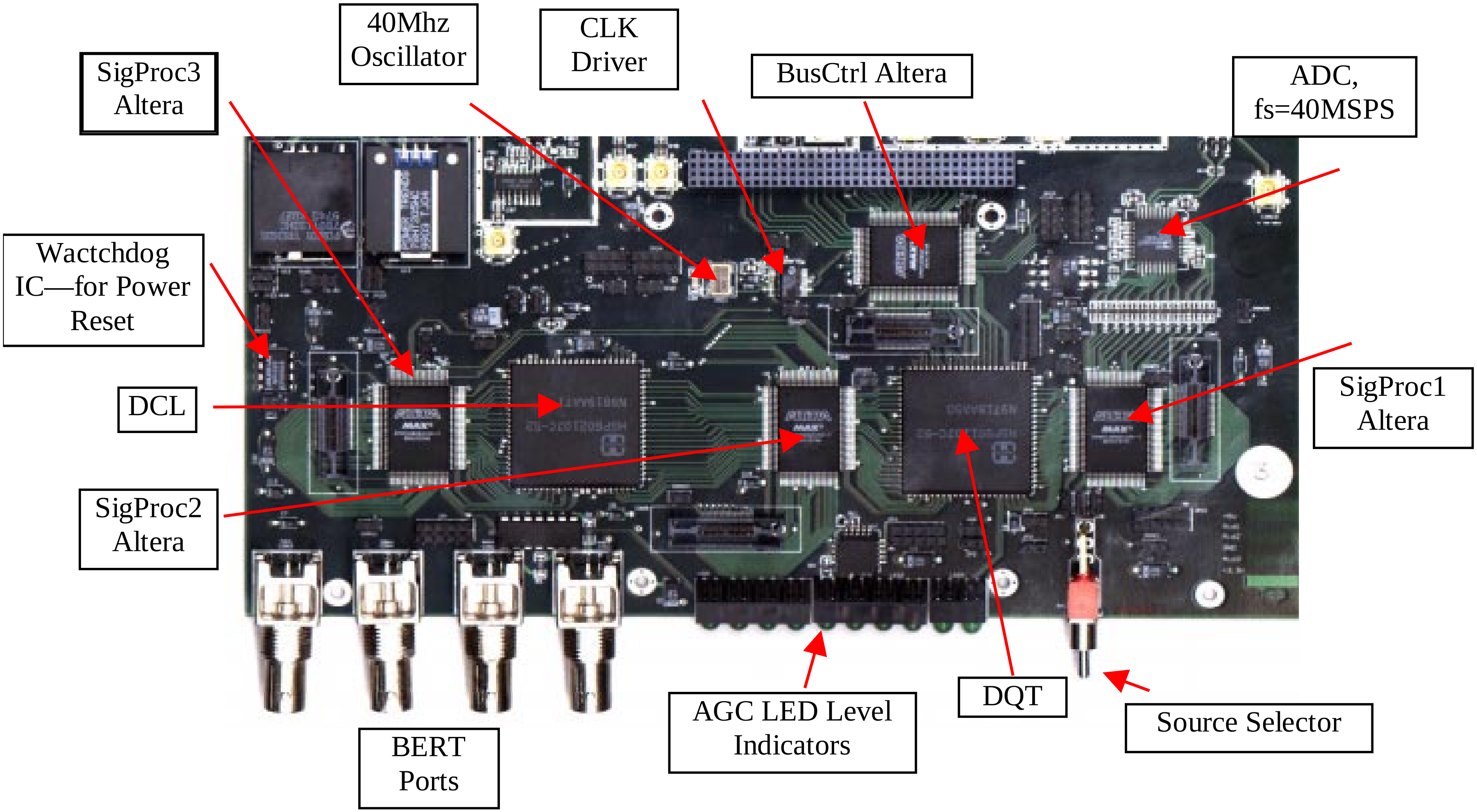
Digital Quadrature Tuner



Digital Costas Loop

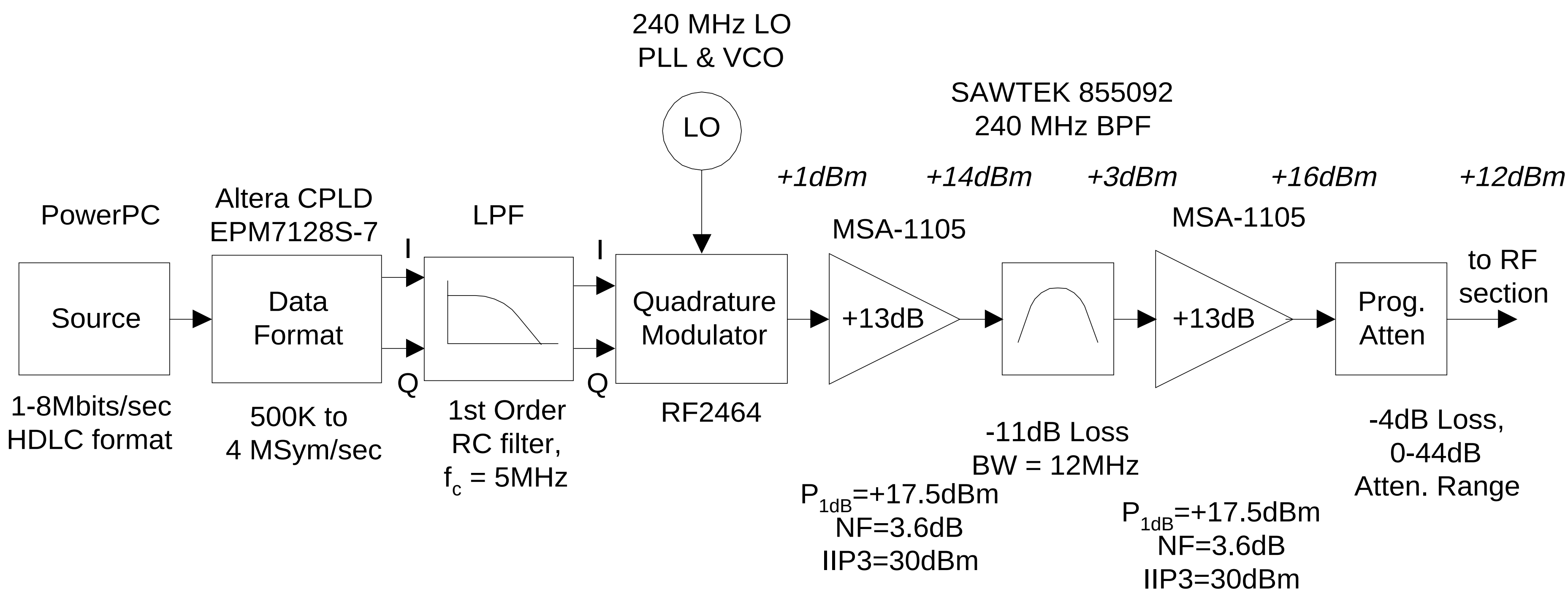


Digital Section

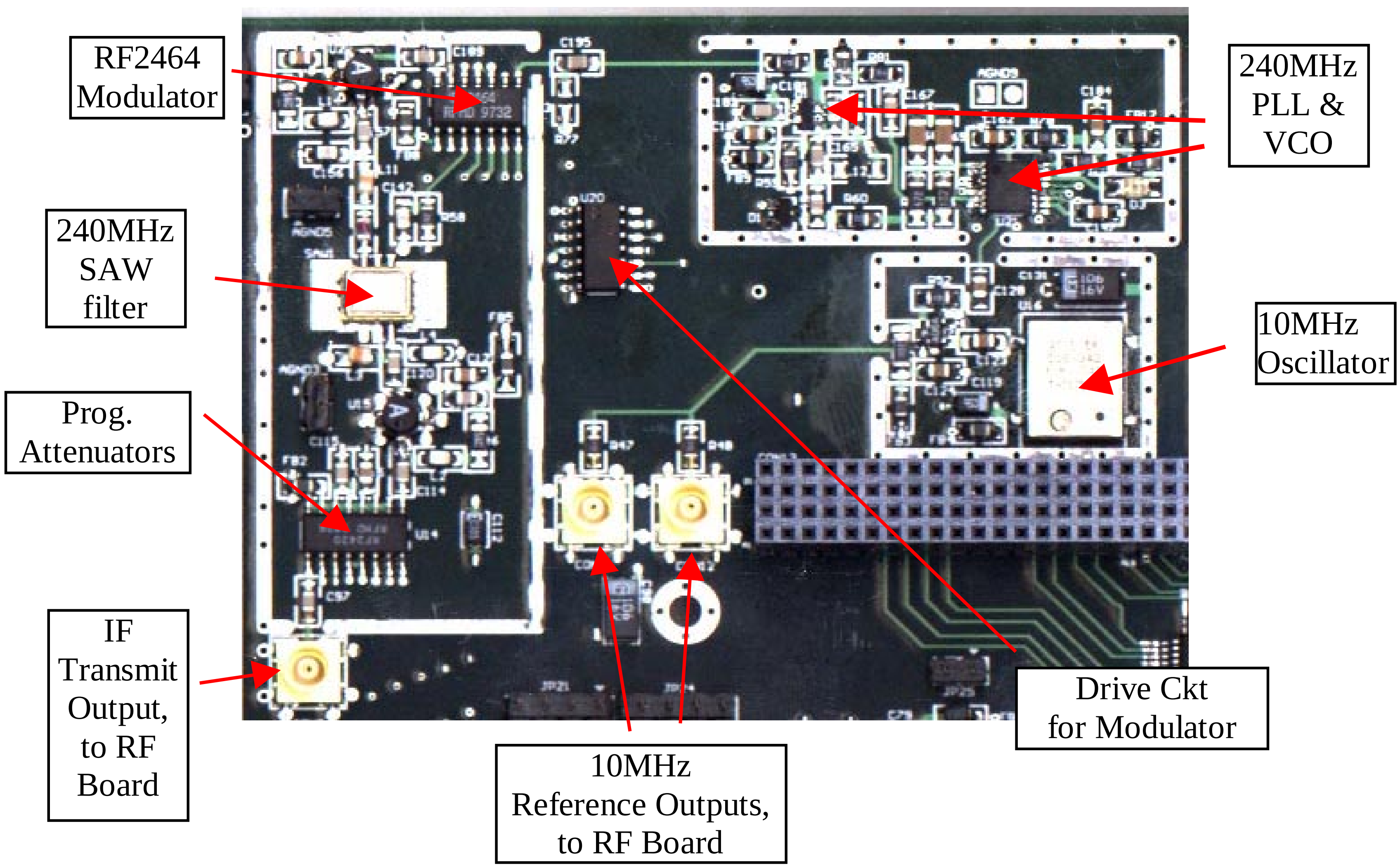


Transmitter Implementation

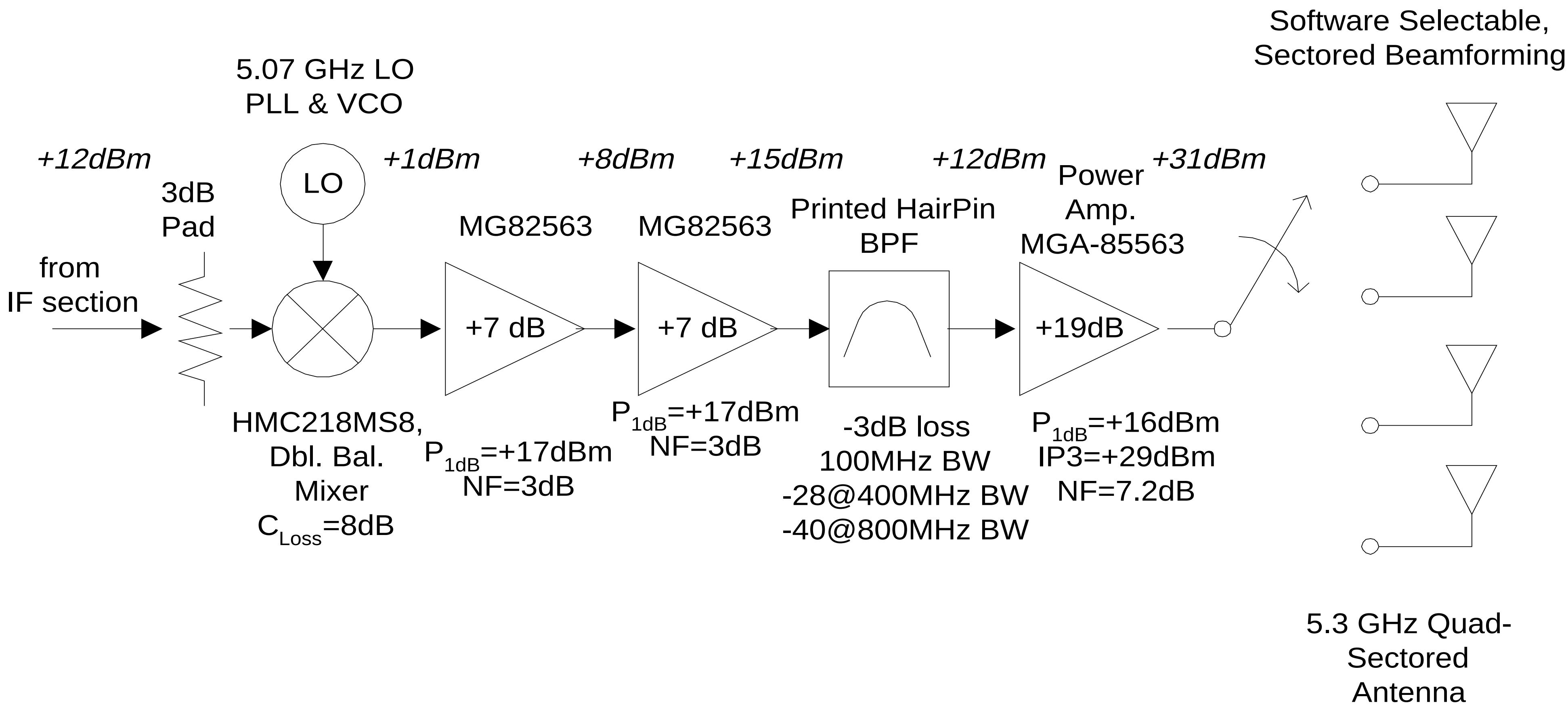
(Baseband to IF)



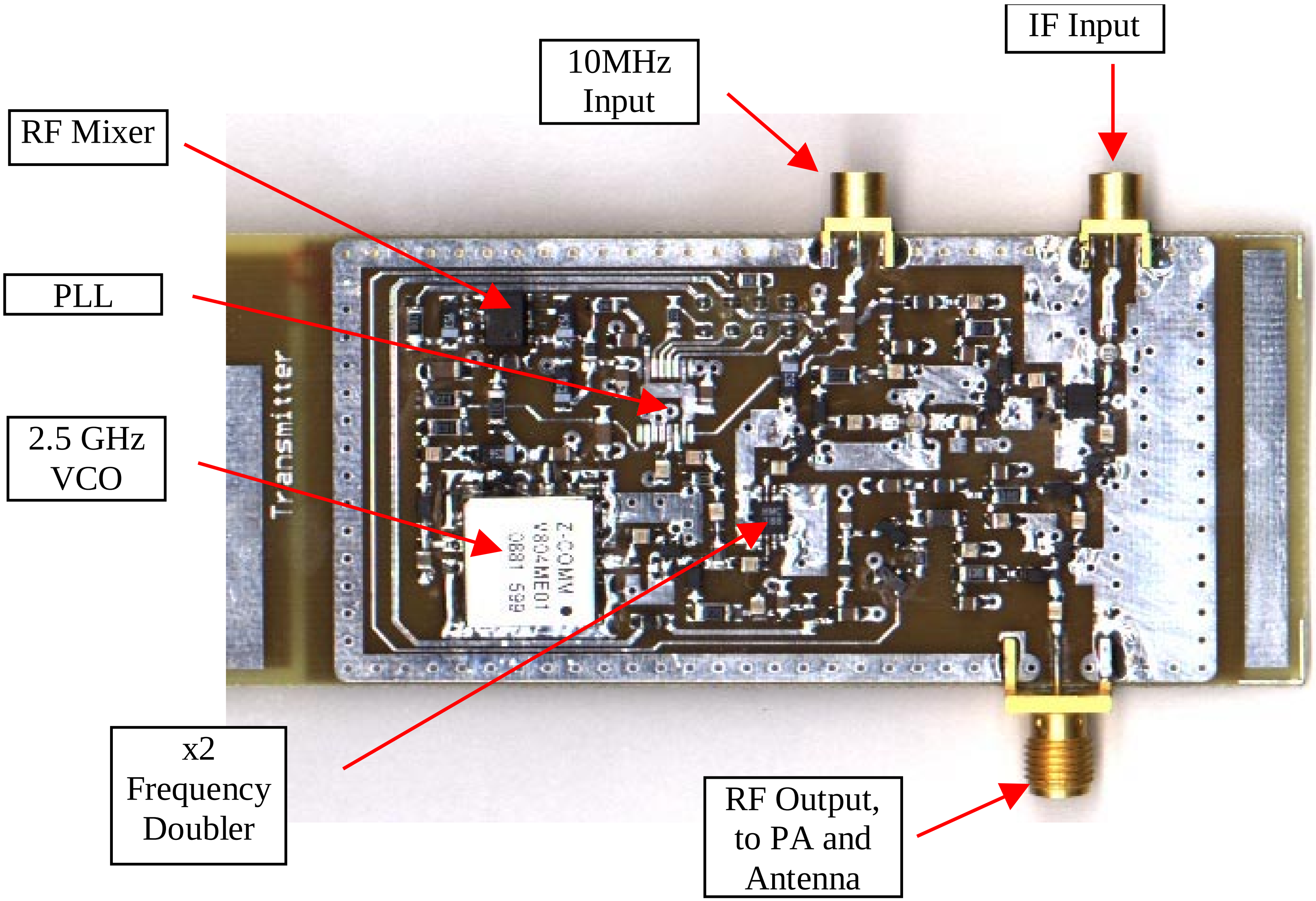
Close Up View of Tx IF Stage



Transmit RF Section



Transmit RF


IF Input
10MHz Input
RF Mixer
PLL
2.5 GHz VCO
x2 Frequency Doubler
RF Output, to PA and Antenna
Transmitter

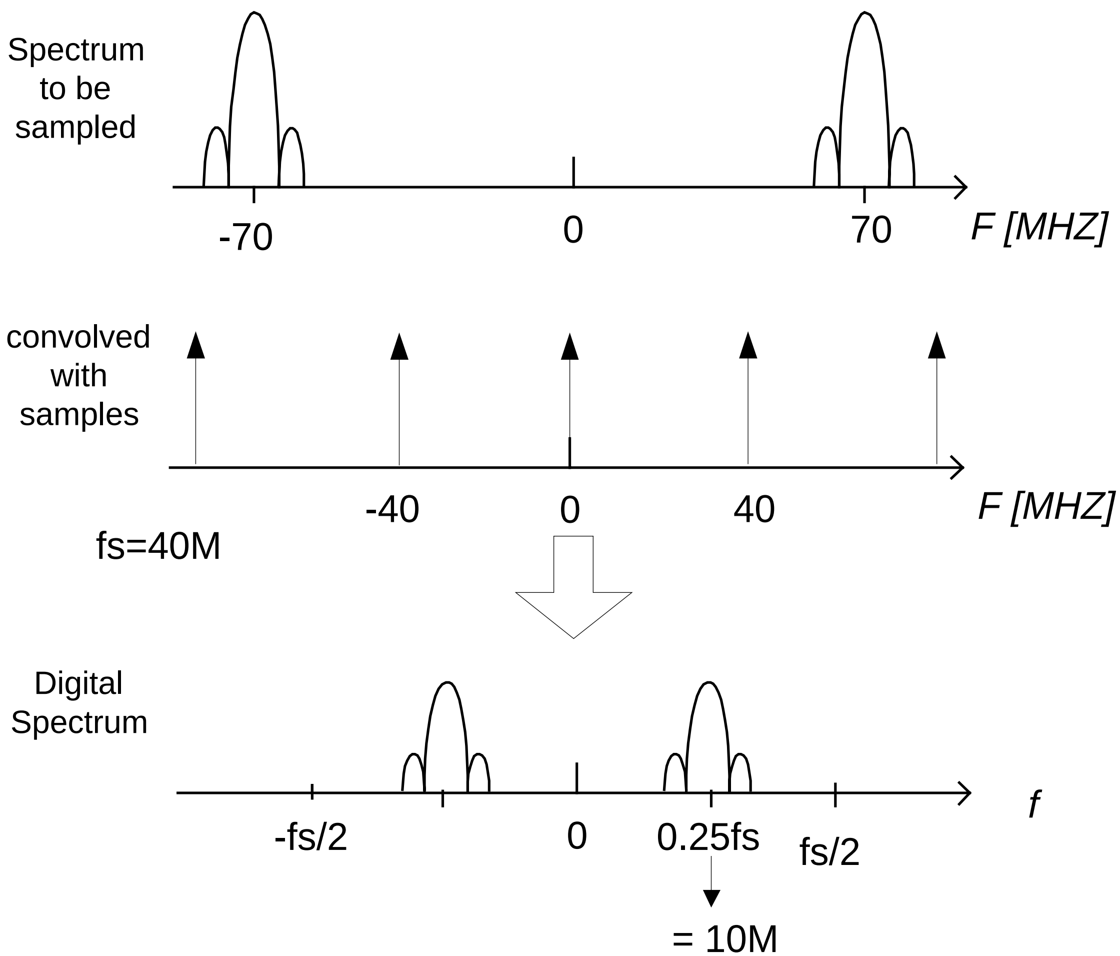
Summary

- Software controlled radio with modular RF front ends for use in channel estimation.
- High-Speed (up to 8 Mbps) wireless radio which is capable of physical layer and data-link layer adaptability.

Future Work

- Use this radio "platform" to develop protocols and algorithms to control the physical & data-link layer.
- Real time channel estimation and the use of these parameters in the above adaptation algorithms.

Sub-Sampling



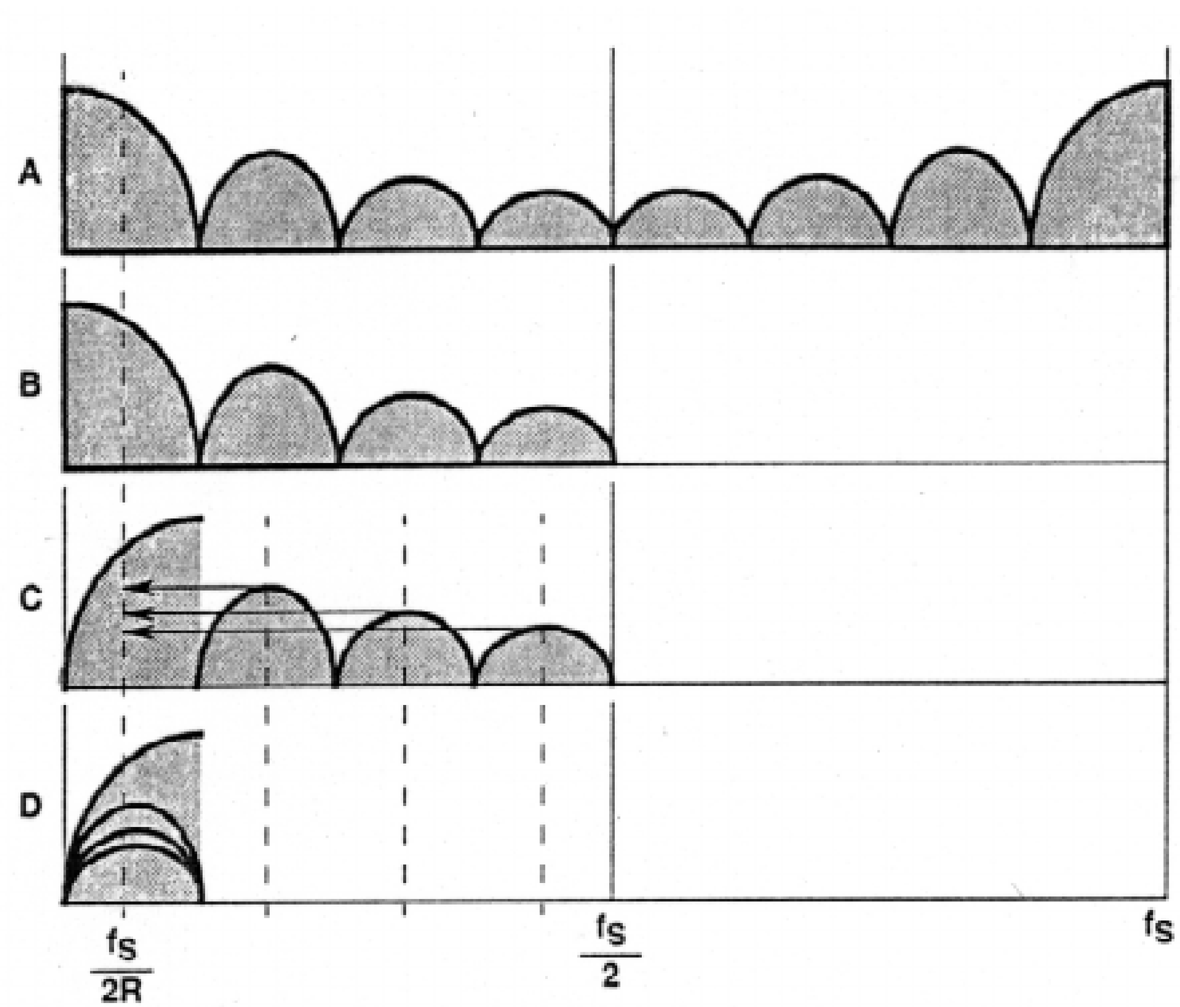
How to choose f_s ,

$$\frac{2f_H}{k+1} < f_s < \frac{2f_L}{k}$$

where the maximum value of k is :

$$k < \frac{f_L}{f_H - f_L}$$

Decimation



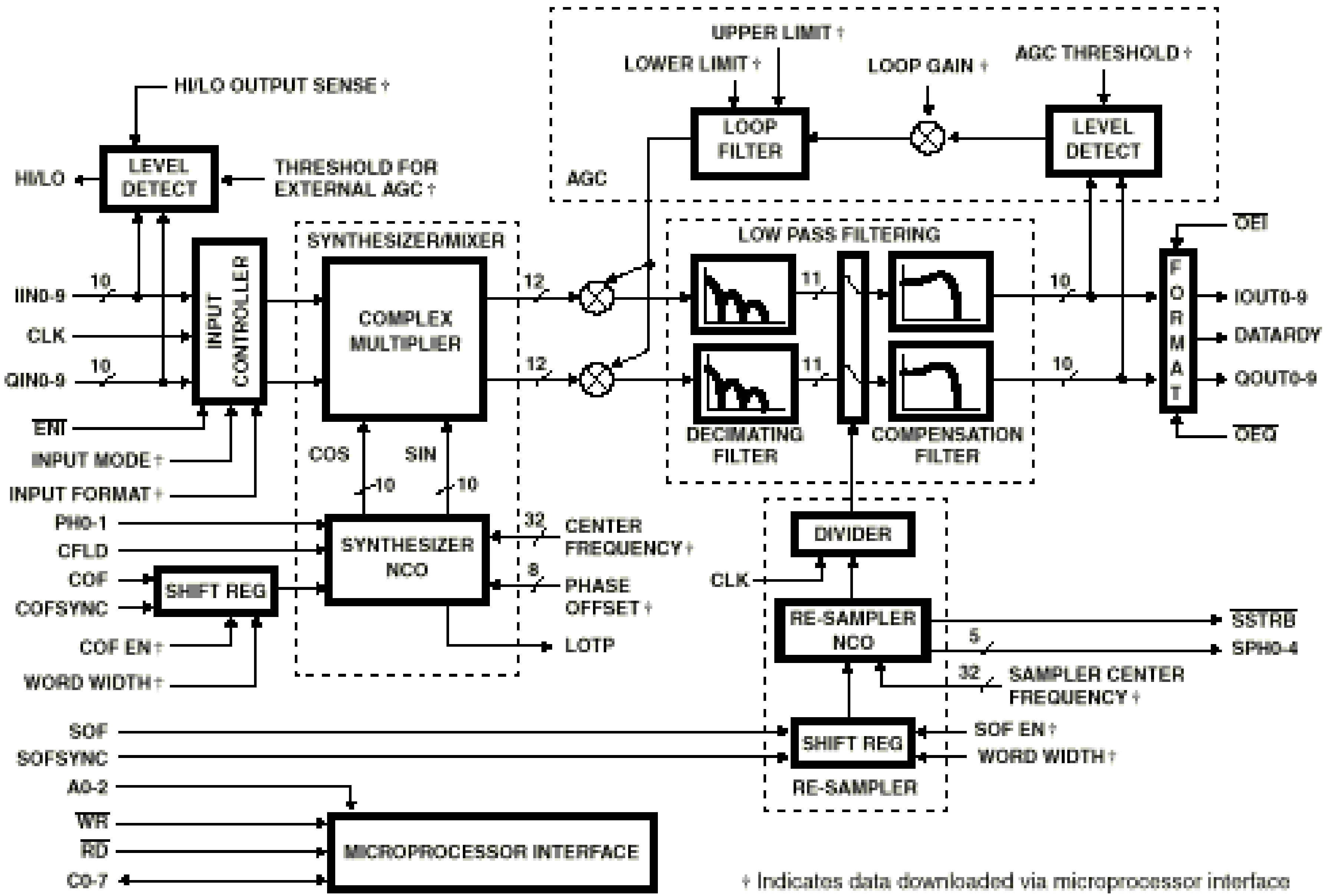
Apparent useable BW

Can Only see up to $\frac{f_s}{2}$

Decimation creates new "folding frequency"

Noise and possible interferers aliased into passband?--How much attenuation? Use Alias Profile

Digital Quadrature Tuner, detail



† Indicates data downloaded via microprocessor interface

Digital Costas Loop, detail