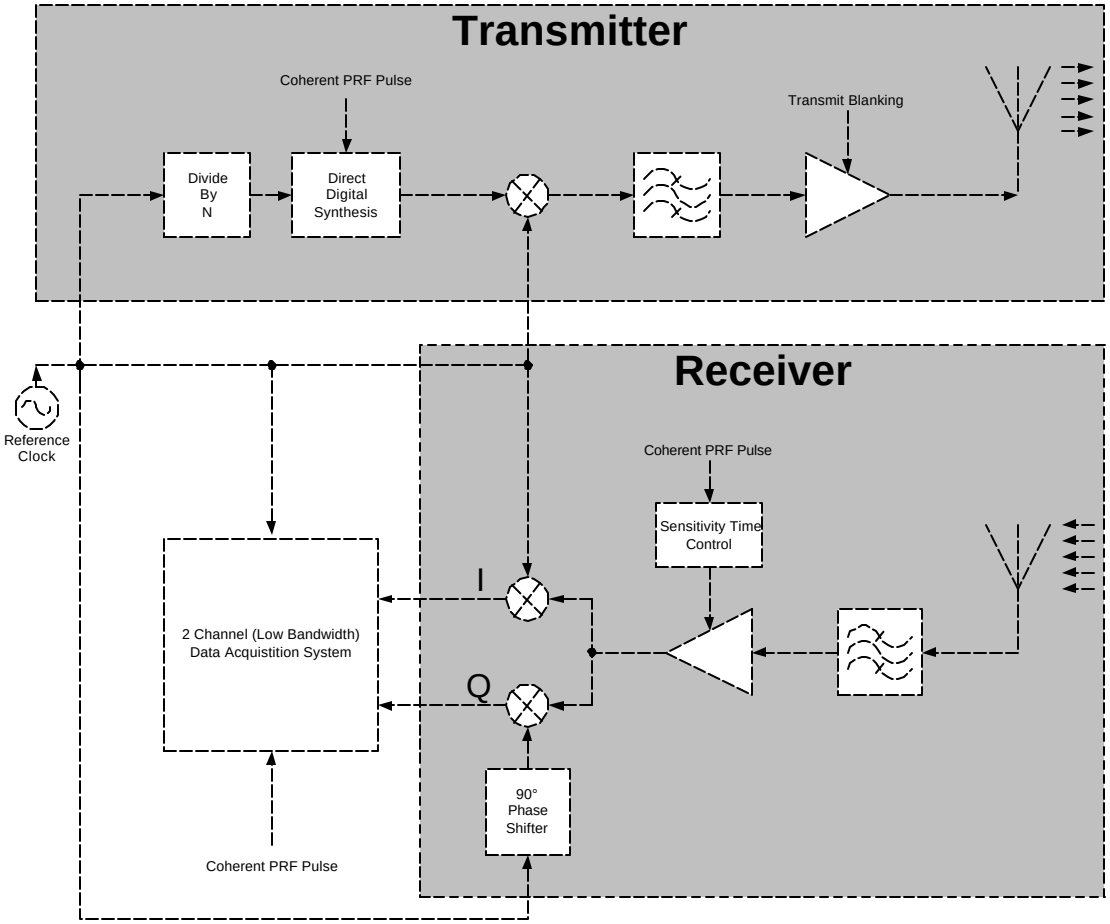
Design and Development of a One Gigasample per Second Radar Data Acquisition System

By Ryan Eakin

October 29, 2001

System Motivation/Background

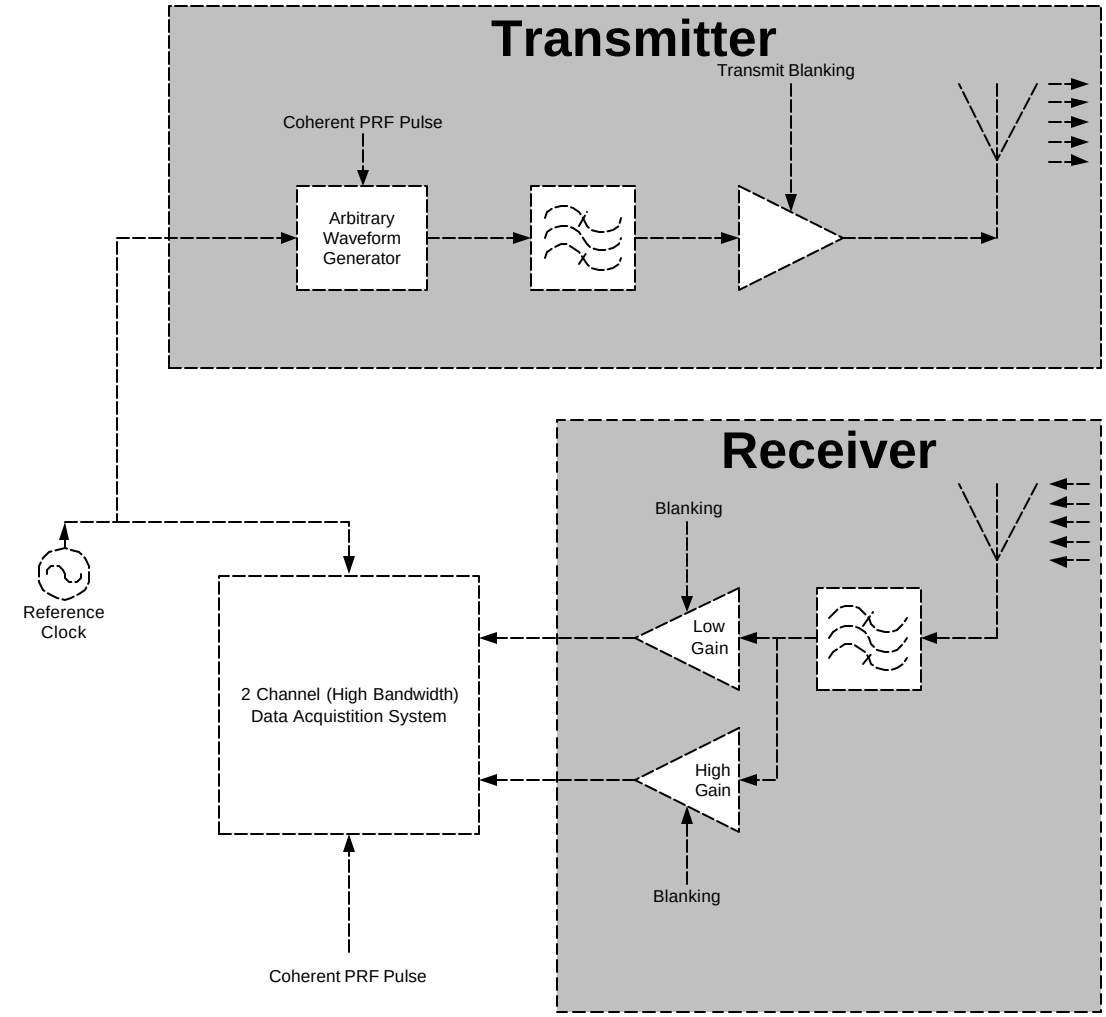
Traditional Coherent Radar



Traditional Radar Problems

- Analog components cannot be precisely characterized and are non-ideal
  - Characteristics change with temperature
- Analog components add:
  - noise
  - Harmonics
- All of these result in degraded system performance

Digital RF Radar System

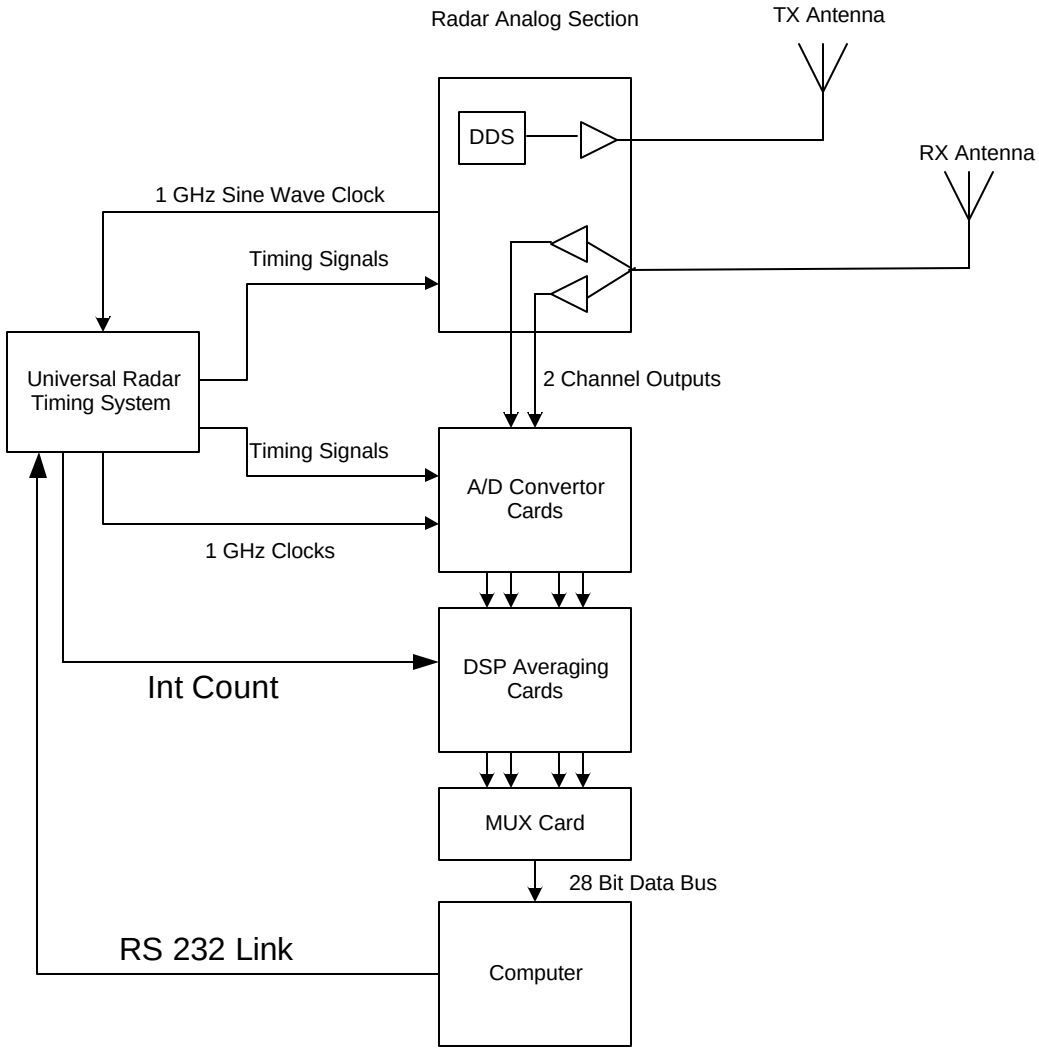


Advantages of Digital RF Radar

- All mixers are eliminated from the system
- Increased ADC bandwidth eliminates IQ downconversion
  - Allows STC to be replaced with 2 fixed gain amps
- Amplifiers/antennas/filters can be compensated for digitally for a more ideal system response

Acquisition System Design

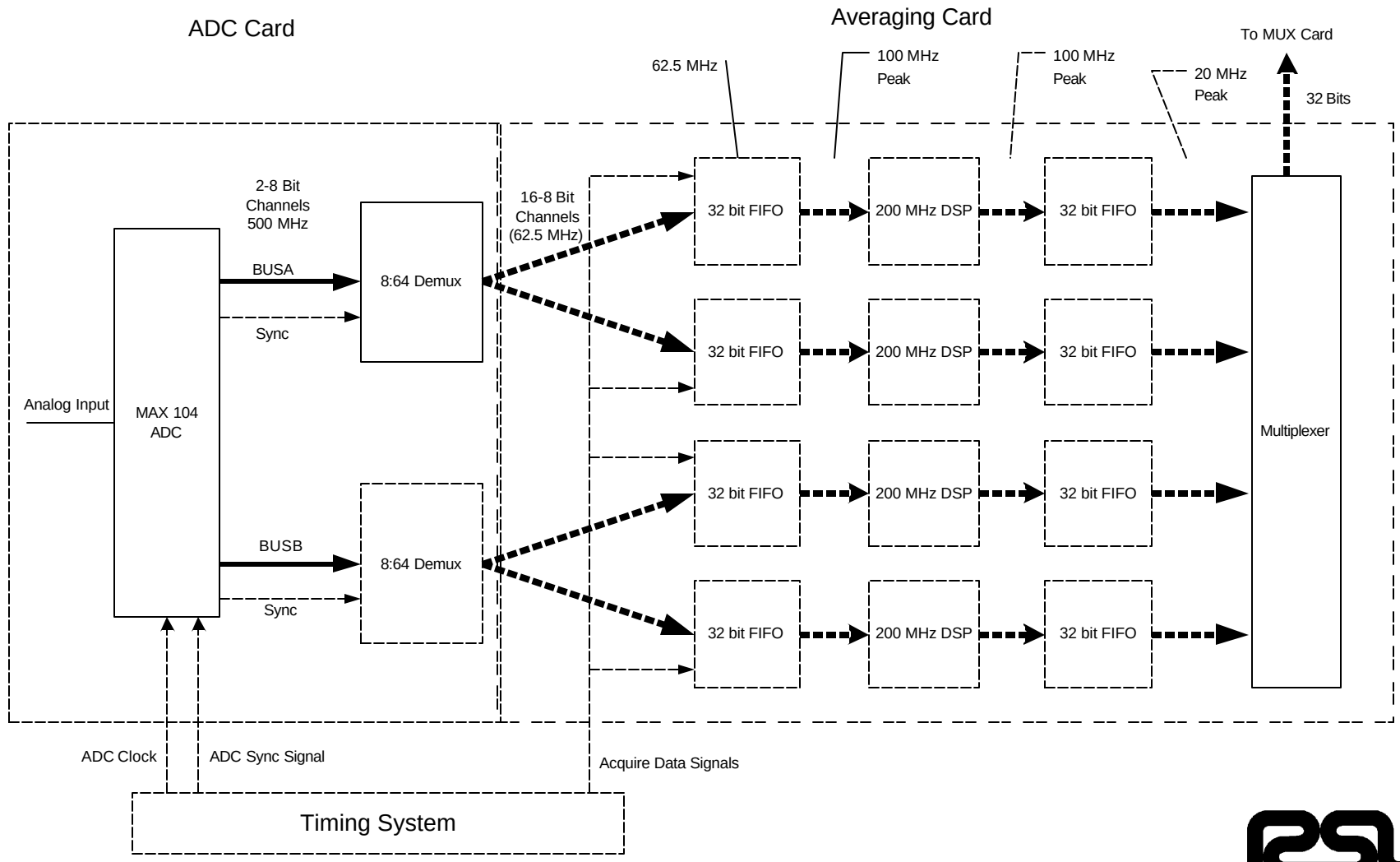
RSL Digital RF System Block Diagram



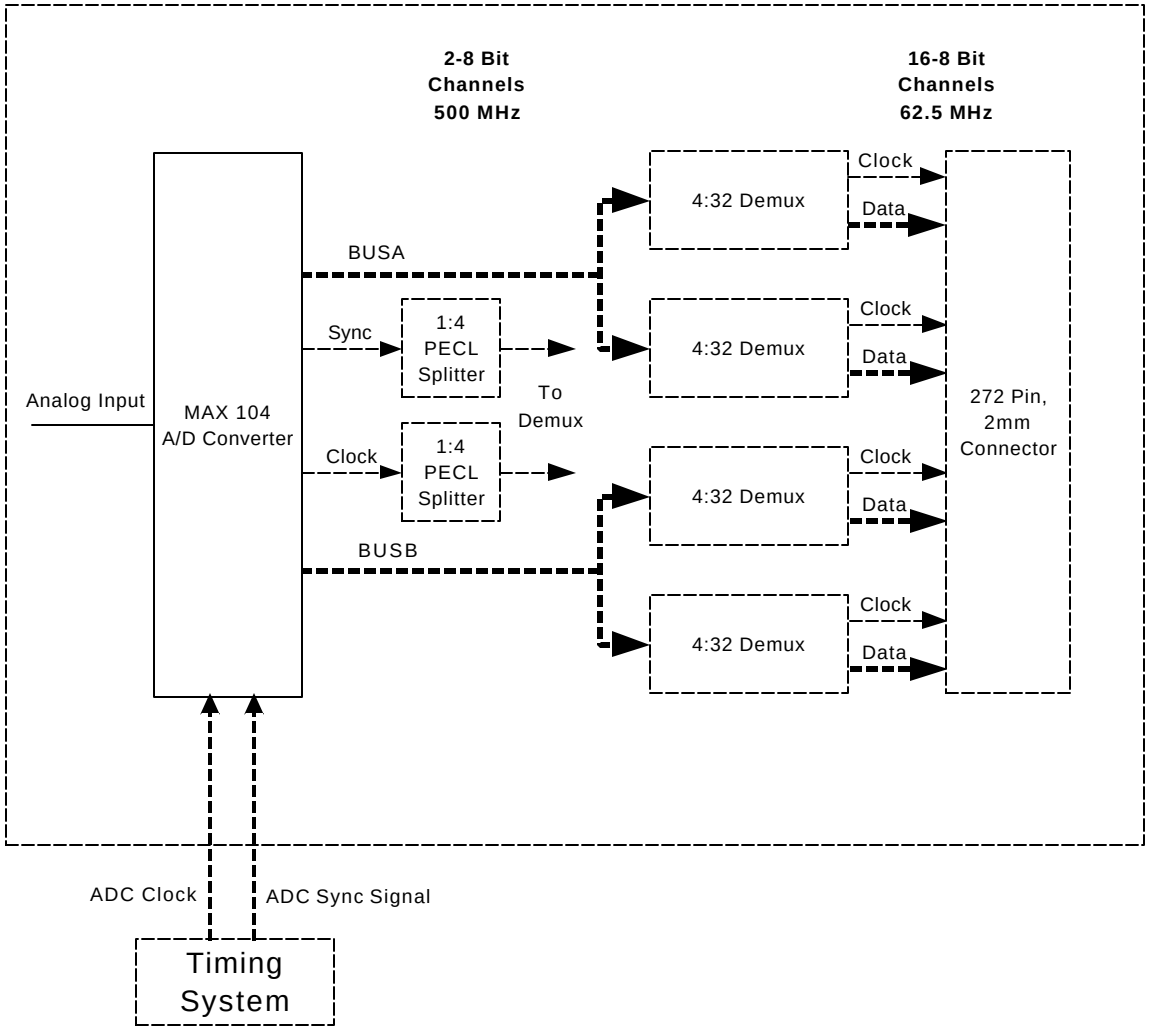
Acquisition System Specifications

- 4 8-bit channels
- 1 GS/s maximum sampling rate
- 2.2 GHz analog bandwidth to allow direct digitization of RF signals
- Input clock 1 GHz sine wave drive
- Performs coherent averaging adjustable from 1 to 65,535

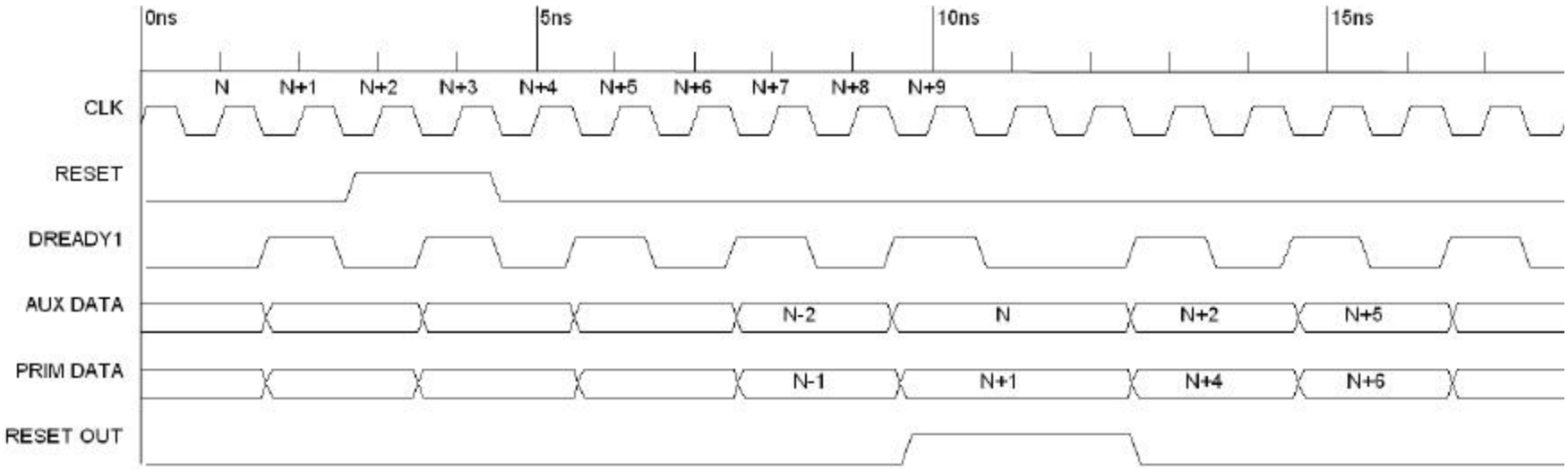
A/D Channel Overview



ADC Card Detailed Diagram



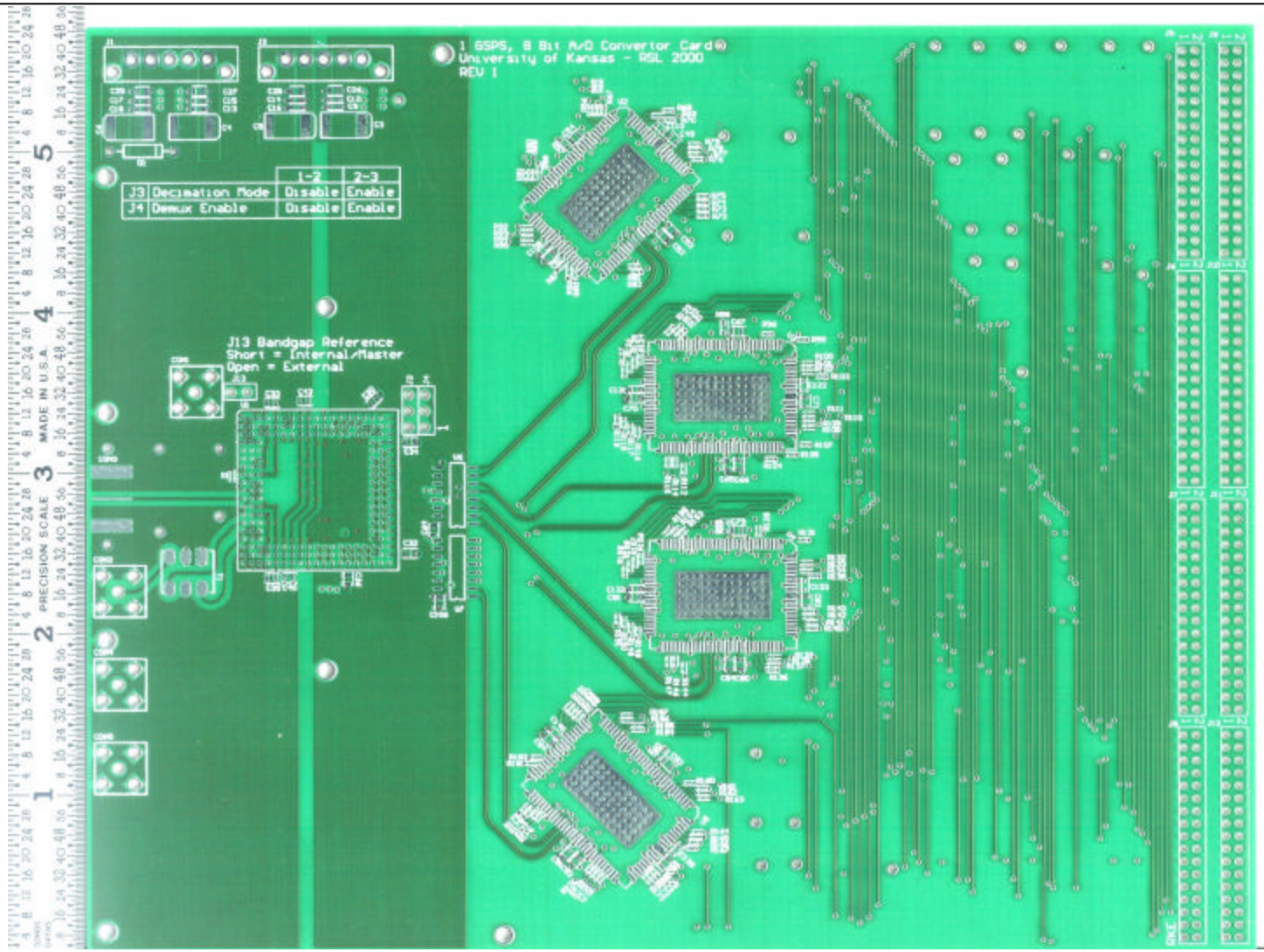
ADC Synchronization for Coherency



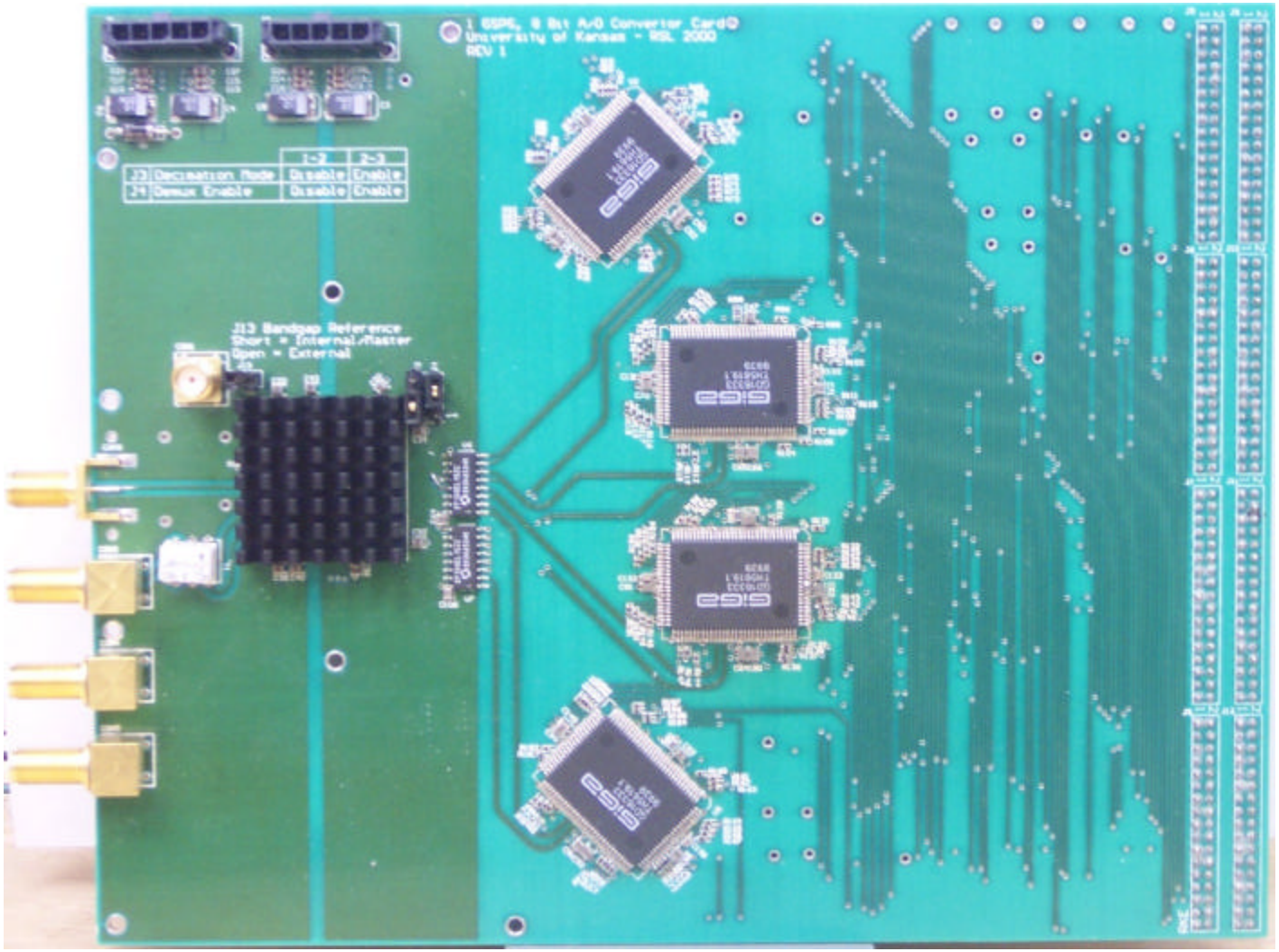
ADC Synchronization for Coherency

- Without synchronization, system coherency is lost
- Synchronization is made complex because of pipelined devices
- Synchronizing to a 1-GHz clock requires a 400 ps “window” on the sync pulse

1 GS/s ADC Card



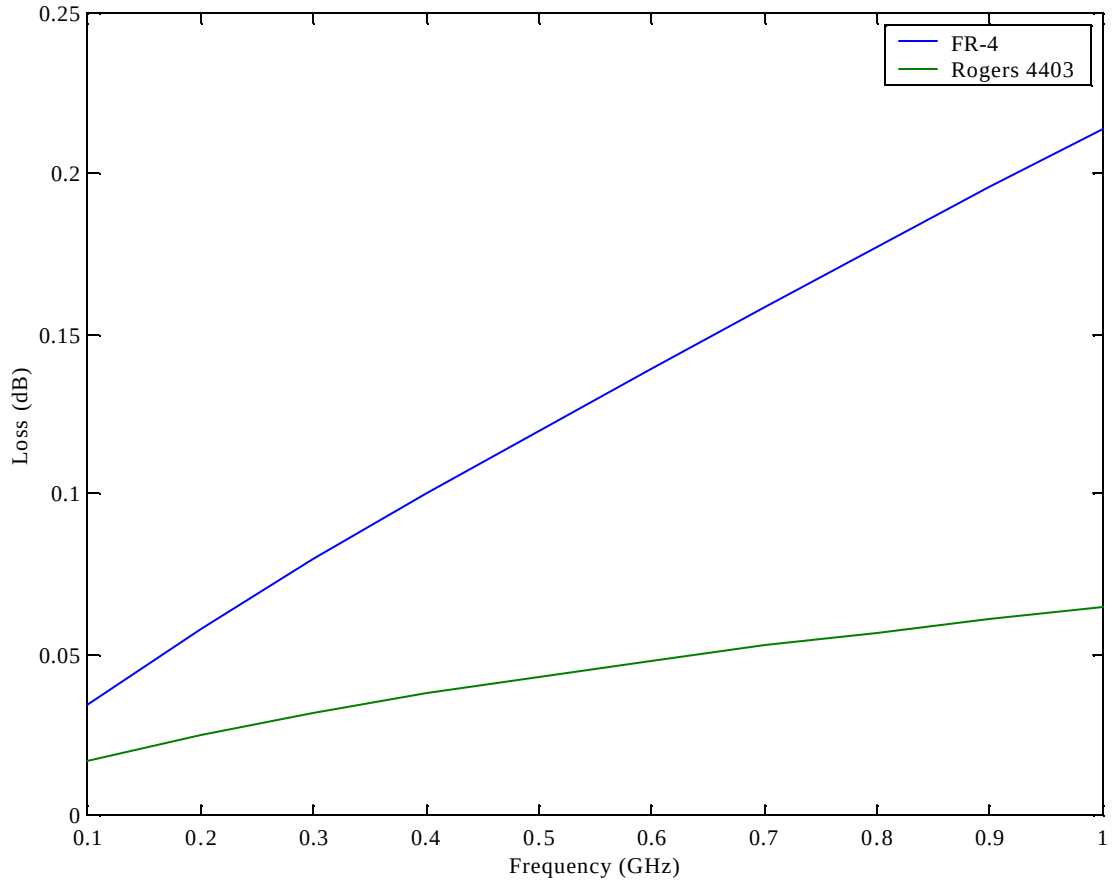
1 GS/s ADC Card



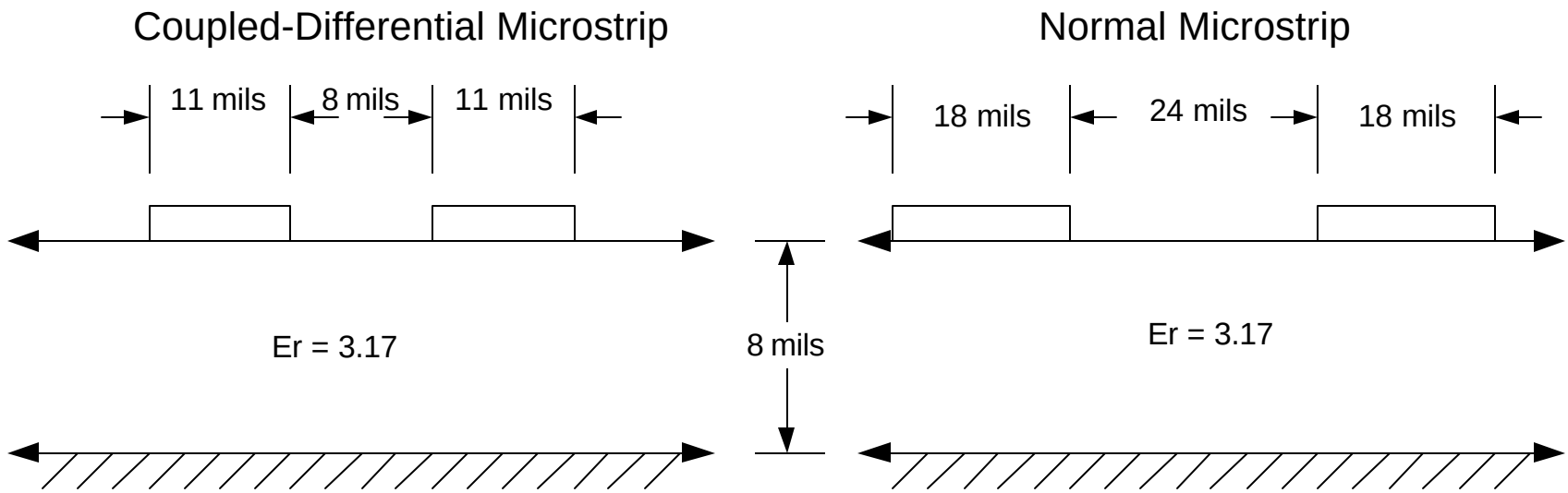
ADC Card PCB Specs

- ADC card
  - 6 layers using Rogers 4000 RF board material.
  - High resolution (5 mil line/spacing).
  - 6 ICs, 150 Resistors, 100 Capacitors.
  - Thermal Vias.

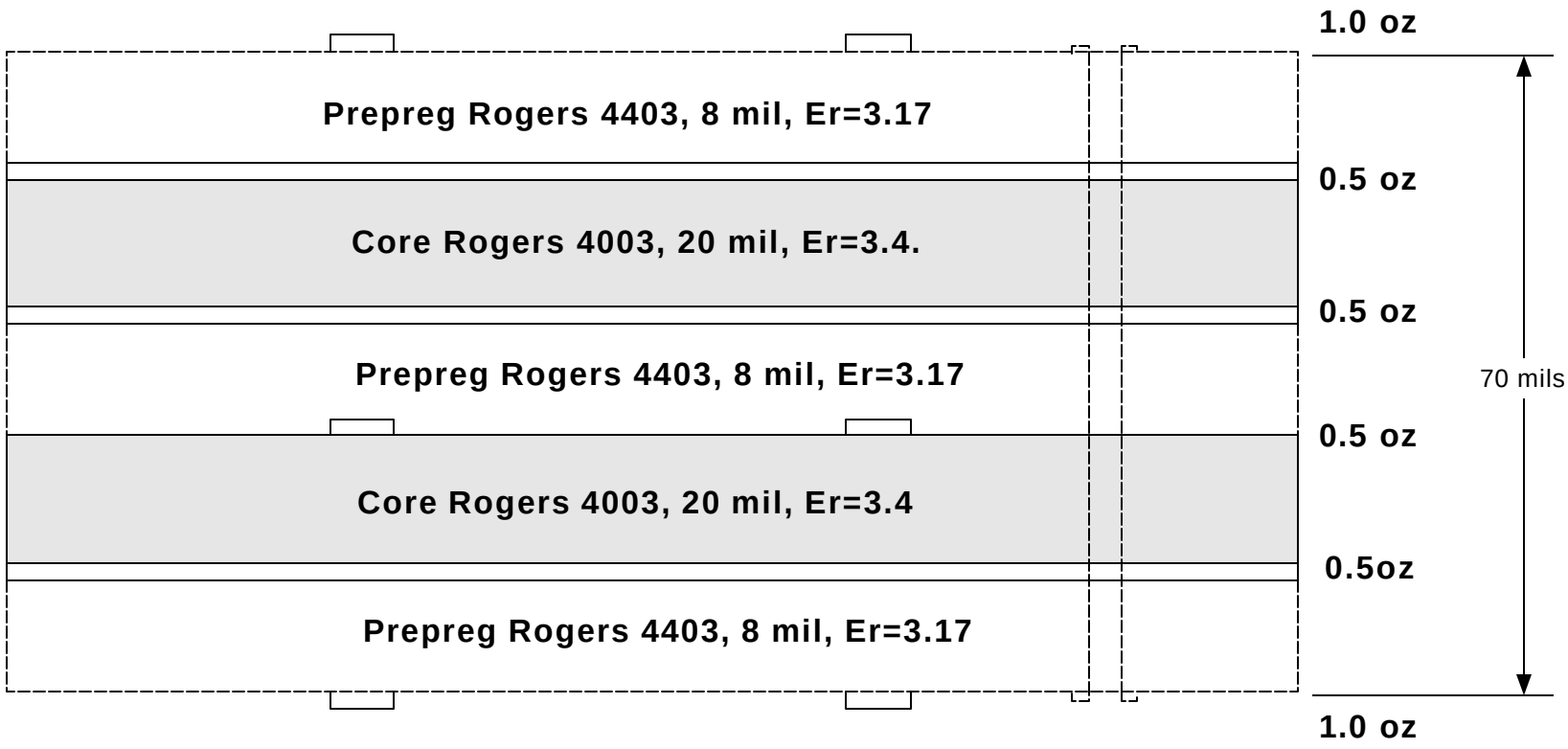
PCB Tangential Loss



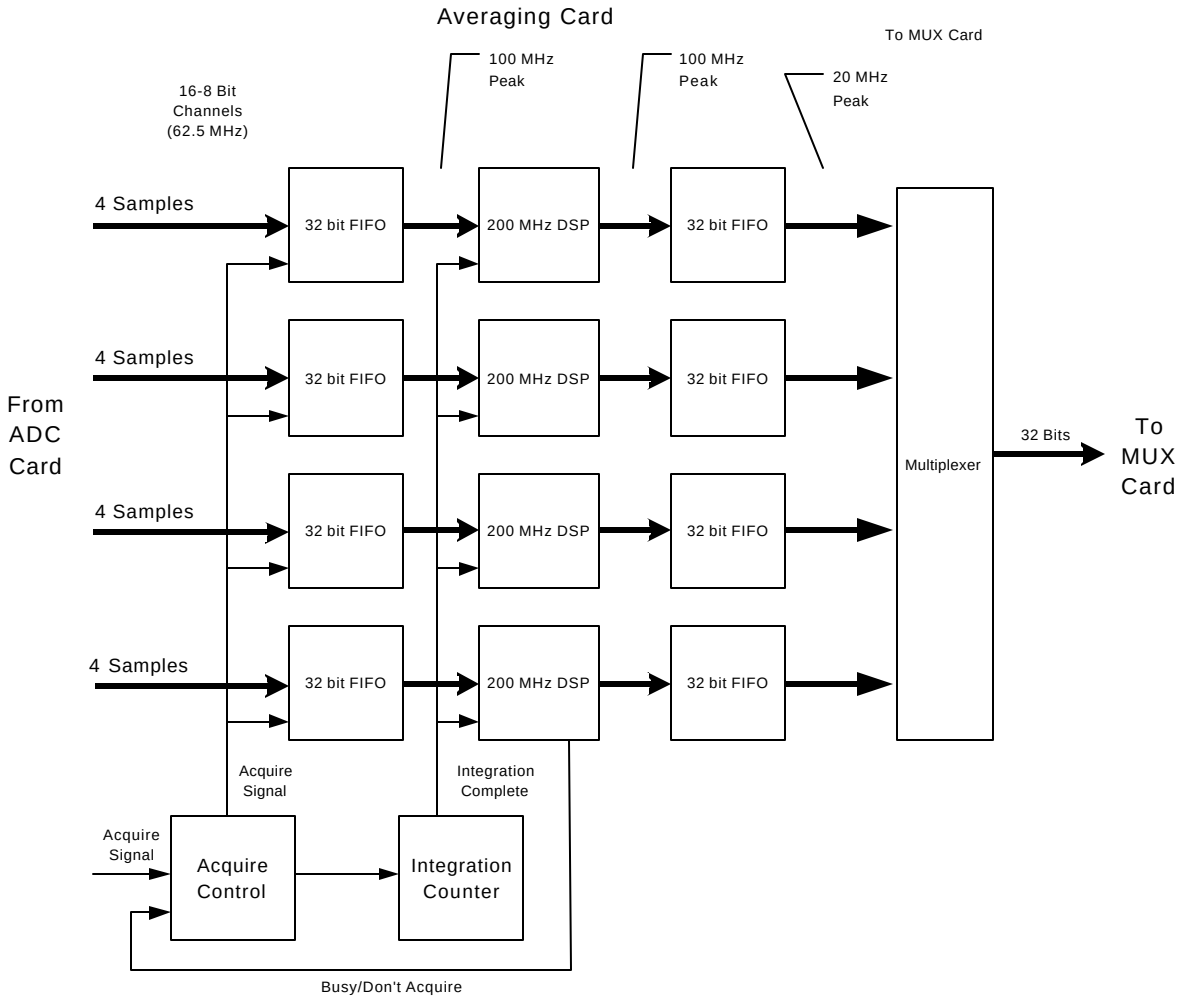
Coupled Differential Lines



ADC Card PCB Stackup



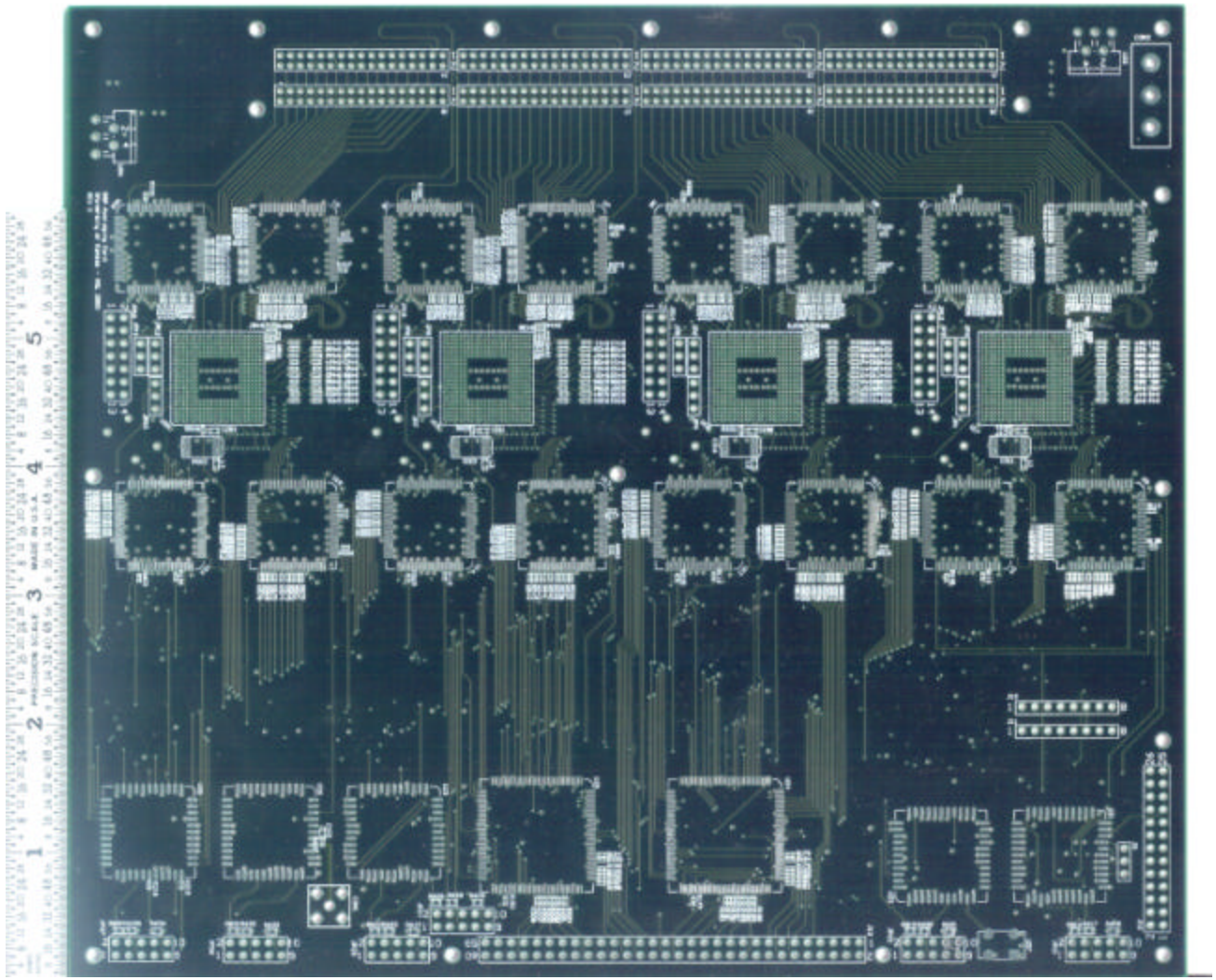
Averaging Card Diagram



Averaging Card Specifications

- 4 32-bit inputs, multiplexed 32 bit output
- Utilizes 200 MHz TI DSPs (1,600 MIPS)
- 133 MHz input FIFOs
- Designed to process 8,000 samples/channel at 30 kHz PRF (goal not met)
- Averages selectable from 1 to 65,535 in increments of 1

Averaging Card PCB

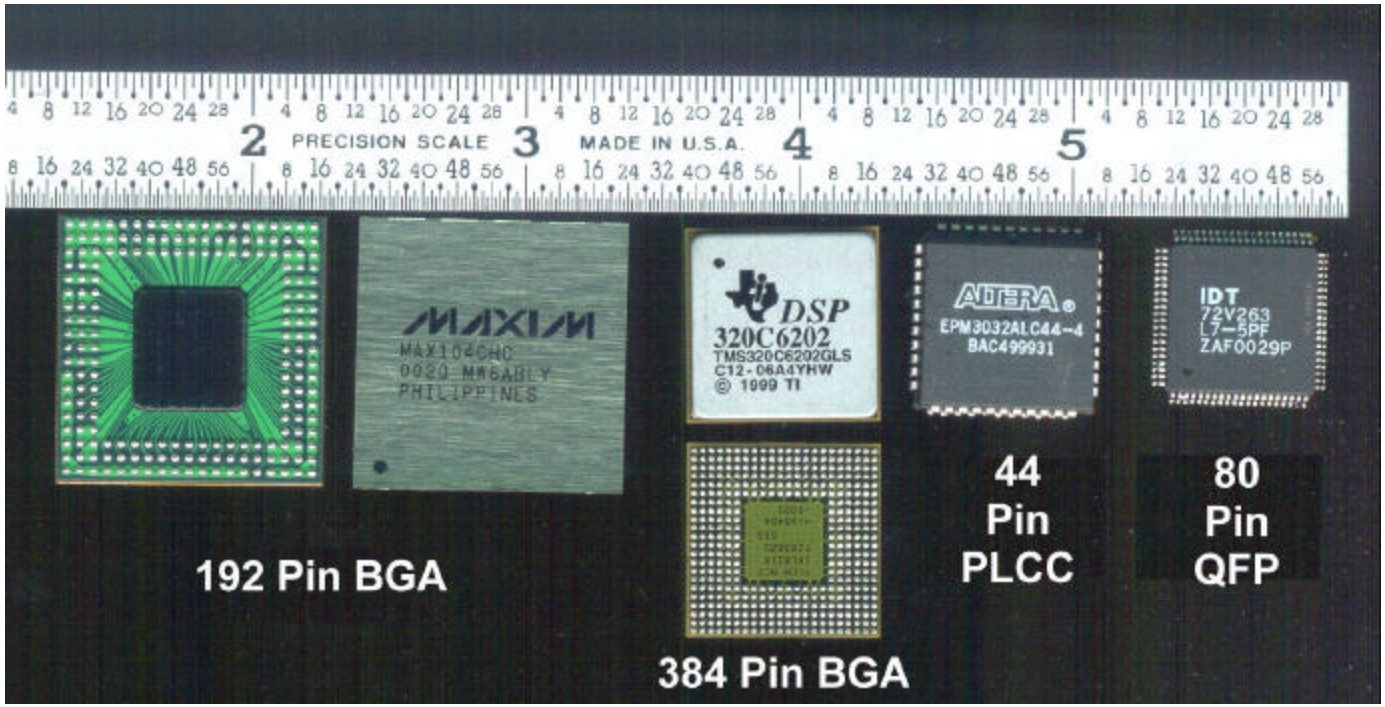


PCB Specifications

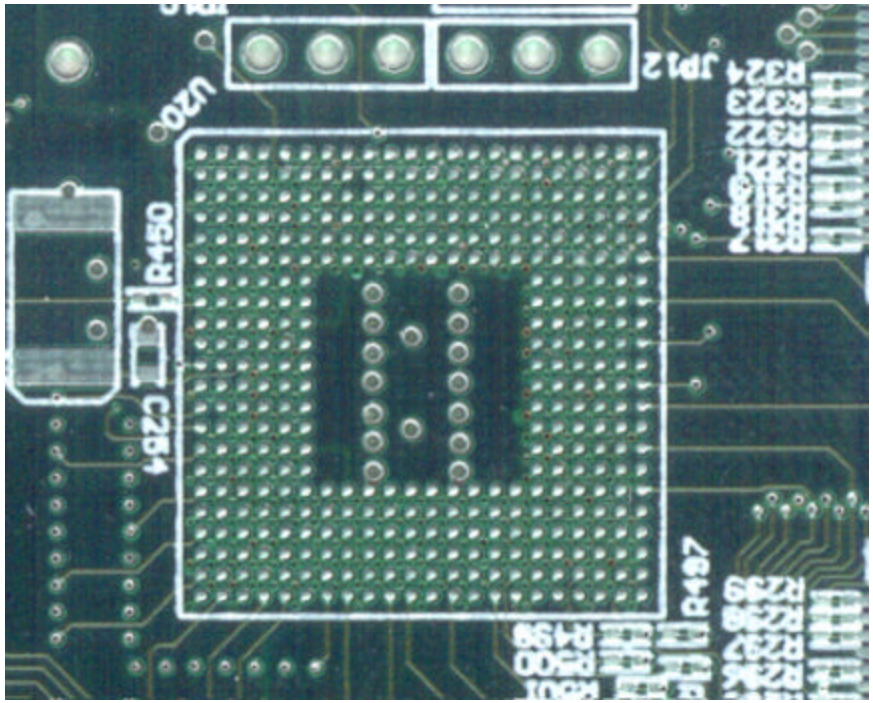
- 6 layer standard FR-4 board.
- High resolution (4 mil line width/spacing).
  - Created manufacturability issues
- 34 ICs, 600 resistors, 328 capacitors.
- Components on both sides.

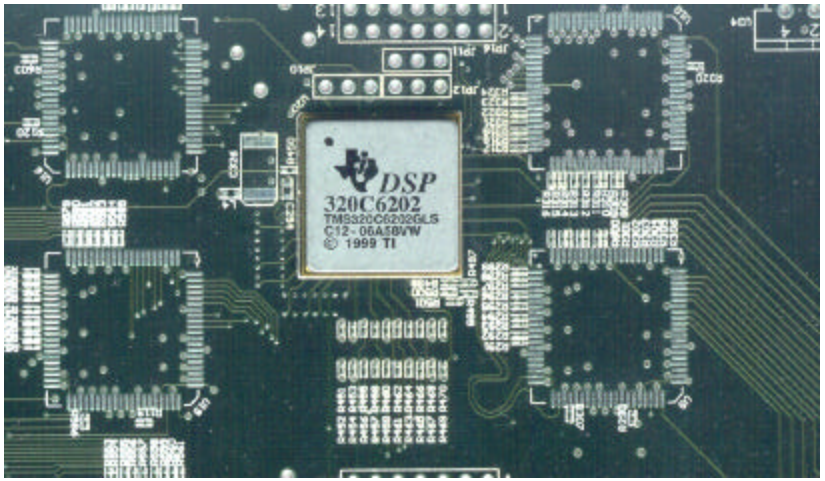
Packaging Technologies

- A key feature of the design is the use of Ball Grid Array (BGA) packaging technology
- Tiny balls of solder attach the bottom of the IC directly to the circuit board
- Increases pin density and performance



BGA Mounting

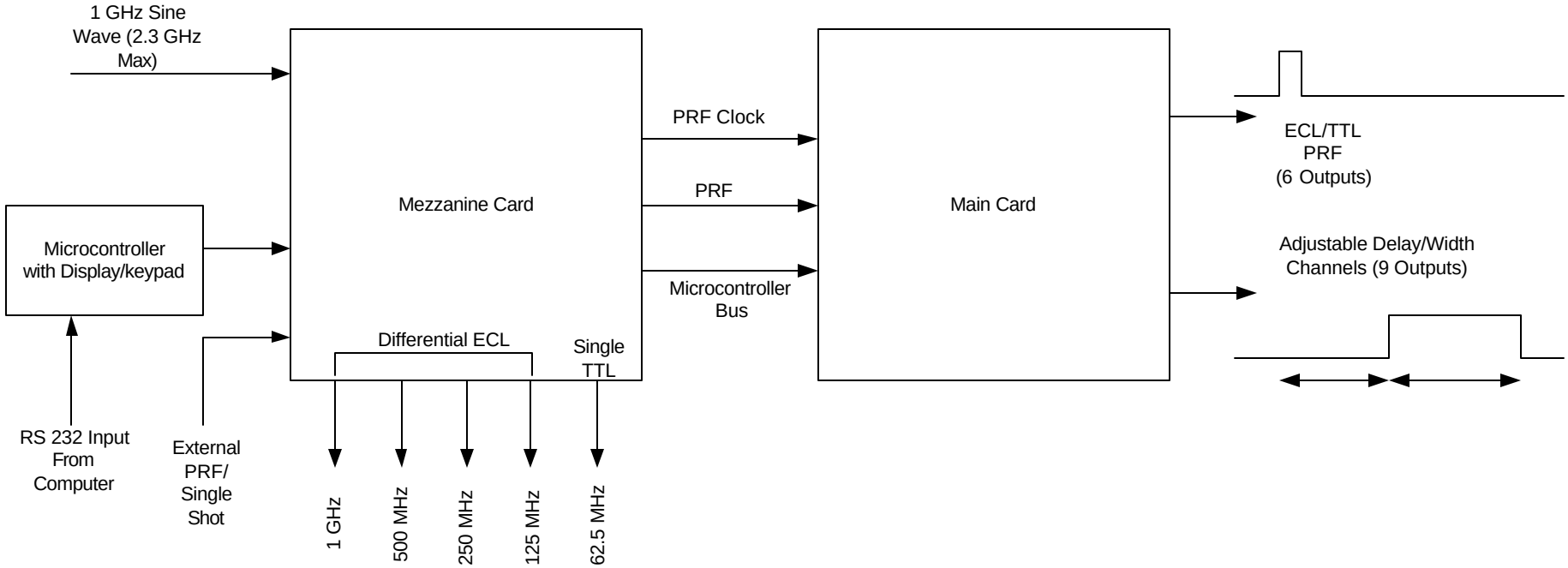




Averaging Card Design Problem

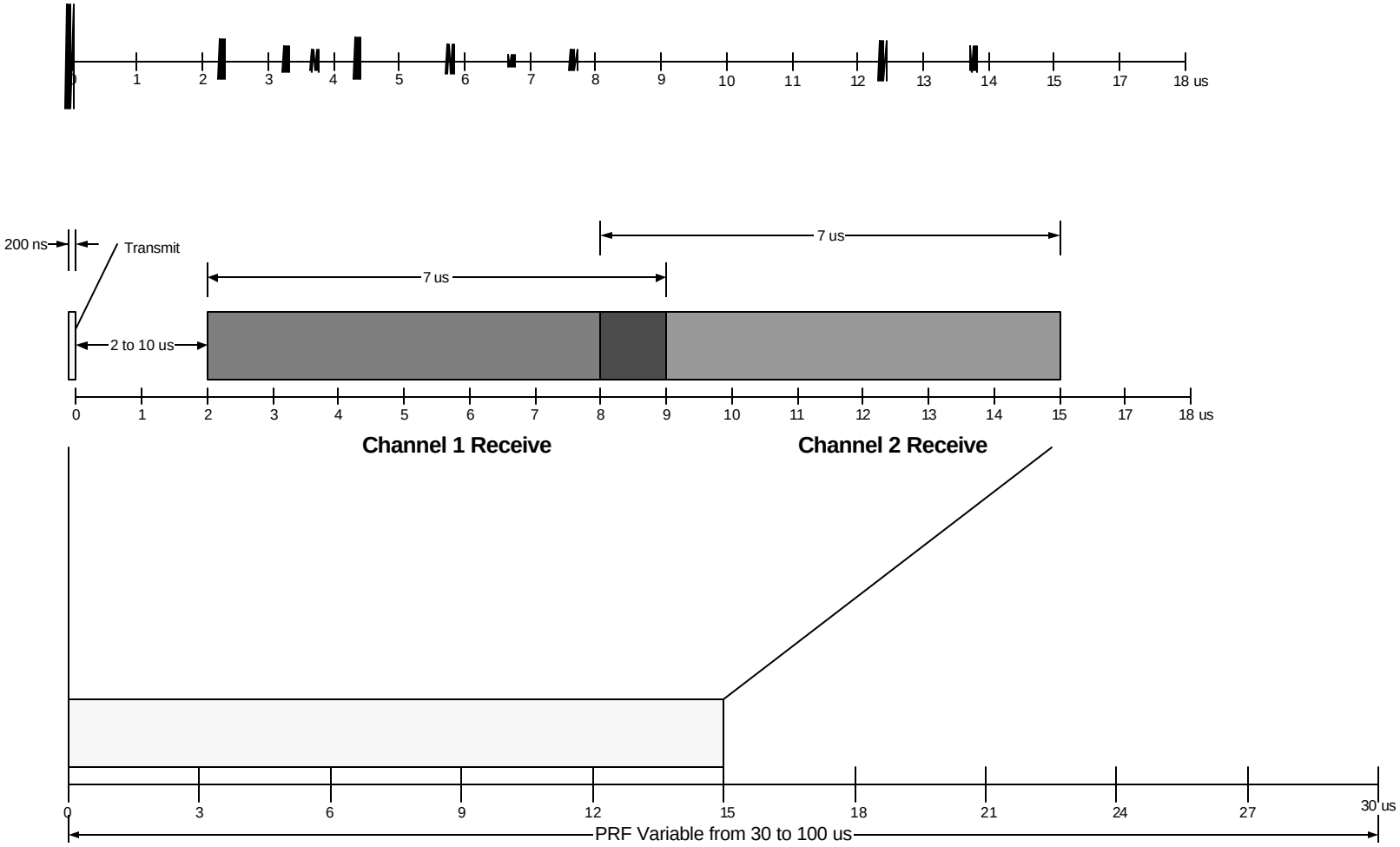
- Ultra fine pitch (0.8 mm) BGA resulted in the following manufacturing problems:
  - Required 4/4 mil PCB width/spacing and tiny vias resulting in low PCB yields
  - Devices did not solder correctly and board operation was intermittent.
- Wide pitch BGA (1.27 mm) on the ADC card was easy to design and manufacture

Universal Radar Timing System



- Stand alone radar timing system in 19” enclosure.
- Computer or manual control.
- Accepts input clock from 100 MHz to 2.3 GHz.

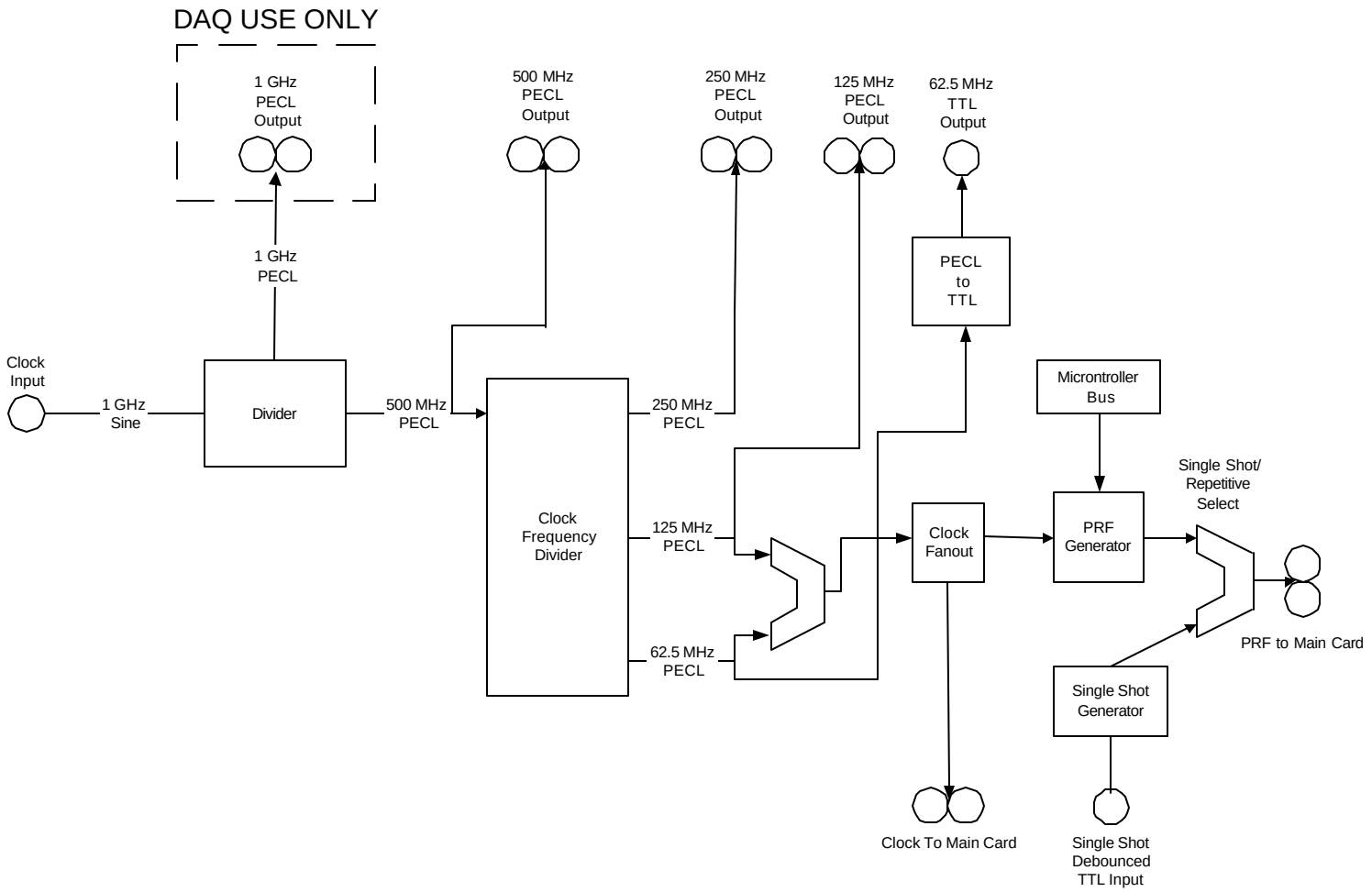
Radar Timing



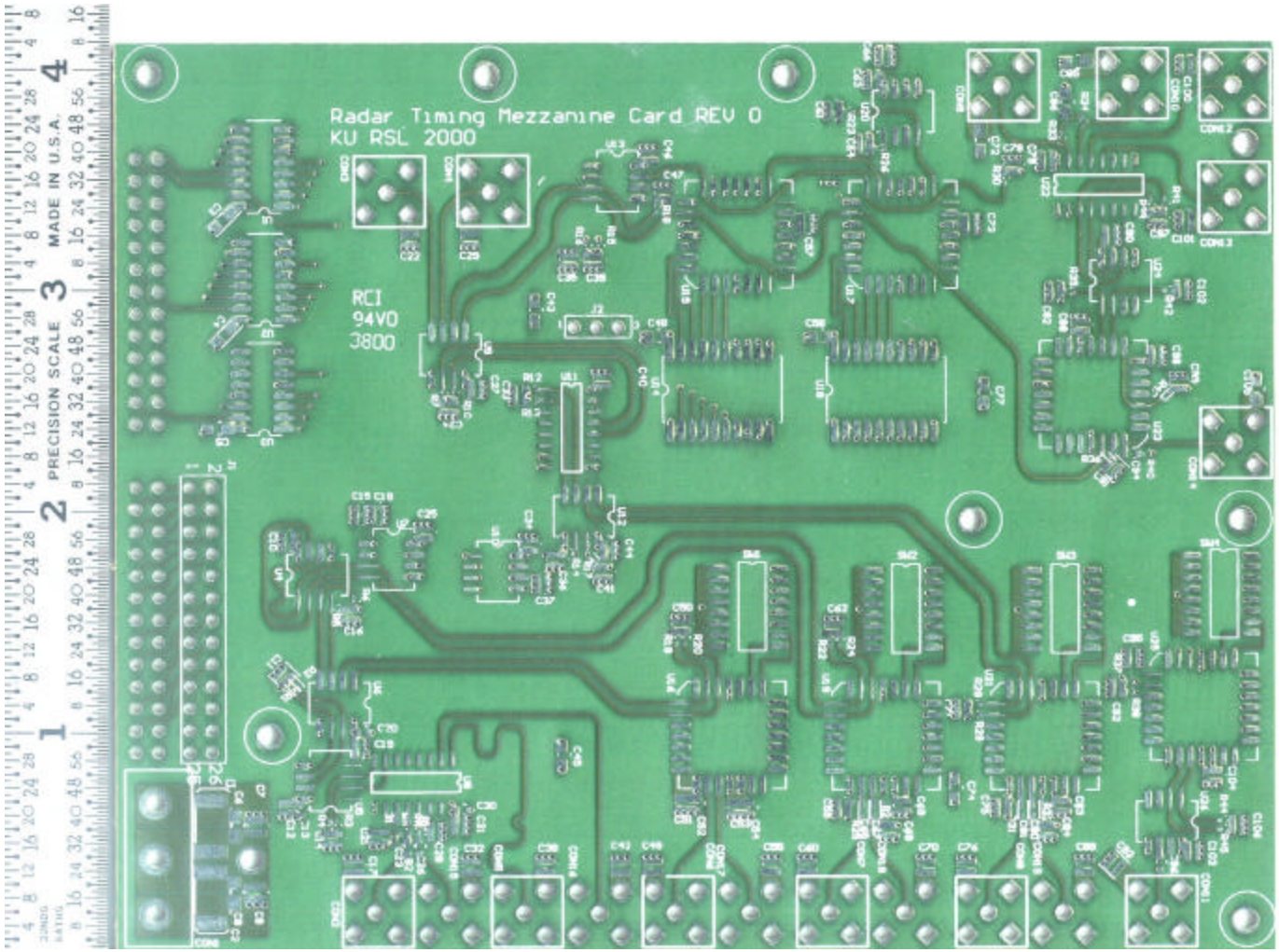
Timing System Specifications

- Sine wave clock input
- 2.3 GHz maximum input frequency
- Generates radar PRF signal (1 kHz minimum, 16 ns steps)
- Generates 9 adjustable timing “windows”
- Outputs divided versions of input clock
- Signals edges must be adjustable to a 400 ps window
  - Required for ADC sync signal
  - Accomplished with ECL technology

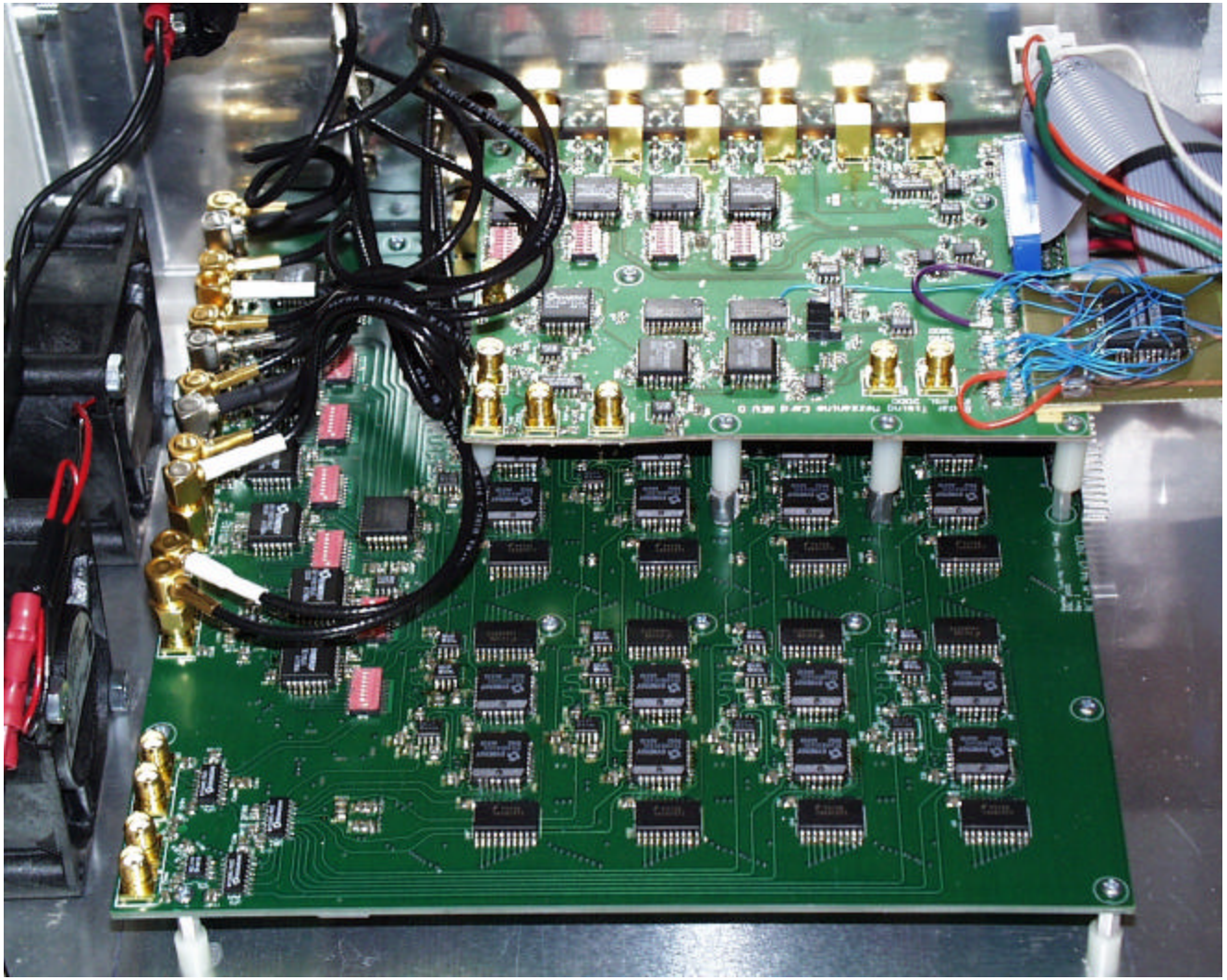
Mezzanine Card Diagram



Mezzanine Card



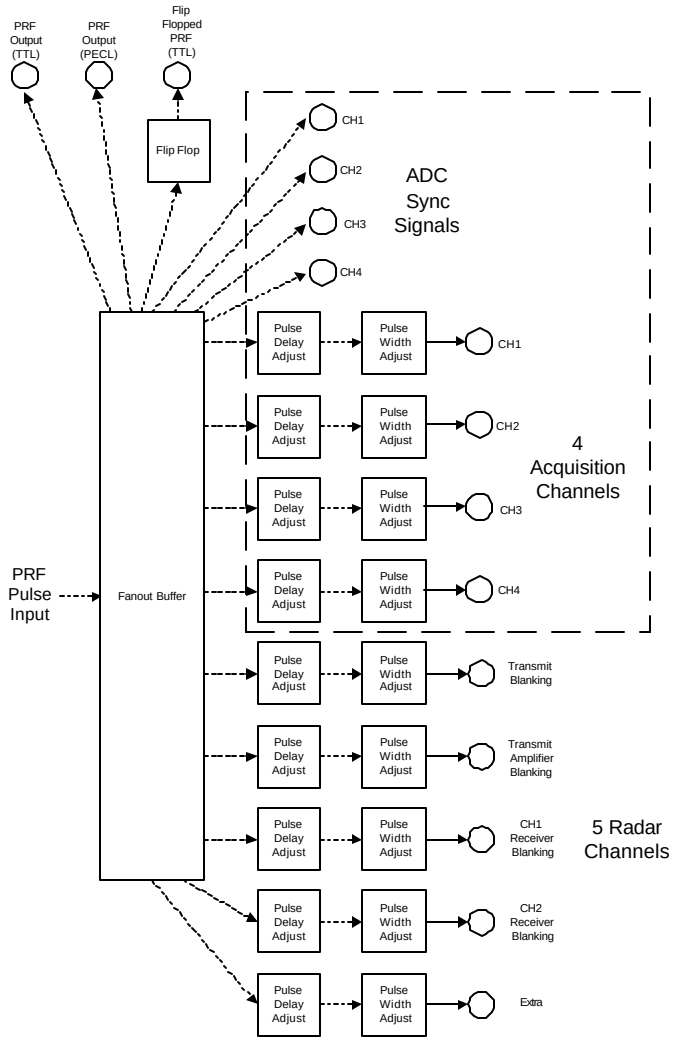
Mezzanine Card (in system)



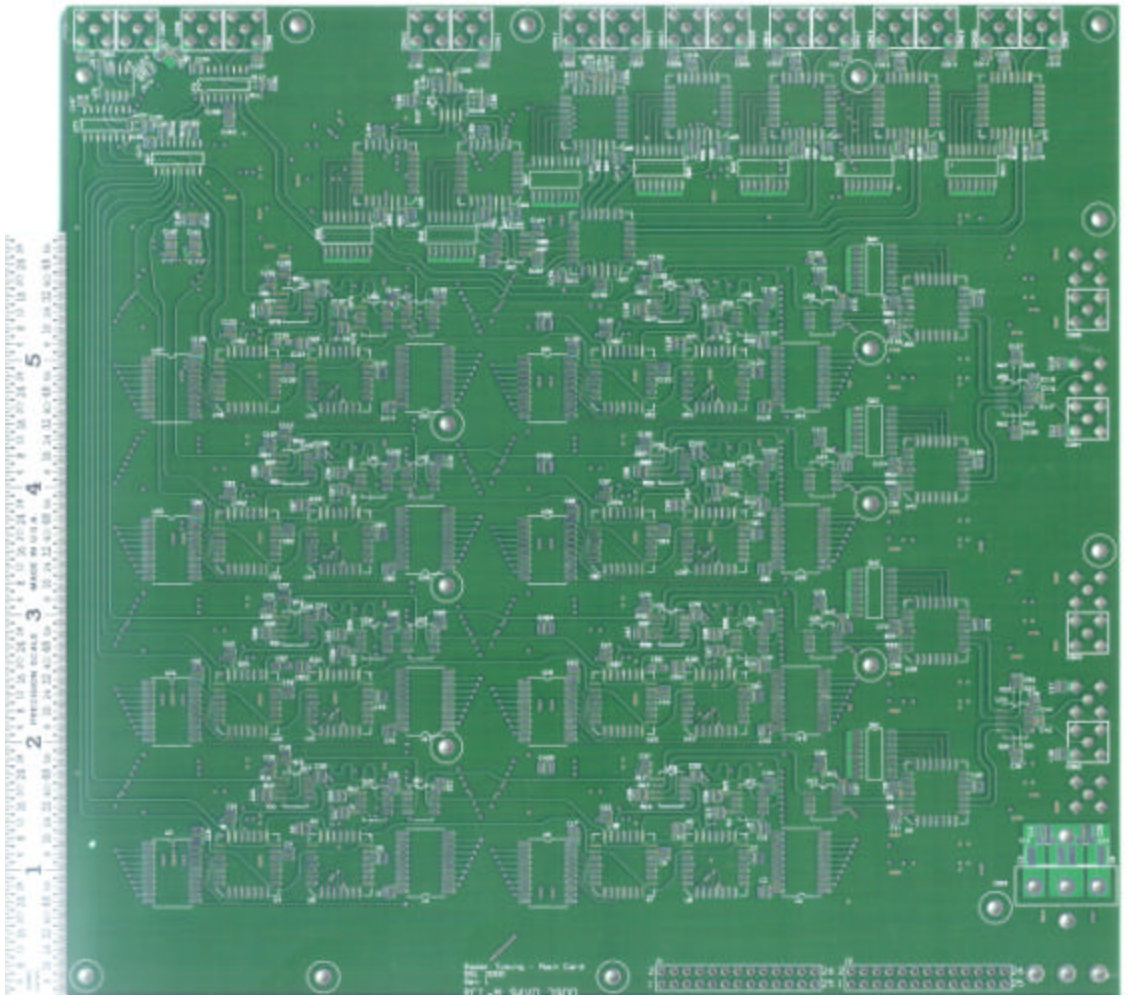
Mezzanine Card PCB Specifications

- 6 layers using Rogers 3000 RF board material
- 22 ICs, 40 Resistors, 100 Capacitors
- Measured power consumption: 10W (2A @ 5V)

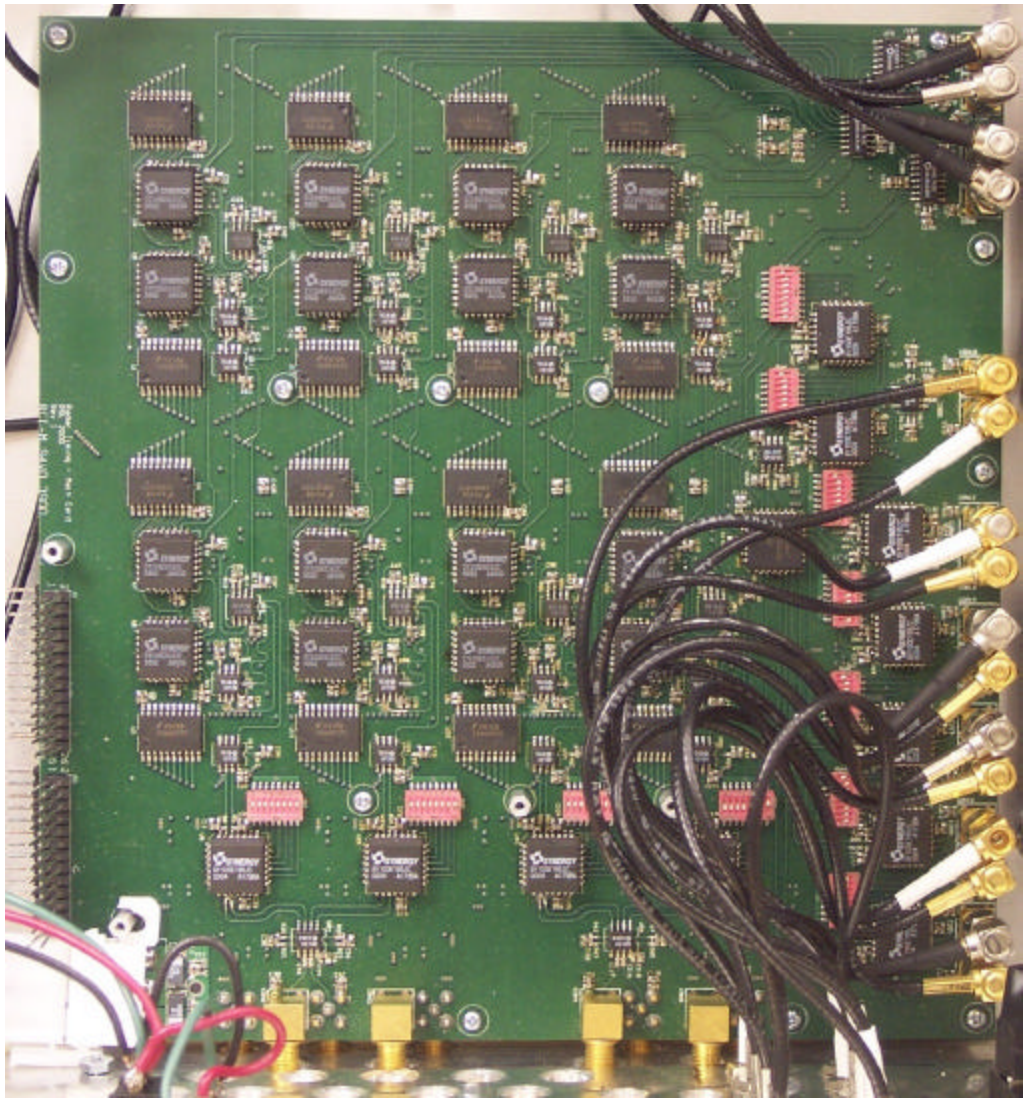
Main Card Diagram



Main Card PCB



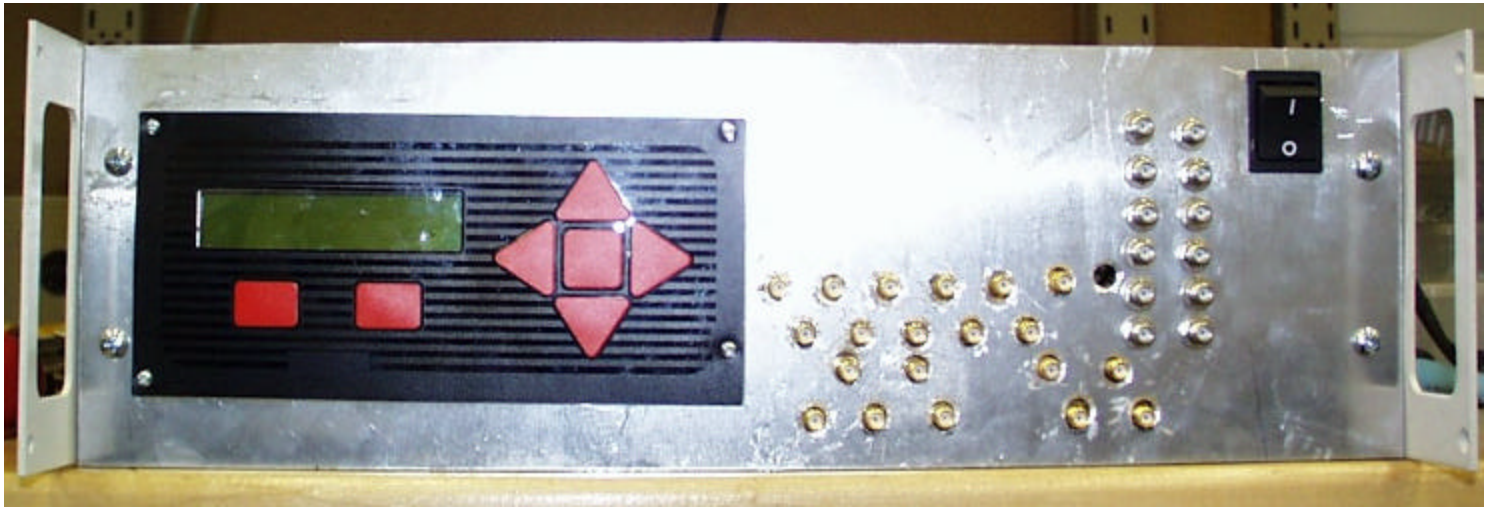
Main Card Finished PCB



Main Card PCB Specifications

- 8 layers using standard FR-4 material.
- 155 ICs, 224 resistors, 420 capacitors.
- Components on both sides.
- Blind vias to maximize density
- Measured power consumption: 54W (10.7A @ 5V)

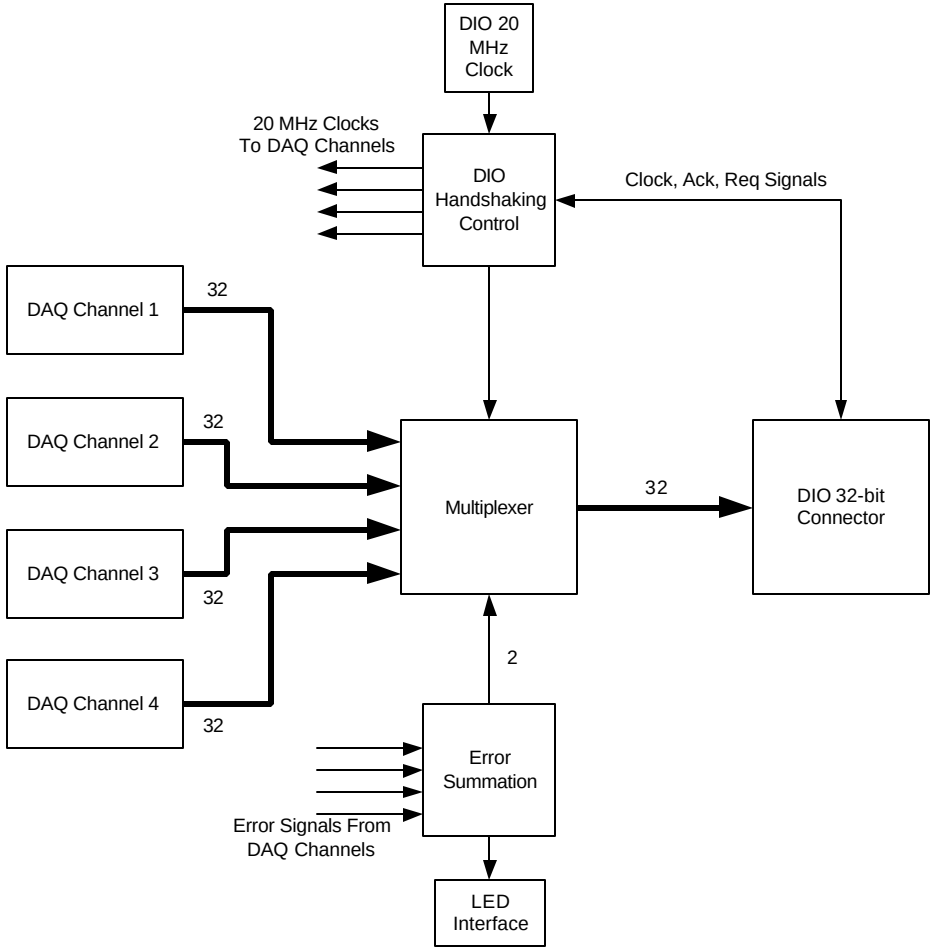
Timing System



LCD Front Panel

Multiplexer Card

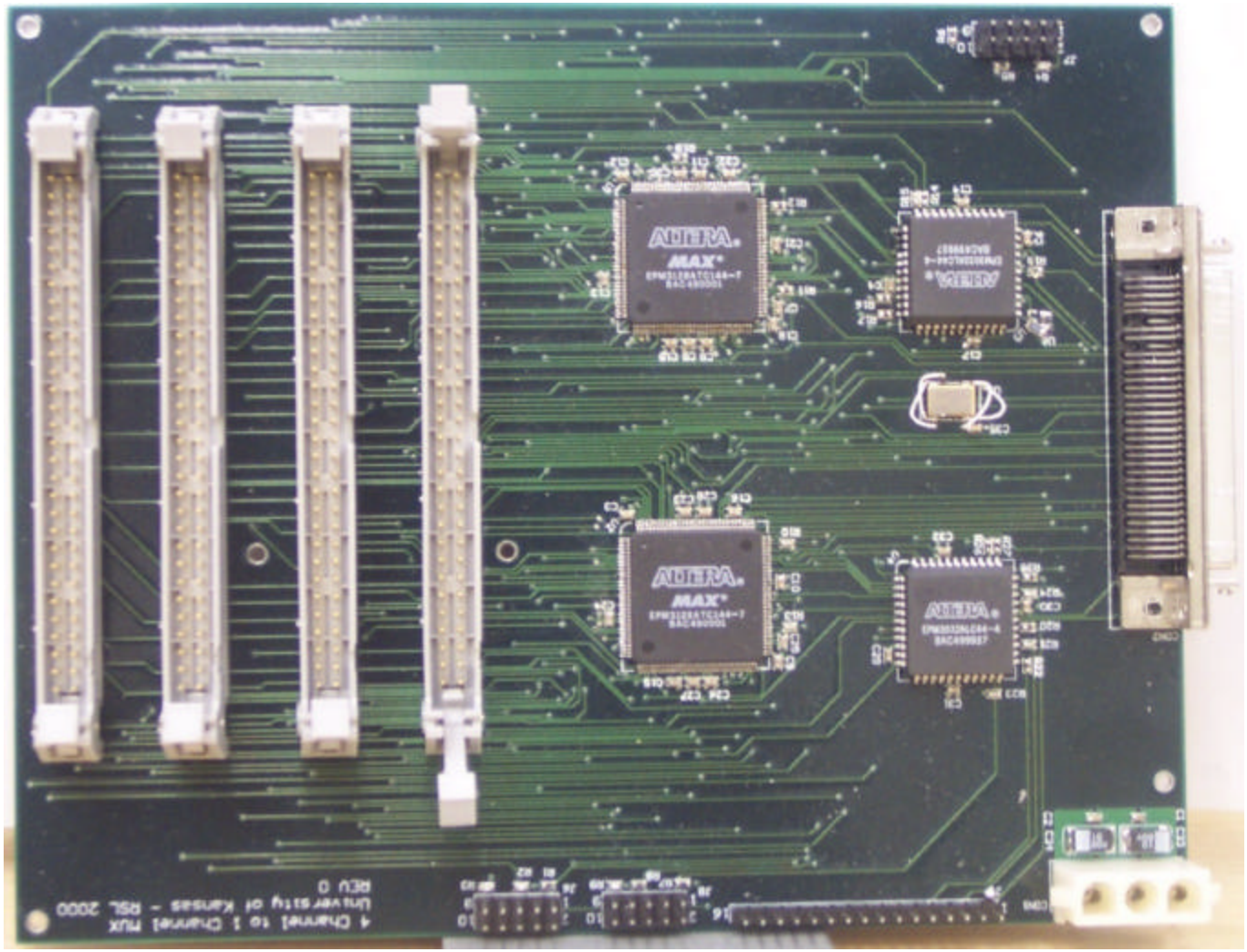
Multiplexer Card Diagram



Multiplexer Card Specifications

- Converts 4 32-bit channels into a single 32-bit channel
- Provide handshaking with computer DIO card (NI DIO 32HS)
- Operates at 20 MHz (80 Mbyte/s peak rate)
- Consolidates 8 error signals into 2 signals for computer link

Finished Multiplexer Card



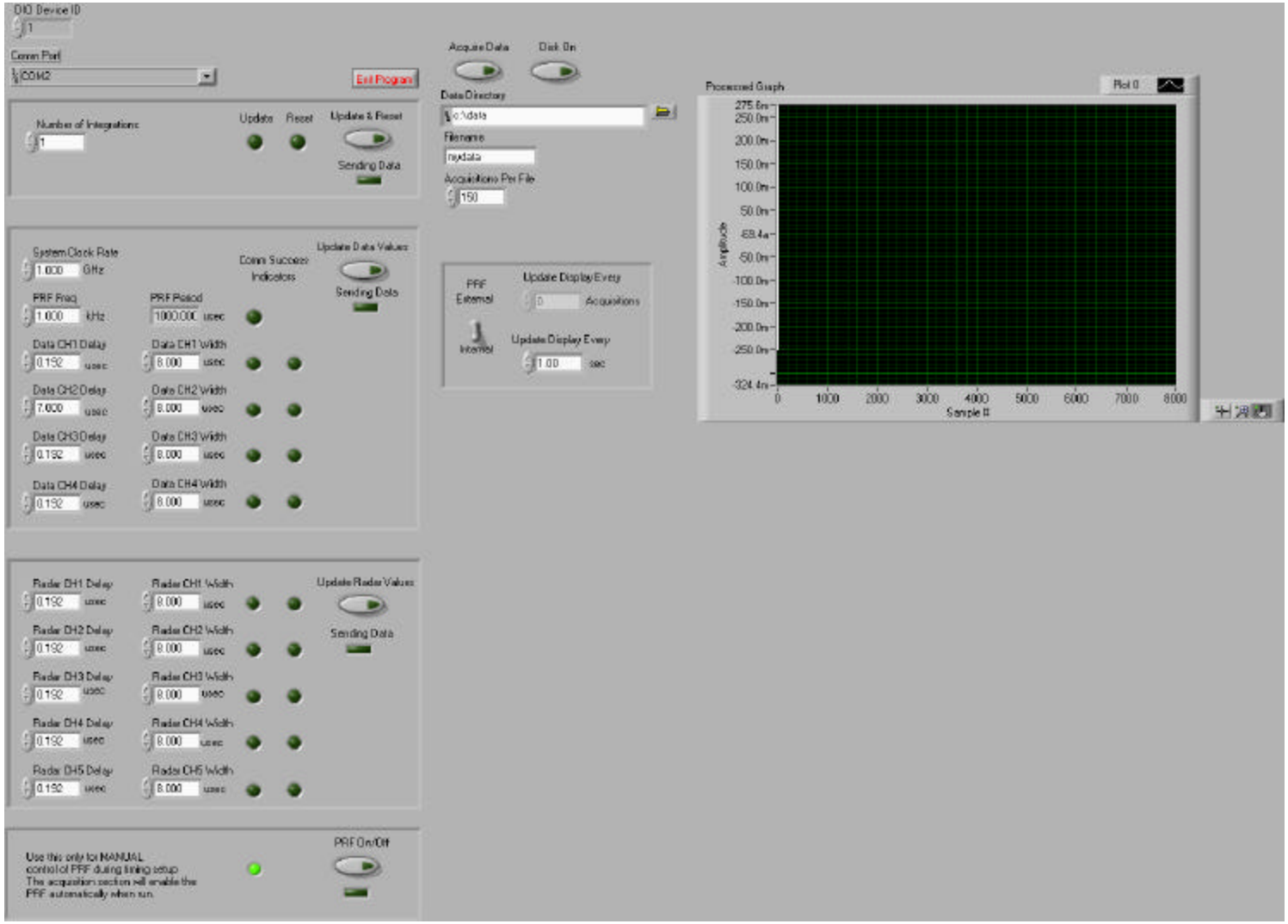
Multiplexer Card PCB Specs

- 4 layer FR-4, 2 signal layers
- Board routed using an autorouter

User Interface Software

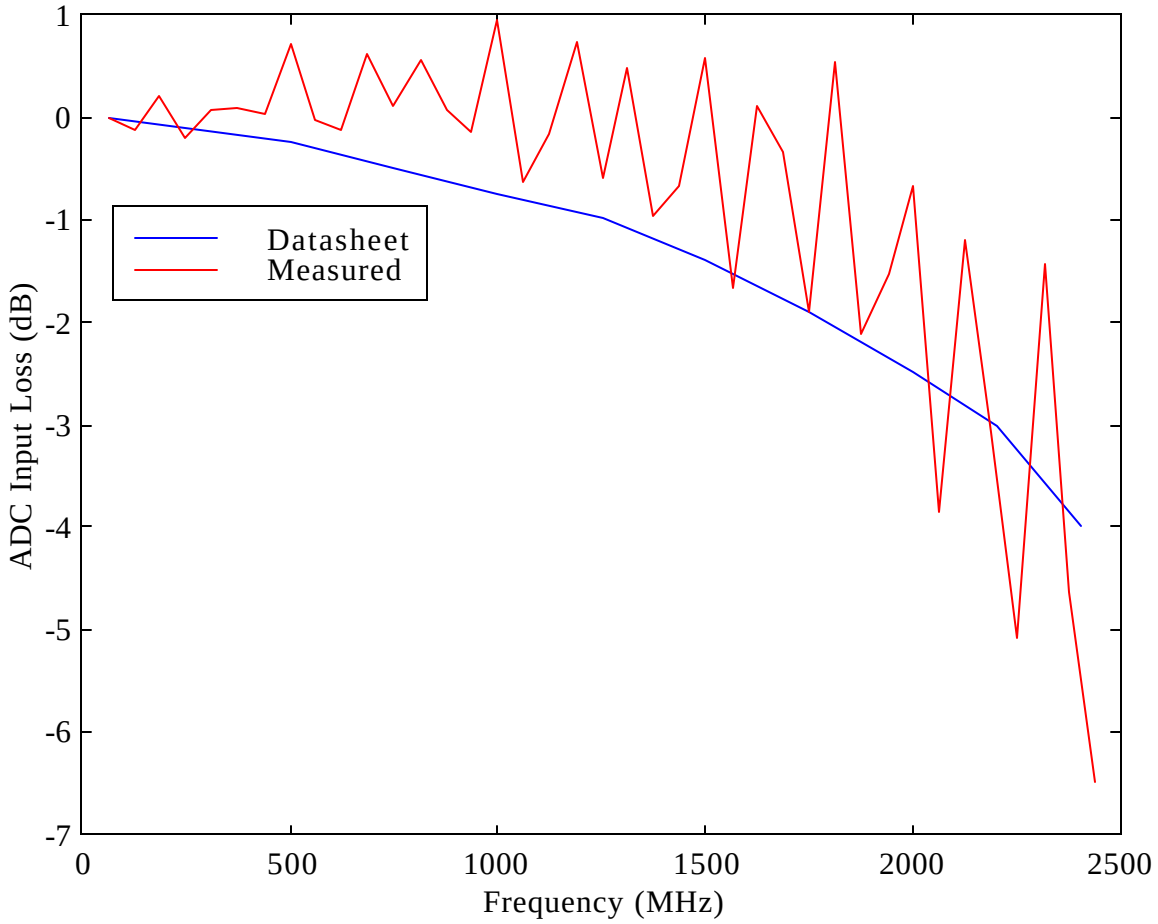
- Labview used to create acquisition software
  - Provides graphical programming environment
  - DIO low level routines pre-written
  - RS 232 low level routines pre-written

GUI Front Panel

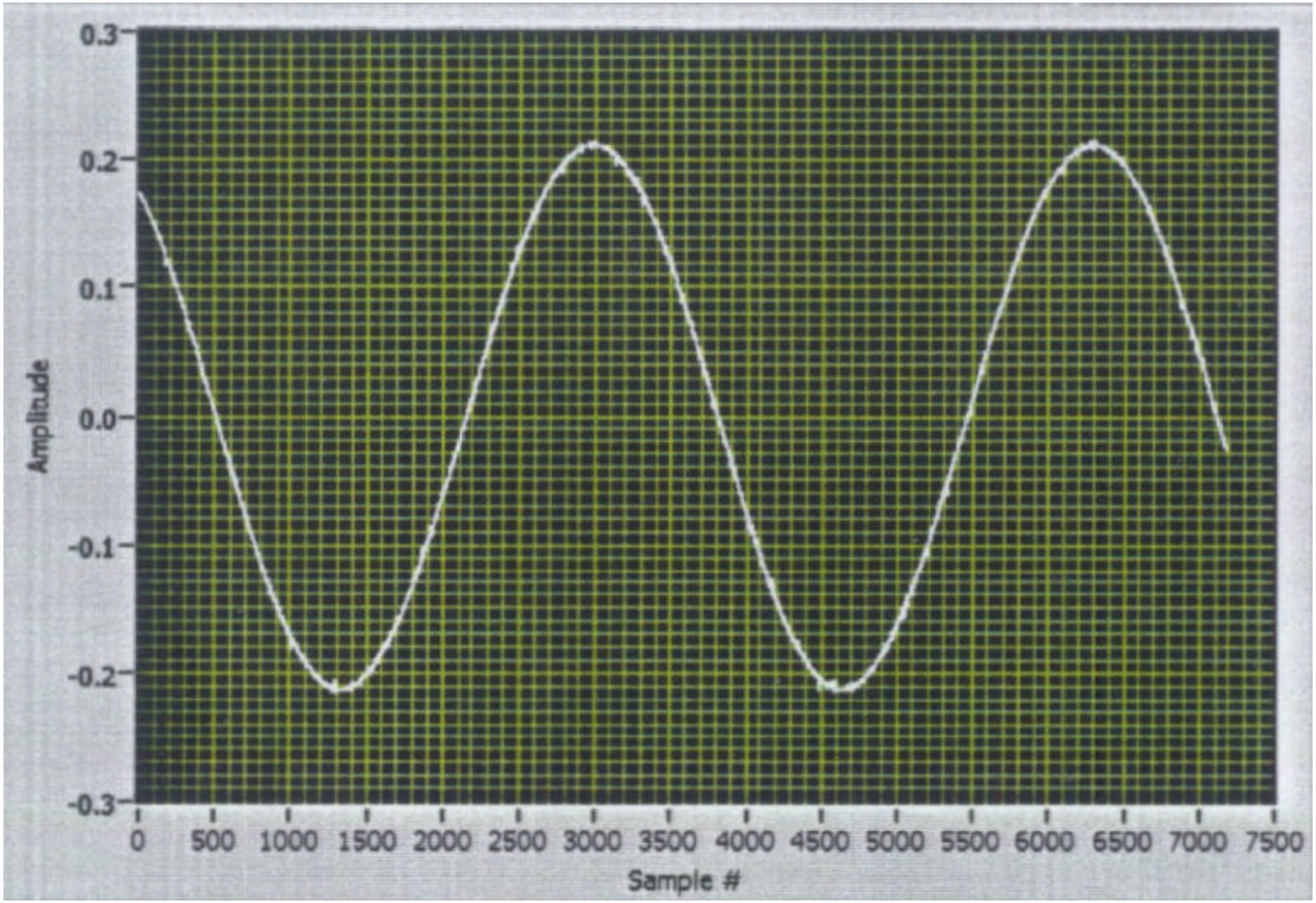


System Performance/Results

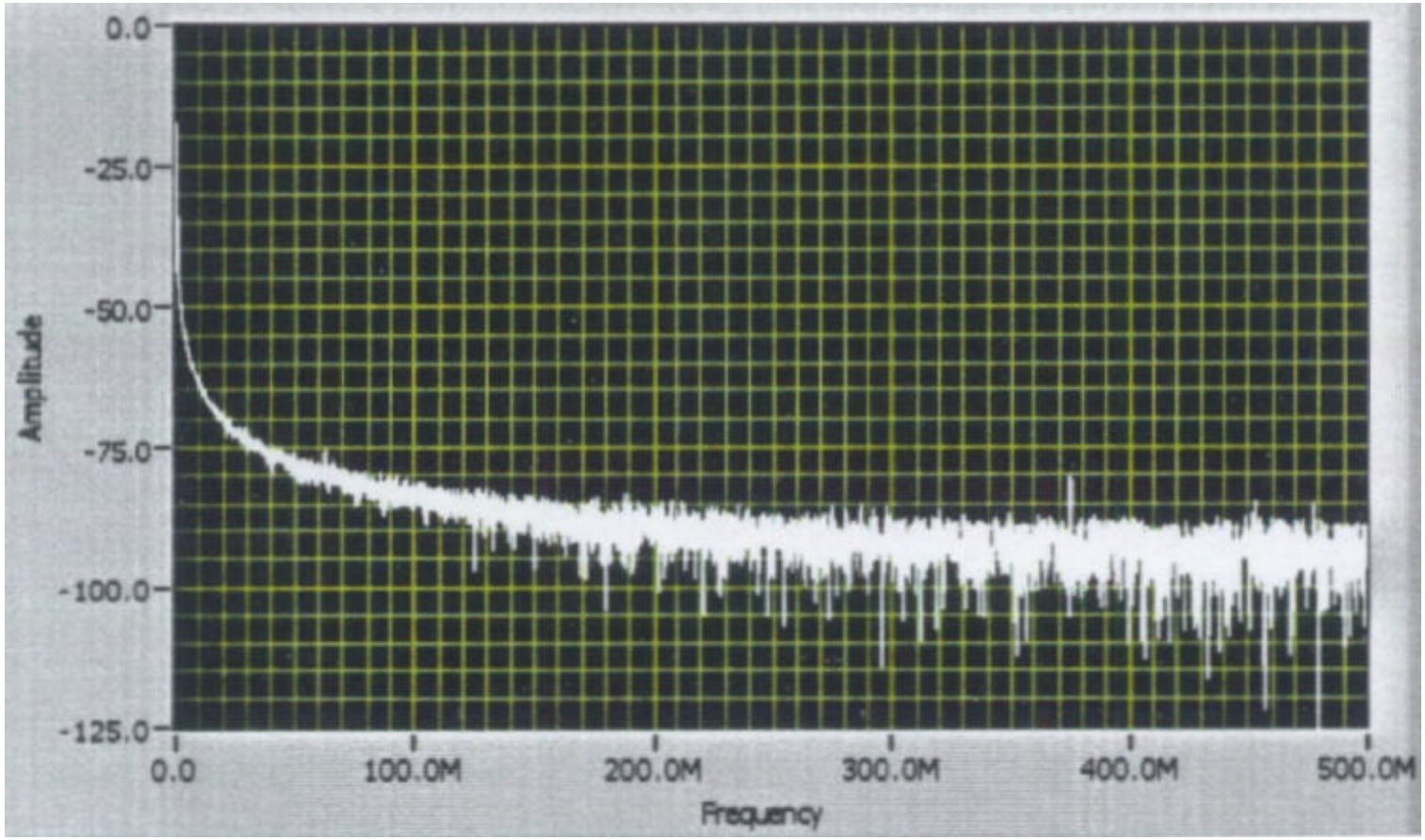
ADC Performance



System Time Domain Output



System Frequency Domain Output



Performance Summary

- ADC analog input was verified to operate over 2.2 Ghz
- System capture and record was verified
- ADC SFDR was measured to be 63 dB (62-69 dB datasheet)
- System throughput to the drive: 1.3 Mbyte/s
- Coherent averaging demonstrated but malfunctioning average card prevented adequate testing
- Timing system operated to 2.3 Ghz
- Averaging card maximum PRF is 10 kHz

Project Summary

- 4 of 5 circuit boards work at or above requirements
- Timing system is complete and validated
- Averaging card needs additional development work
- Labview software is ~90% complete (pending average card work)

The End